

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from PCLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

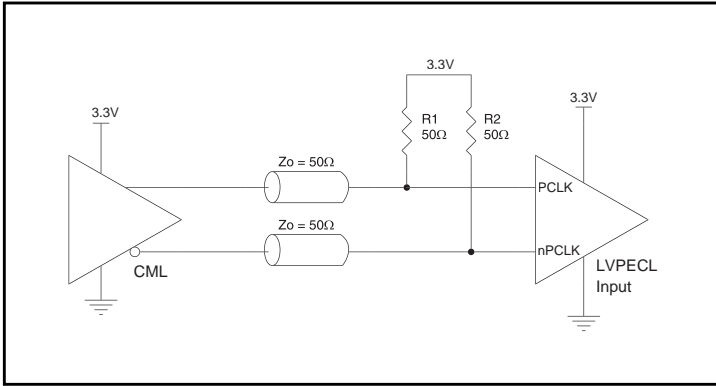


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

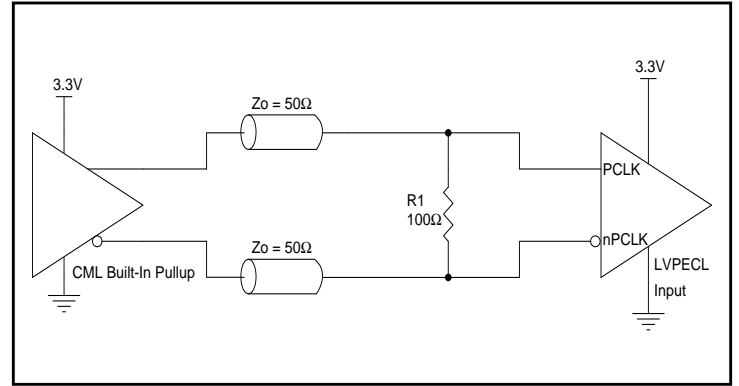


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

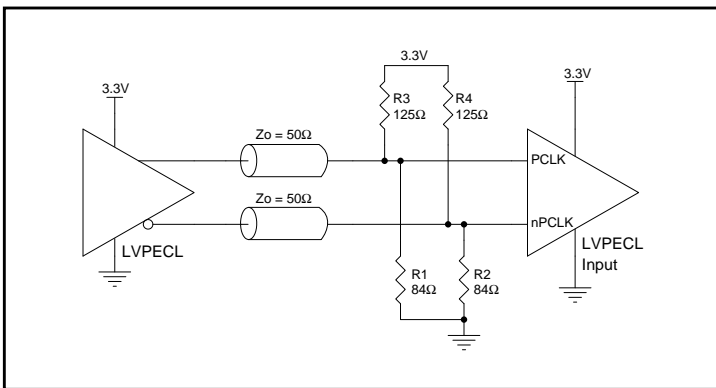


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

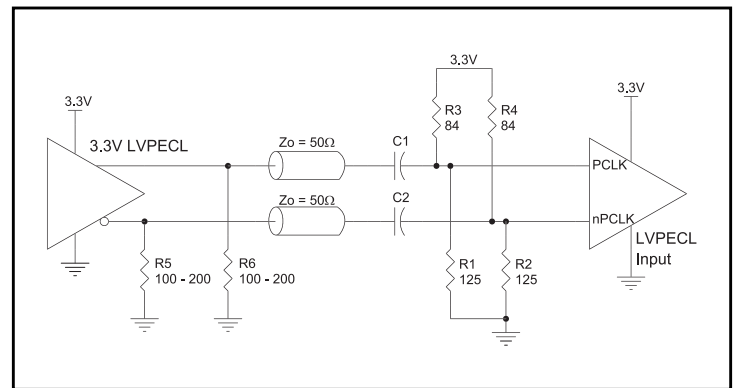


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

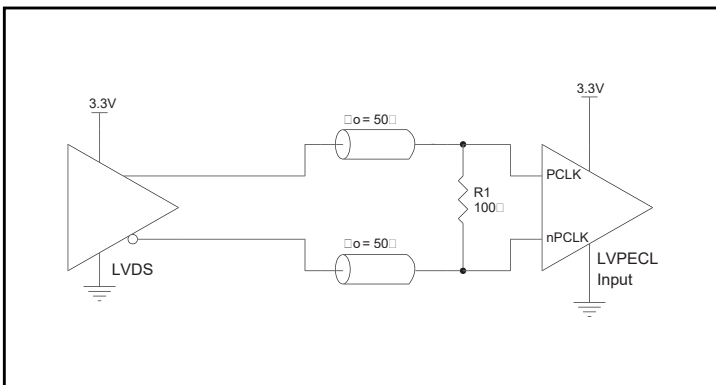


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

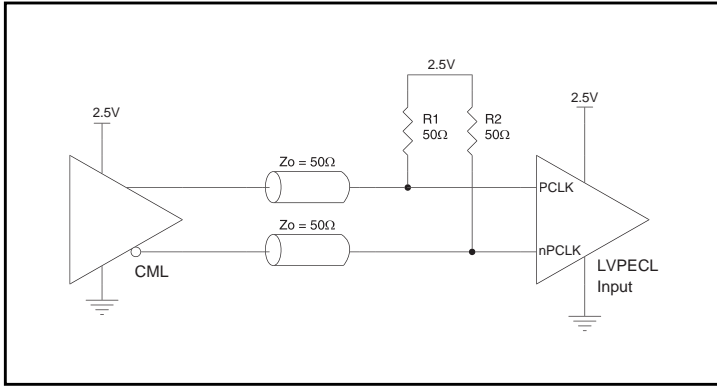


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

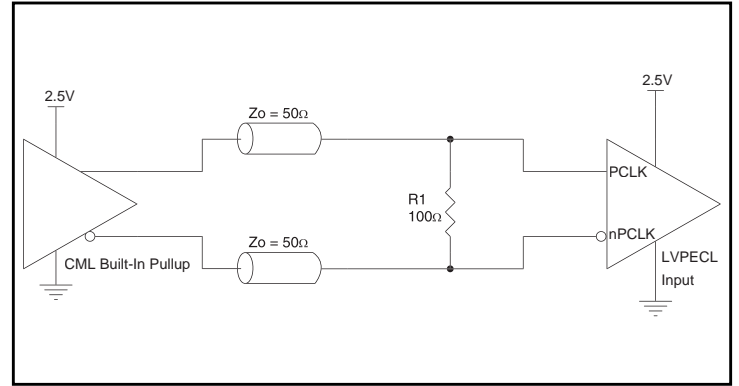


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

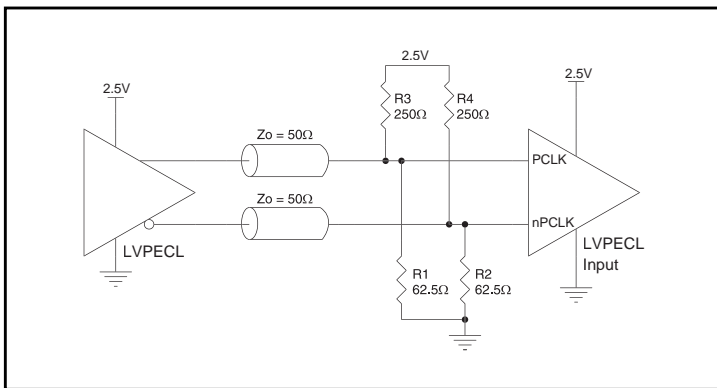


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

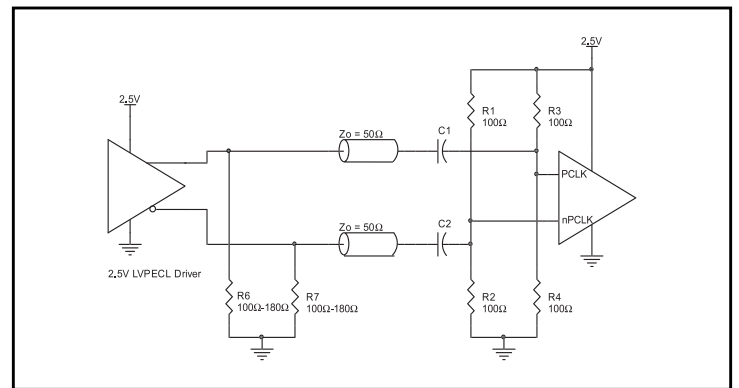


Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

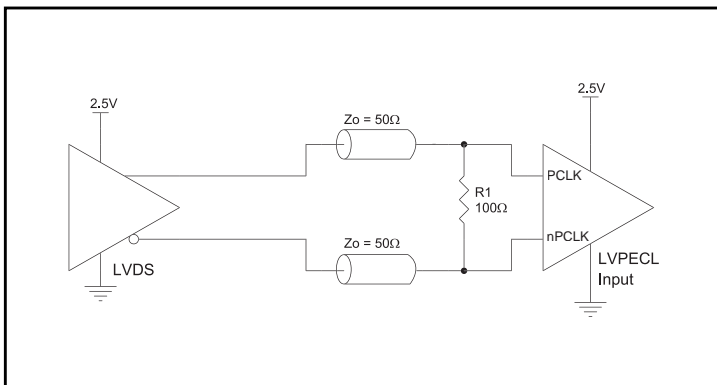


Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

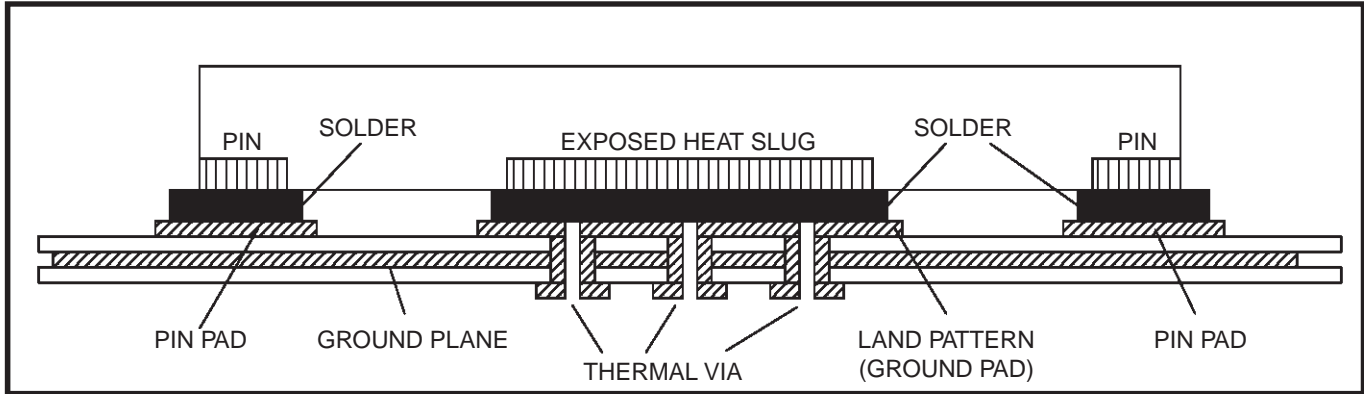


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 5A and 5B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

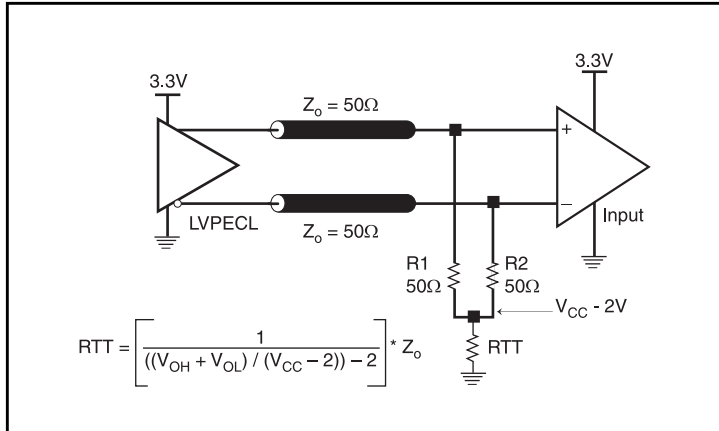


Figure 5A. 3.3V LVPECL Output Termination

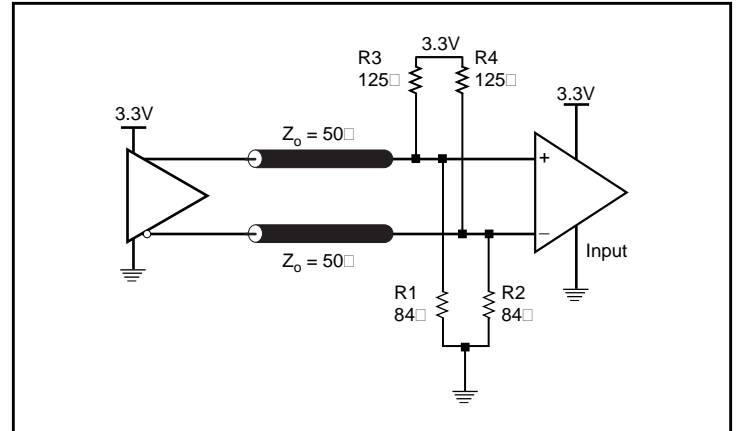


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground

level. The R3 in Figure 6B can be eliminated and the termination is shown in Figure 6C.

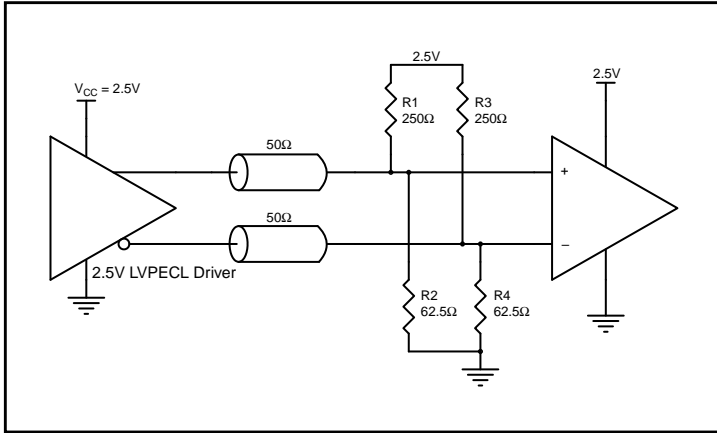


Figure 6A. 2.5V LVPECL Driver Termination Example

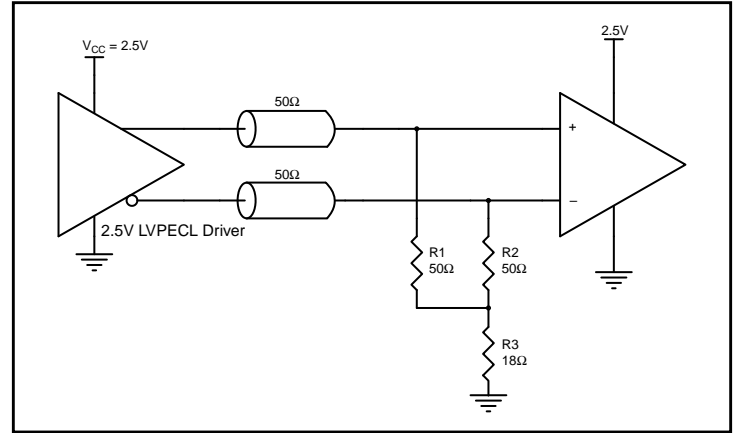


Figure 6B. 2.5V LVPECL Driver Termination Example

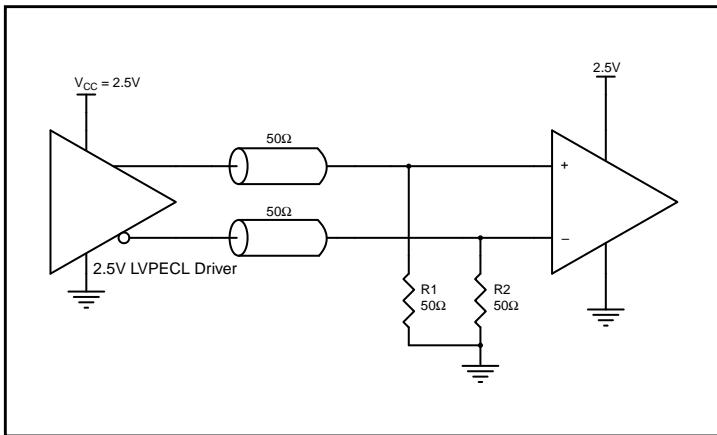


Figure 6C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8SLVP2102I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8SLVP2102I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85° is as follows:

$$I_{EE_MAX} = 56mA$$

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 56mA = \mathbf{194.04mW}$
- Power (outputs)_{MAX} = **36mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 36mW = \mathbf{144mW}$

$$\mathbf{Total\ Power_{_MAX}} (3.465V, \text{ with all outputs switching}) = 194.04mW + 144mW = \mathbf{338.04mW}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 5 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.338W * 74.7^\circ C/W = 110.2^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 16-Lead VFQFPN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7*.

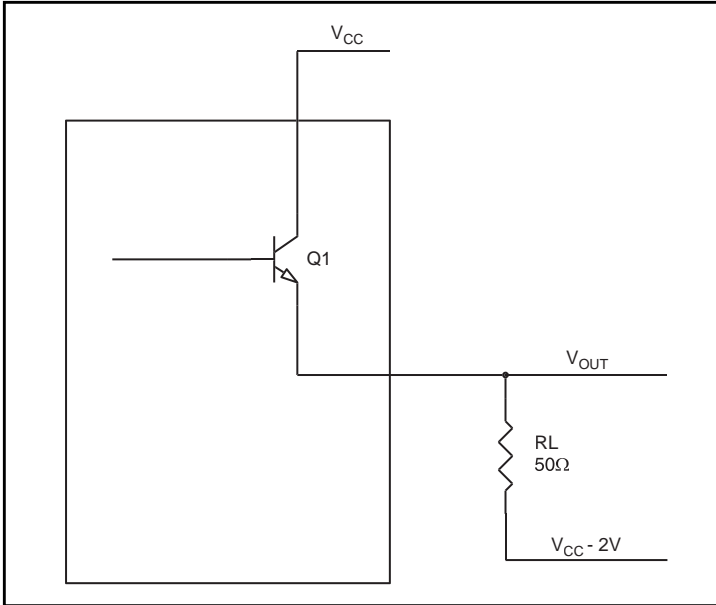


Figure 7. LVPECL Driver Circuit and Termination

To calculate power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$. These are typical calculations.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.8V$
 $(V_{CC_MAX} - V_{OH_MAX}) = 0.8V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.4V$
 $(V_{CC_MAX} - V_{OL_MAX}) = 1.4V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.4V)/50\Omega] * 1.4V = \mathbf{16.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{36mW}$$

Case Temperature Considerations

The IDT8SLVP2102I supports applications in a natural convection environment that does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, Ψ_{JB} , is calculated using the following equation:

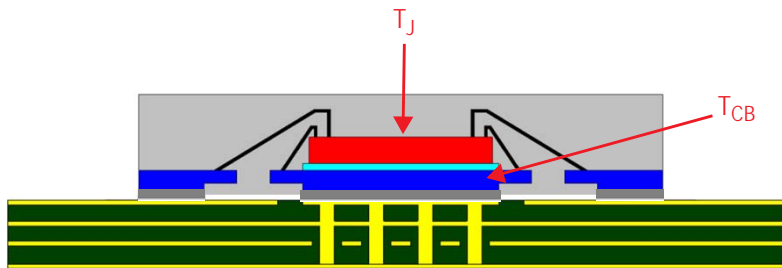
$T_J = T_{CB} + \Psi_{JB} \times P_d$, Where

T_J = Junction temperature at steady state condition in (°C).

T_{CB} = Case temperature (Bottom) at steady state condition in (°C).

Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

P_d = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_d$

Package type:	16-Lead VFQFPN
Body size:	3mm x 3mm x0.9mm
ePad size:	1.7mm x 1.7mm
Thermal Via:	2 x 2 matrix
Ψ_{JB}	5.1 C/W
T_{CB}	105°C
P_d	0.338 W

For the variables above, the junction temperature is equal to 107°C. Since this is below the maximum junction temperature of 125°C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 110.2°C, this device can function without the degradation of the specified AC or DC parameters.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16-Lead VFQFPN

θ_{JA} at 0 Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for the 8SLVP2102 is: 261

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-n1nlg16p2

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVP2102ANLGI	202AI	“Lead-Free” 16-Lead VFQFPN	Tube	-40°C to 85°C
8SLVP2102ANLGI8	202AI	“Lead-Free” 16-Lead VFQFPN	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to 85°C
8SLVP2102ANLGI/W	202AI	“Lead-Free” 16-Lead VFQFPN	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to 85°C

Table 8. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History

Date	Description of Change
March 13, 2018	Updated the package outline drawings; however, no technical changes Completed other minor changes
August 21, 2017	Added a feature about case temperature to Features Added Case Temperature Considerations Updated the Package Outline Drawings. No mechanical changes.
February 26, 2014	Ordering Info: Changed Tray to Tube.
January 28, 2014	Changed Note 6 to read "V _{IL} should not be less than -0.3V. V _{IH} should not be higher than V _{CC} ."
January 30, 2013	Added Features Bullet: Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can also accept single-ended LVCMOS levels. Added NOTE 8 to V _{PP} , V _{CMR} . Updated the "Wiring the Differential Input to Accept Single-Ended Levels" note.
July 31, 2012	Ordering Information Table - added additional row. Added Orientation Packaging Table.
June 20, 2012	Power Supply DC Characteristics Tables - changed I _{CC} to 180mA. Added "±1" to test conditions (PCN #651).