# HS-4080AEH

Radiation Hardened Full Bridge N-Channel FET Driver

The HS-4080AEH is a monolithic, high frequency, medium voltage Full Bridge N-Channel FET Driver IC. The device includes a TTL-level input comparator, which can be used to facilitate the “hysteresis” and PWM modes of operation. Its HEN (High Enable) lead can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. The HS-4080AEH is well suited for use in distributed DC power supplies and DC/DC converters, since it can switch at high frequencies.

This device can also drive medium voltage motors and two HS-4080AEHs can be used to drive high performance stepper motors, since the short minimum “on-time” can provide fine micro-stepping capability.

Short propagation delays maximize control loop crossover frequencies and dead times, which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

Constructed with the Renesas dielectrically isolated radiation hardened Silicon Gate (RSG) process, this device is immune to single event latch-up and has been specifically designed to provide highly reliable performance in harsh radiation environments. Complete your design with radiation hardened MOSFETs from Renesas.

## Features

- Electrically screened to SMD # 5962-99617
- QML qualified per MIL-PRF-38535 requirements
- TID Rad Hard Assurance (RHA) testing
  - HDR (50 - 300 rad(Si)/s). . . . . 300krad(Si) (max)
  - HDR (0.01 rad(Si)/s) . . . . . .50krad(Si)
- Latch-up immune RSG DI process
- Drives N-Channel FET full bridge including high-side chop capability
- Bootstrap supply max voltage to $95V_{DC}$
- TTL comparator input levels
- Drives 1000pF load with rise and fall times of 50ns
- User-programmable dead time
- Charge-pump and bootstrap maintain upper bias supplies
- DIS (Disable) pin pulls gates low
- Operates from single supply. . . . . 12V to 15V
- Low power consumption
- Undervoltage protection

## Applications

- Full bridge power supplies
- PWM motion control

## Application Block Diagram

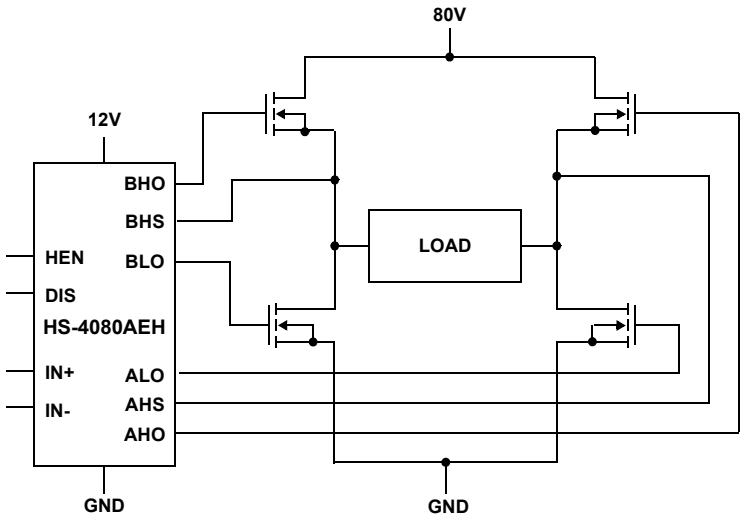



FIGURE 1. APPLICATION BLOCK DIAGRAM

# Ordering Information

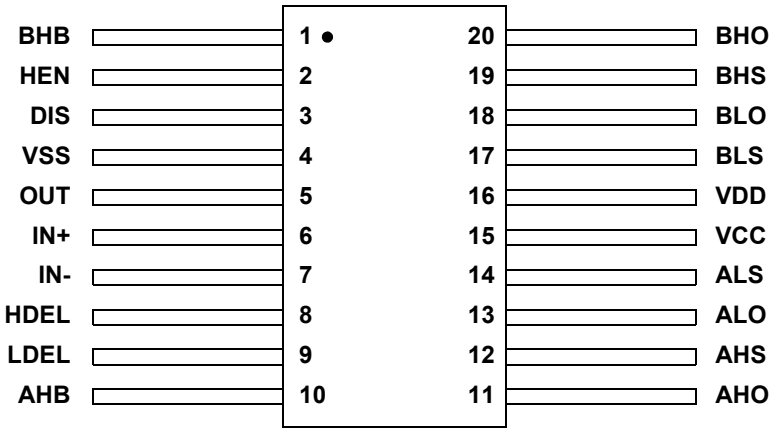
| ORDERING SMD NUMBER (Note 2) | PART NUMBER (Notes 1) | RADIATION HARDNESS (Total Ionizing Dose) | PACKAGE DESCRIPTION (RoHS Compliant) | PKG. DWG. # | TEMPERATURE RANGE |
|---|---|---|---|---|---|
| 5962F9961702V9A(Note 3) | HS0-4080AEH-Q | HDR to 300krad(Si), LDR to 50krad(Si) | DIE | - | -55 to +125°C |
| 5962F9961702VXC | HS9-4080AEH-Q | | 20 Ld Flatpack | K20.A | |
| HS0-4080AEH/SAMPLE (Notes 3, 4) | HS0-4080AEH/SAMPLE | N/A | DIE | - | |
| HS9-4080AEH/PROTO (Note 4) | HS9-4080AEH/PROTO | N/A | 20 Ld Flatpack | K20.A | |

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

# Pin Configuration

HS-4080AEH
(FLATPACK, CDFP4-F20)
TOP VIEW



# Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | BHB | B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 50µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 15V. |
| 2 | HEN | High-side Enable input. Logic level input that when low overrides IN+/IN- (Pins 6 and 7) to put AHO and BHO drivers (Pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pin can be driven by signal levels of 0V to 15V (no greater than VDD). An internal 100µA pull-up to VDD will hold HEN high, so no connection is required if high-side and low-side outputs are to be controlled by IN+/IN -inputs. |
| 3 | DIS | DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than VDD). An internal 100µA pull-up to VDD will hold DIS high if this pin is not driven. |
| 4 | VSS | Chip negative supply, generally will be ground. |
| 5 | OUT | OUTput of the input control comparator. This rail-to-rail output signal can be used for feedback and hysteresis. |
| 6 | IN+ | Noninverting input of control comparator. The input common-mode voltage range of this comparator is 1V to 4.5V. If IN+ is greater than IN- (Pin 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pin 3) high level will override IN+/IN- control for all outputs. HEN (Pin 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pins 8 and 9). |
| 7 | IN- | Inverting input of control comparator. The input common-mode voltage range of this comparator is 1V to 4.5V. See IN+ (Pin 6) description. |
| 8 | HDEL | High-side turn-on DELay. Connect resistor from this pin to VSS to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V. |
| 9 | LDEL | Low-side turn-on DELay. Connect resistor from this pin to VSS to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V. |
| 10 | AHB | A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 15V. |
| 11 | AHO | A High-side Output. Connect to gate of A High-side power MOSFET. |
| 12 | AHS | A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| 13 | ALO | A Low-side Output. Connect to gate of A Low-side power MOSFET. |
| 14 | ALS | A Low-side Source connection. Connect to source of A Low-side power MOSFET. |
| 15 | VCC | Positive supply to gate drivers. Must be same potential as VDD (Pin 16). Connect to anodes of two bootstrap diodes. |
| 16 | VDD | Positive supply to lower gate drivers. Must be same potential as VCC (Pin 15). De-couple this pin to VSS (Pin 4). |
| 17 | BLS | B Low-side Source connection. Connect to source of B Low-side power MOSFET. |
| 18 | BLO | B Low-side Output. Connect to gate of B Low-side power MOSFET. |
| 19 | BHS | B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| 20 | BHO | B High-side Output. Connect to gate of B High-side power MOSFET. |

## Typical Application (Hysteresis Mode Switching)

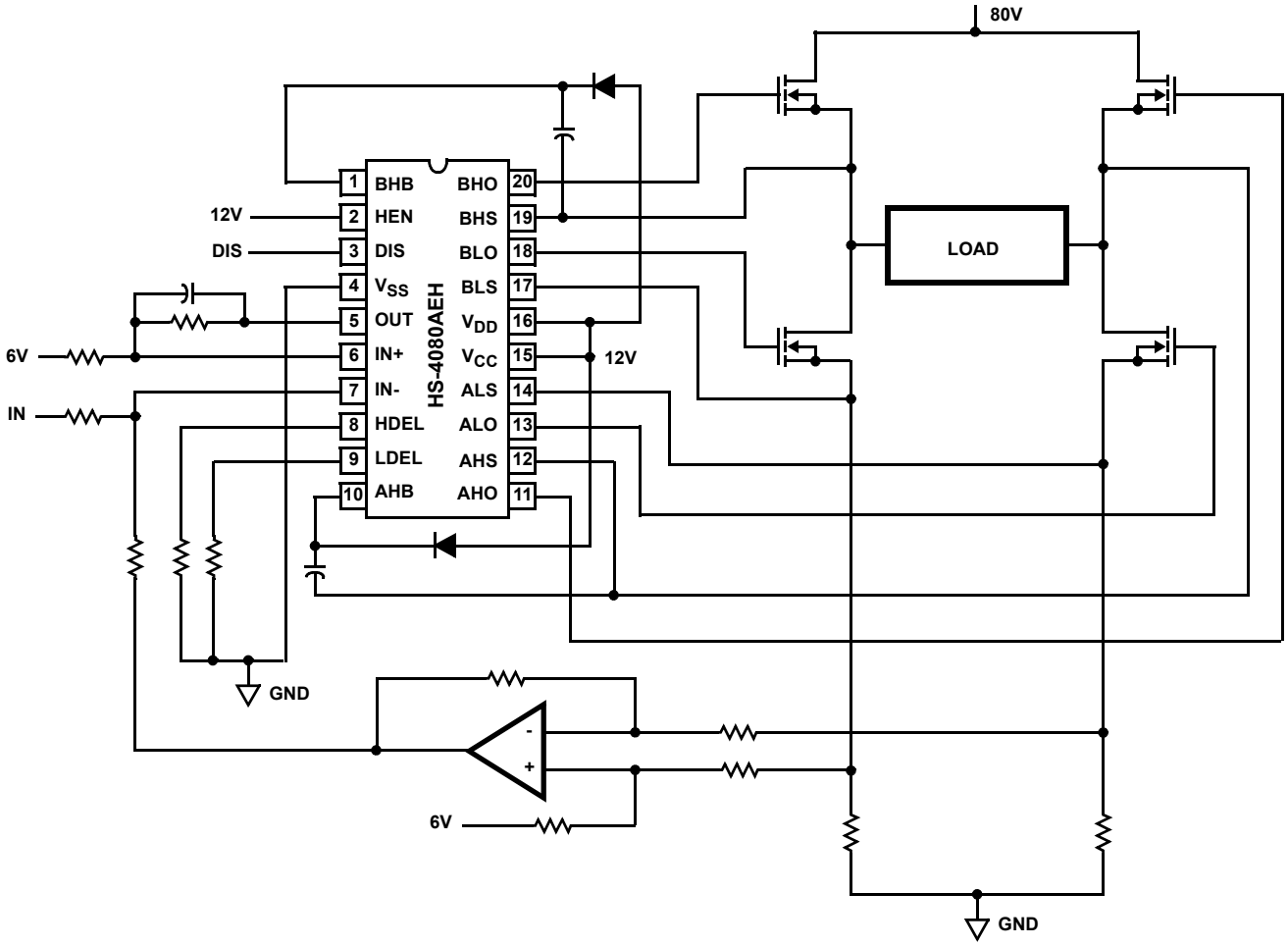



FIGURE 2. TYPICAL APPLICATION

# Die Characteristics

**DIE DIMENSIONS:**

4760µm x 5660mm (188 mils x 223 mils)
Thickness: 483mm ±25.4mm (19 mils ±1 mil)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: Phosphorus Silicon Glass
Thickness: 8.0kÅ ±1.0kÅ

**Top Metallization:**

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

**Substrate:**

Radiation Hardened Silicon Gate,
Dielectric Isolation

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential:**

Unbiased (DI)

**ADDITIONAL INFORMATION:**

**Worst Case Current Density:**

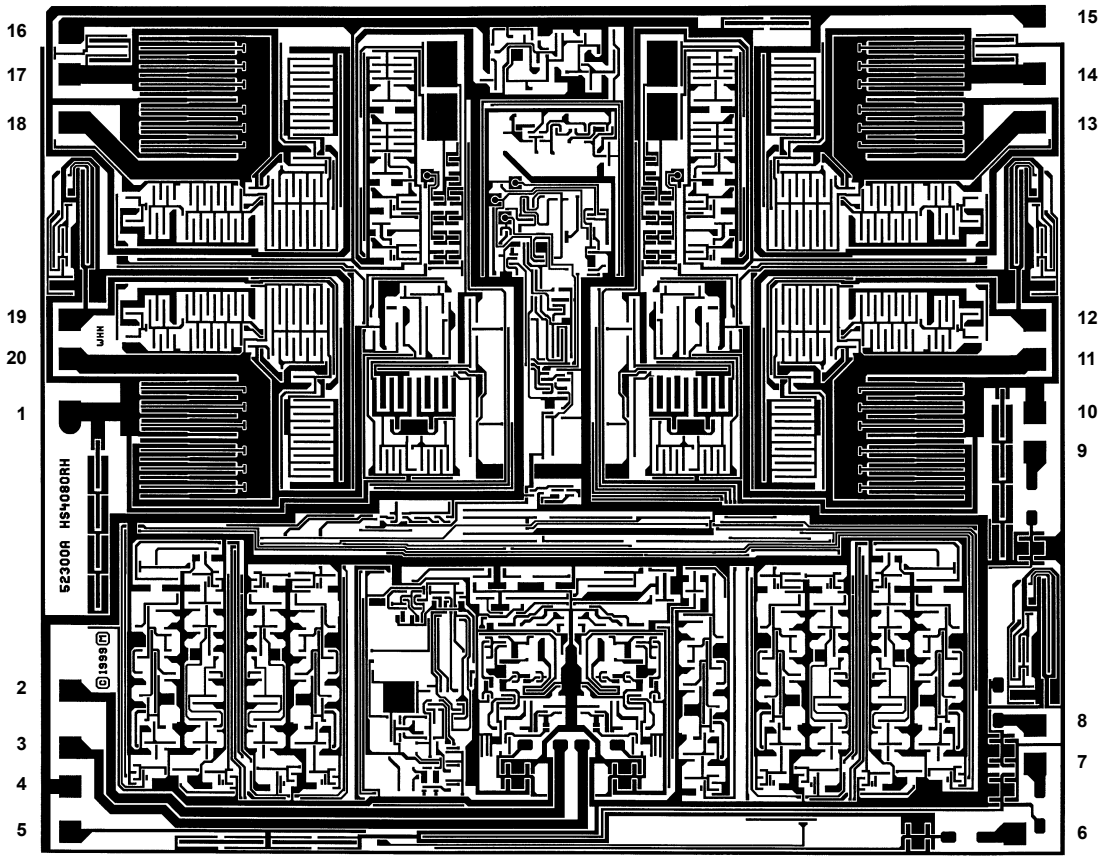
$< 2.0 \times 10^5$ A/cm$^2$

**Transistor Count:**

432

# Metallization Mask Layout

**HS-4080AEH**

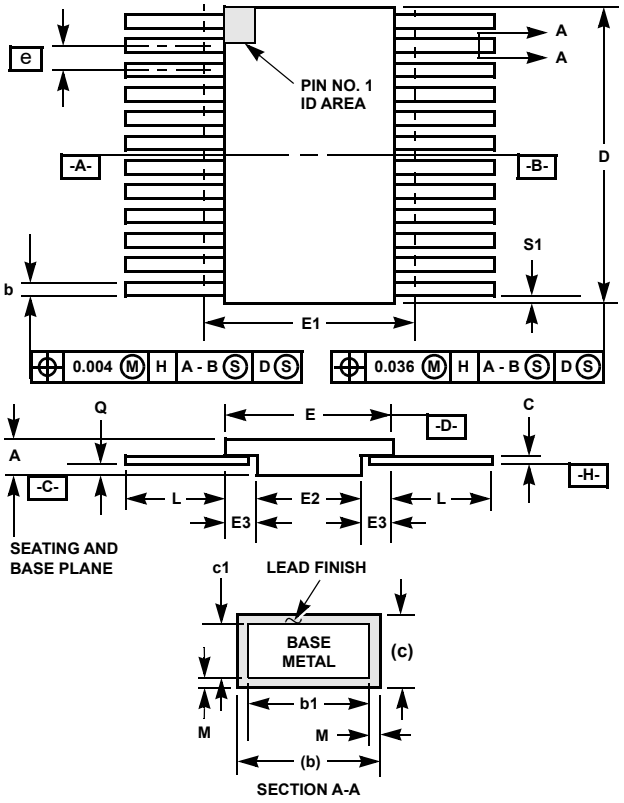


# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| Feb 7, 2024 | 7.00 | Updated Feature bullets.<br>Updated Ordering information table.<br>Updated Pin Descriptions for HEN, DIS, IN+, and IN-.<br>Removed About Intersil section. |
| May 27, 2015 | 6.00 | -Updated entire datasheet to Intersil new standard.<br>-Removed part number “HS-4080ARH’ throughout the document.<br>- Ordering information table on page 2: Added part numbers HS0-4080AEH/SAMPLE and HS9-4080AEH/PROTO.<br>-Added revision history and about Intersil verbiage. |

**For the most recent package outline drawing, see K20.A.**




## K20.A MIL-STD-1835 CDFP4-F20 (F-9A, CONFIGURATION B)
## 20 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.045 | 0.115 | 1.14 | 2.92 | - |
| b | 0.015 | 0.022 | 0.38 | 0.56 | - |
| b1 | 0.015 | 0.019 | 0.38 | 0.48 | - |
| c | 0.004 | 0.009 | 0.10 | 0.23 | - |
| c1 | 0.004 | 0.006 | 0.10 | 0.15 | - |
| D | - | 0.540 | - | 13.72 | 3 |
| E | 0.245 | 0.300 | 6.22 | 7.62 | - |
| E1 | - | 0.330 | - | 8.38 | 3 |
| E2 | 0.130 | - | 3.30 | - | - |
| E3 | 0.030 | - | 0.76 | - | 7 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| k | 0.008 | 0.015 | 0.20 | 0.38 | 2 |
| L | 0.250 | 0.370 | 6.35 | 9.40 | - |
| Q | 0.026 | 0.045 | 0.66 | 1.14 | 8 |
| S1 | 0.00 | - | 0.00 | - | 6 |
| M | - | 0.0015 | - | 0.04 | - |
| N | 20 | | 20 | | - |

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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