HI-390

Dual SPDT CMOS Analog Switch

NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

DATASHEET

FN4754
Rev 1.00
August 2002

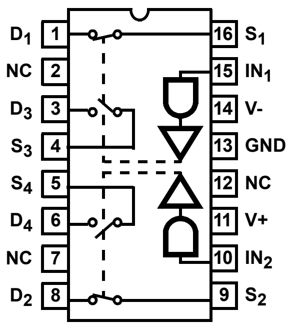
The HI-390 switch is a monolithic device fabricated using CMOS technology and the Intersil dielectric isolation process. This device is TTL compatible and features low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1-0390-2	-55 to 125	16 Ld CERDIP	F16.3

Pinout Switch States shown for a Logic "1" Input

HI-390 (CERDIP)
TOP VIEW



LOGIC	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

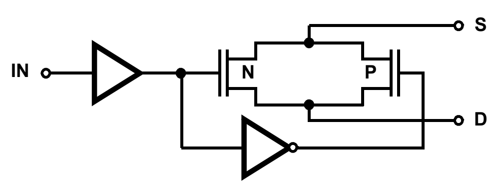
Features

- Analog Signal Range (±15V Supplies) . . . . ±15V
- Low Leakage 40pA
- Low On Resistance 35Ω
- Break-Before-Make Delay 60ns
- Charge Injection 30pC
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power. 1.0mW

Applications

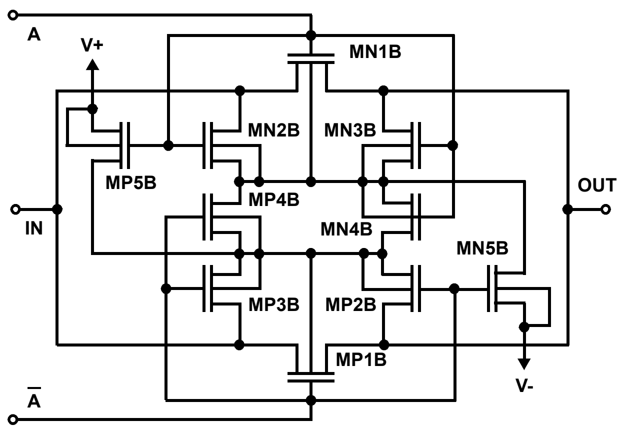
- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram

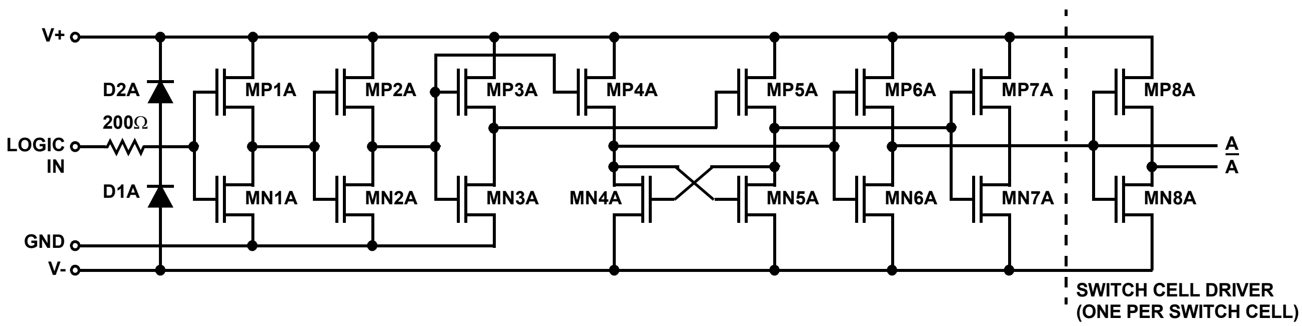


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies (V+ to V-) 44V
Digital Input Voltage . . . . (V+) +4V to (V-) -4V
Analog Input Voltage . . . . (V+) +1.5V to (V-) -1.5V

Operating Conditions

Temperature Ranges
HI-390-2 . . . . -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package.	75	20

Maximum Junction Temperature
Hermetic Package . . . . 175°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic “1” = 4V, for Logic “0” = 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switch ON Time, t_{ON}		25	-	210	300	ns
Switch OFF Time, t_{OFF}		25	-	160	250	ns
Break-Before-Make Delay, t_{OPEN}		25	-	60	-	ns
Charge Injection Voltage, ΔV	(Note 7)	25	-	3	-	mV
OFF Isolation	(Note 6)	25	-	60	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		25	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		25	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$		25	-	35	-	pF
Digital Input Capacitance, C_{IN}		25	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Low Level, V_{INL}		Full	-	-	0.8	V
Input High Level, V_{INH}		Full	4	-	-	V
Input Leakage Current (Low), I_{INL}	(Note 5)	Full	-	-	1	µA
Input Leakage Current (High), I_{INH}	(Note 5)	Full	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range		Full	-15	-	+15	V
ON Resistance, r_{ON}	(Note 2)	25	-	35	50	Ω
		Full	-	40	75	Ω
OFF Input Leakage Current, $I_{S(OFF)}$	(Note 3)	25	-	0.04	1	nA
		Full	-	1	100	nA
OFF Output Leakage Current, $I_{D(OFF)}$	(Note 3)	25	-	0.04	1	nA
		Full	-	1	100	nA
ON Input Leakage Current, $I_{S(ON)}$	(Note 4)	25	-	0.03	1	nA
		Full	-	0.5	100	nA

Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. V_{IN} for Logic “1” = 4V, for Logic “0” = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Current, I+	(Note 8)	25	-	0.09	0.5	mA
		Full	-	-	1	mA
Current, I-	(Note 8)	25	-	0.01	10	µA
		Full	-	-	100	µA
Current, I+	(Note 9)	25	-	0.01	10	µA
		Full	-	-	100	µA
Current, I-	(Note 9)	25	-	0.01	10	µA
		Full	-	-	100	µA

NOTES:

2. $V_S = \pm10V$, $I_{OUT} = \mp10mA$. On resistance derived from the voltage measured across the switch under these conditions.
3. $V_S = \pm14V$, $V_D = \mp14V$.
4. $V_S = V_D = \pm14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K, $C_L = C_{FIXTURE} + C_{PROBE}$, OFF Isolation = 20 Log V_S/V_D.
7. V_S = 0V, C_L = 10nF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged. Charge Injection = Q = $C_L \times \Delta V$.
8. V_{IN} = 4V (one input, all other inputs = 0V).
9. V_{IN} = 0.8V (all inputs).

Test Circuits and Waveforms

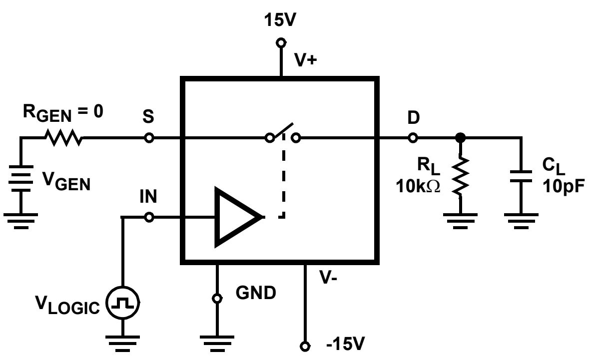


FIGURE 1A. TEST CIRCUIT

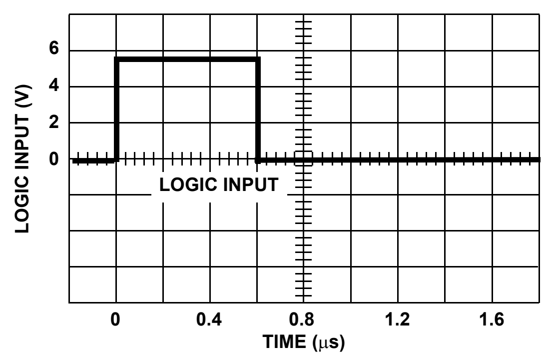


FIGURE 1B. LOGIC INPUT

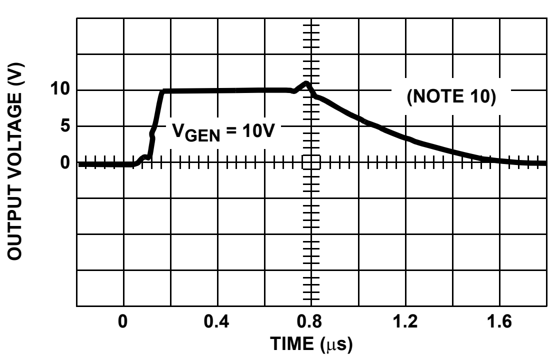


FIGURE 1C. V_{ANALOG} = 10V

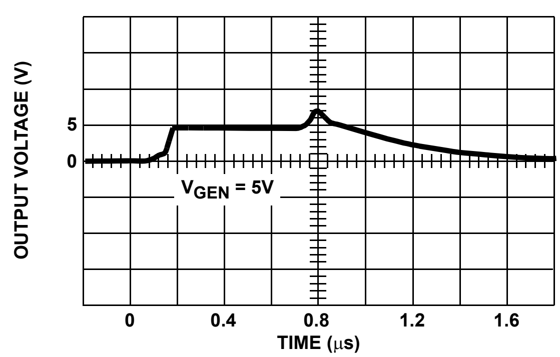


FIGURE 1D. V_{ANALOG} = 5V

Test Circuits and Waveforms (Continued)

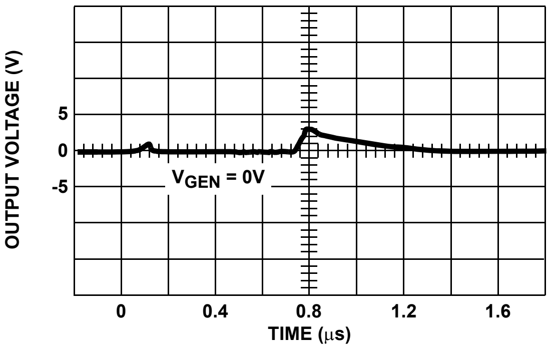


FIGURE 1E. V_{ANALOG} = 0V

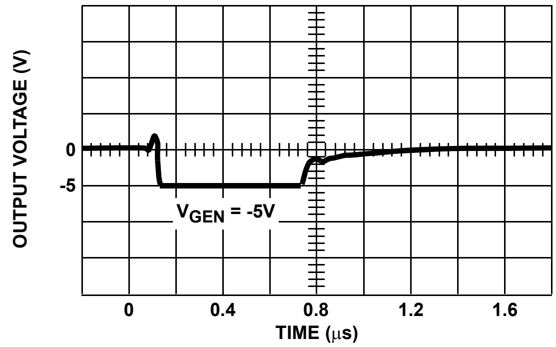


FIGURE 1F. V_{ANALOG} = -5V

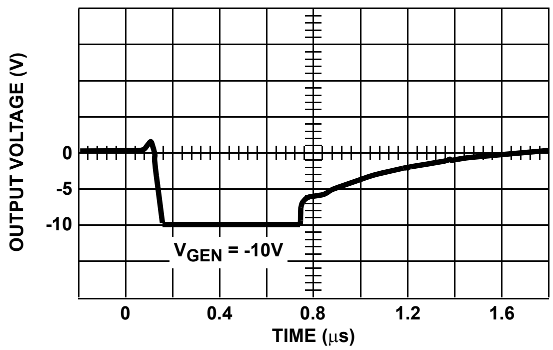


FIGURE 1G. V_{ANALOG} = -10V

NOTE:

10. If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 1. SWITCHING WAVEFORMS FOR VARIOUS ANALOG INPUT VOLTAGES

Typical Performance Curves

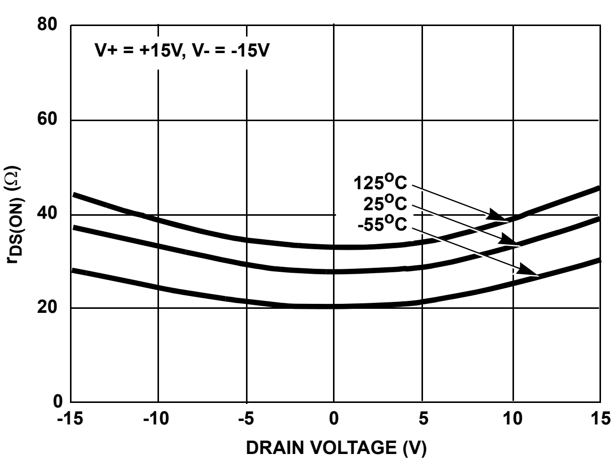


FIGURE 2. $r_{DS(ON)}$ vs V_D

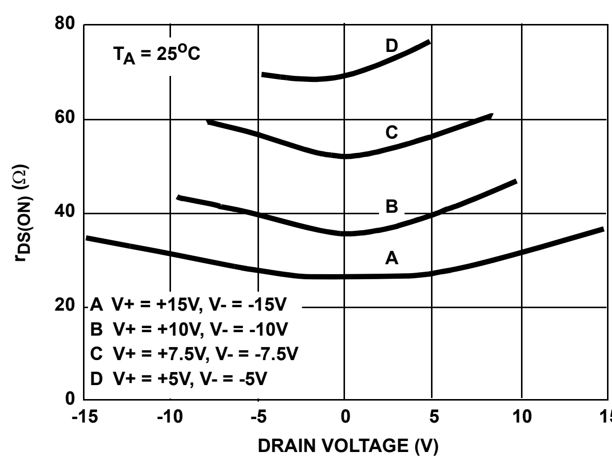


FIGURE 3. $r_{DS(ON)}$ vs V_D

Typical Performance Curves (Continued)

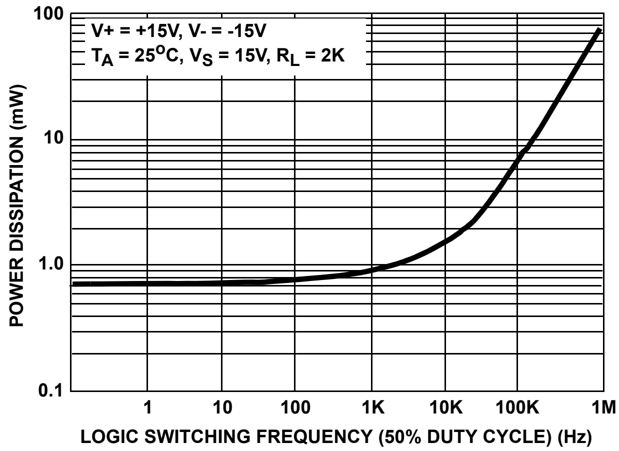


FIGURE 4. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

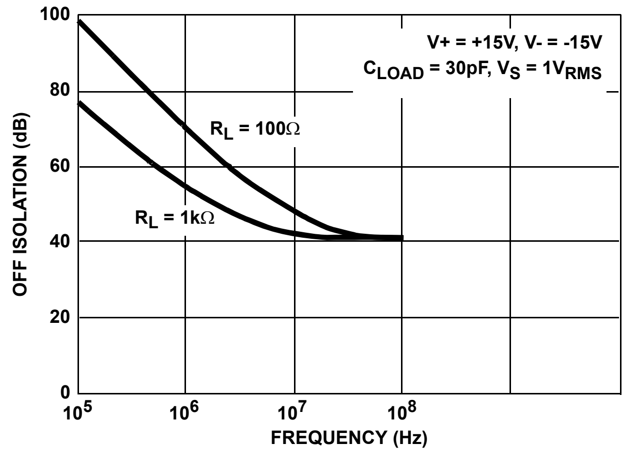


FIGURE 5. OFF ISOLATION vs FREQUENCY

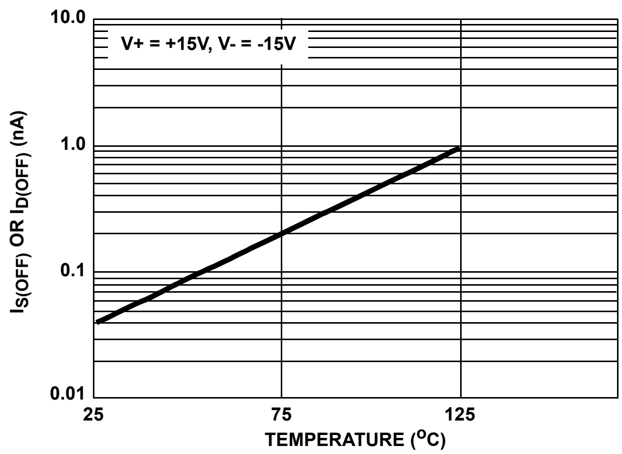


FIGURE 6. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE (NOTE 11)

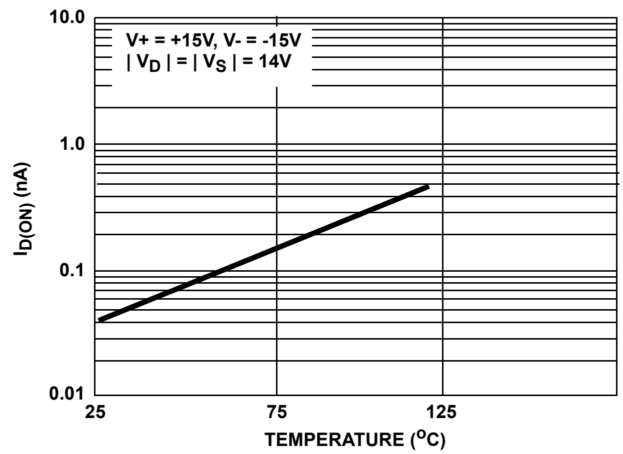


FIGURE 7. $I_{D(ON)}$ vs TEMPERATURE (NOTE 11)

NOTE:

11. The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

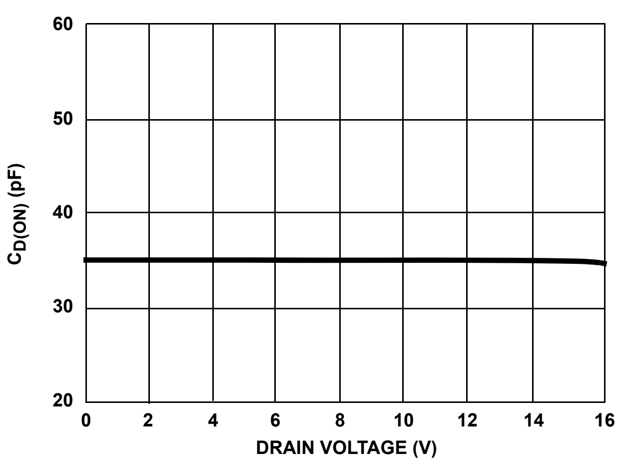


FIGURE 8. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

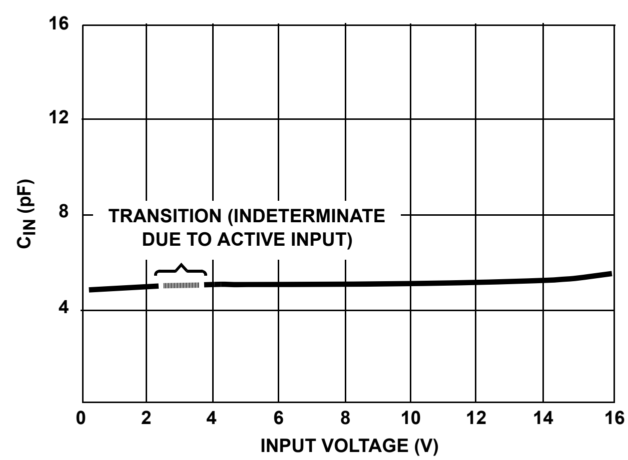


FIGURE 9. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

Typical Performance Curves (Continued)

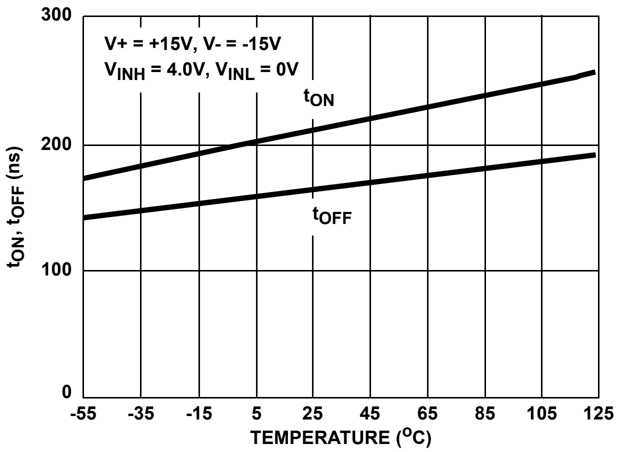


FIGURE 10. SWITCHING TIME vs TEMPERATURE

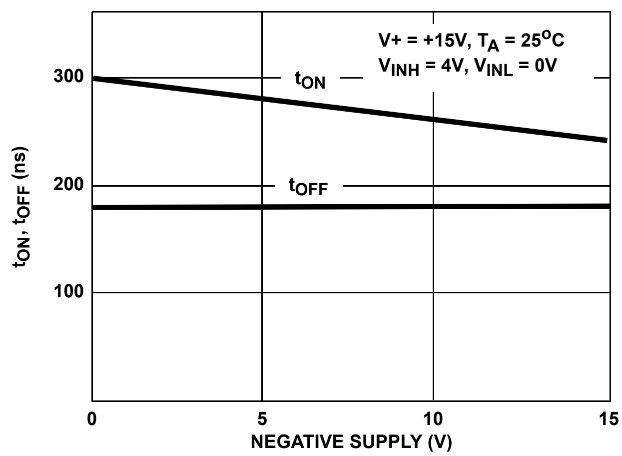


FIGURE 11. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

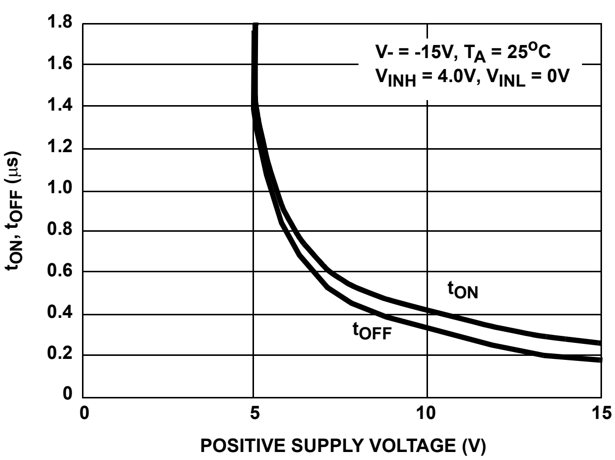


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

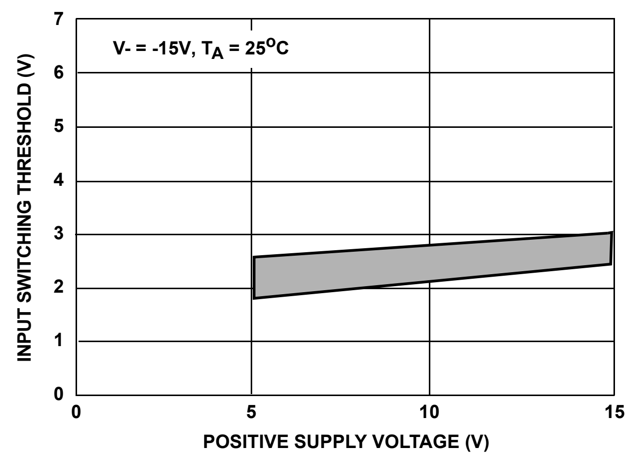
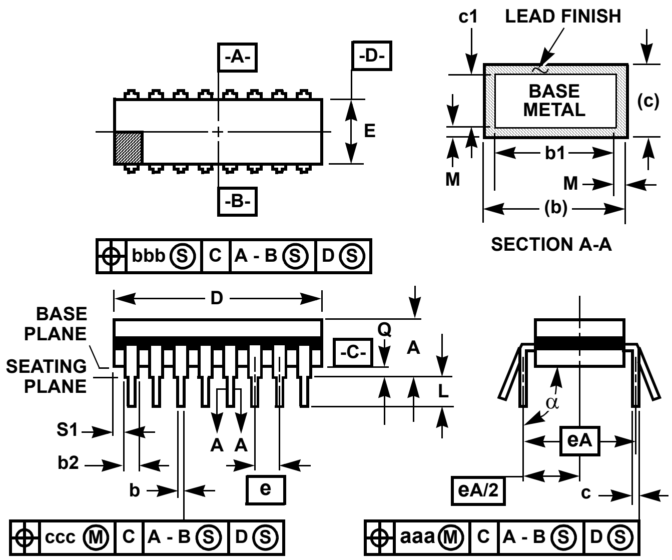


FIGURE 13. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.