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April 1st, 2010 Renesas Electronics Corporation

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HD74LVCZ16245A

16-bit Bidirectional Transceivers with 3-state Outputs

REJ03D0375-0200 (Previous ADE-205-233 (Z)) Rev.2.00 Aug. 20.2004

Description

The HD74LVCZ16245A has sixteen two direction buffers, for the fittest at two direction bus lines with three state outputs in a 48 pin package. When (DIR) is high, data flows from the A inputs to the B outputs, and when (DIR) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input (\overline{G}) high level.

When V_{CC} is between 0 and 1.5 V, the device is in the high impedance state during power up or power down.

Low voltage and high-speed operation is suitable at battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.7 \text{ to } 5.5 \text{ V}$
- All inputs V_{IH} (Max) = 5.5 V (@ V_{CC} = 0 to 5.5 V)
- All inputs / outputs $V_{I/O}$ (Max) = 5.5 V (@ V_{CC} = 0 V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@ V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@ V_{CC} = 3.3 V, Ta = 25°C)
- High impedance state during power up and power down
- Power off disables outputs, permitting live insertion
- High output current ± 24 mA (@V_{CC} = 3.0 to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVCZ16245ATEL	TSSOP-48 pin	TTP-48DBV	Т	EL (1,000 pcs/reel)

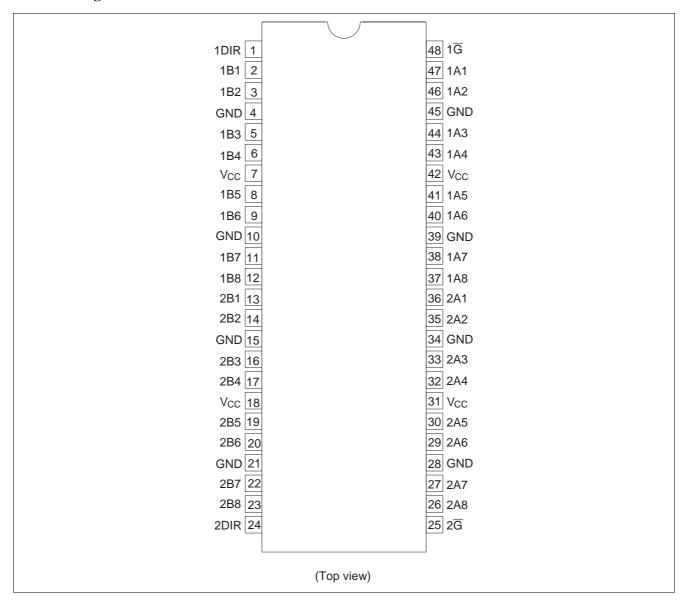
Function Table

Inputs

<u>G</u>	DIR	Operation
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Z

- H: High level
- L: Low level
- X: Immaterial
- Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.5 to 7.0	V	
Input voltage	VI	-0.5 to 7.0	V	
Input / output voltage	V _{I/O}	-0.5 to 7.0	V	Output "Z" or V _{CC} : OFF
		-0.5 to V _{CC} +0.5	 "	Output "H" or "L"
Input diode current	I _{IK}	-50	mA	V ₁ < 0
Output diode current	l _{ok}	-50	mA	V _O < 0
Output current	Io	±50	mA	
V _{CC} , GND current	I _{CC} or I _{GND}	±100	mA	
Storage temperature	Tstg	-65 to 150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

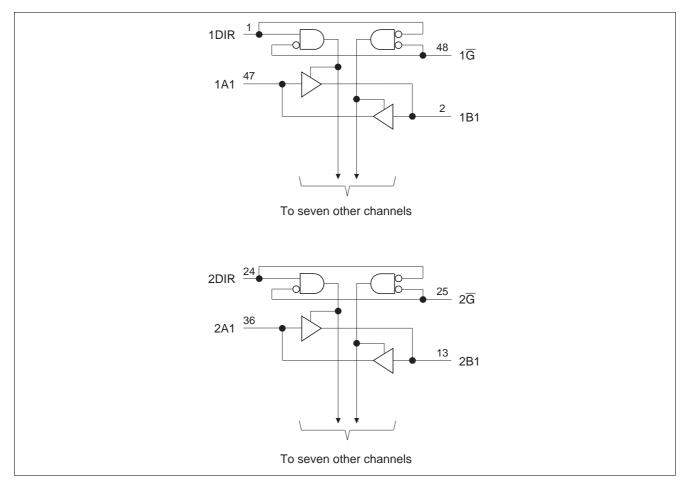
HD74LVCZ16245A

Recommended Operating Conditions

Symbol	Ratings	Unit	Conditions
V_{CC}	2.7 to 5.5	V	At operation
VI	0 to 5.5	V	
V _{I/O}	0 to 5.5	V	Output "Z" or V _{CC} : OFF
	0 to V _{CC}		Output "H" or "L"
I _{OH}	-12	mA	V _{CC} = 2.7 V
	-24 ^{*1}		$V_{CC} = 3.0 \text{ to } 5.5 \text{ V}$
I _{OL}	12	mA	$V_{CC} = 2.7 \text{ V}$
	24 *1		$V_{CC} = 3.0 \text{ to } 5.5 \text{ V}$
t _r , t _f	0 to 6	ns / V	
Та	-40 to +85	°C	
	V _{CC} V _I V _{I/O} I _{OH} I _{OL}	$\begin{array}{c cccc} V_{CC} & 2.7 \text{ to } 5.5 \\ \hline V_{I} & 0 \text{ to } 5.5 \\ \hline V_{I/O} & 0 \text{ to } 5.5 \\ \hline 0 \text{ to } V_{CC} \\ \hline I_{OH} & -12 \\ \hline -24 & 1 \\ \hline I_{OL} & 12 \\ \hline 24 & 1 \\ \hline t_{r}, t_{f} & 0 \text{ to } 6 \\ \hline \end{array}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

Note: 1. Duty cycle ≤ 50%

Logic Diagram



Electrical Characteristics

 $(Ta = -40 \text{ to } 85^{\circ}C)$

Item	Symbol	V _{CC} (V)	Min	Тур	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.7 to 3.6	2.0		_	V	
		4.5 to 5.5	V _{CC} ×0.7	_	_	_	
	V _{IL}	2.7 to 3.6	_	_	0.8	V	
		4.5 to 5.5	_	_	V _{CC} ×0.3		
Output voltage	V _{OH}	2.7 to 5.5	V _{CC} -0.2	_	_	V	I _{OH} = -100 μA
		2.7	2.2	_	_		I _{OH} = -12 mA
		3.0	2.4	_	_		
		3.0	2.2	_	_		I _{OH} = -24 mA
		4.5	3.8	_	_		
	V _{OL}	2.7 to 5.5	_	_	0.2	V	I _{OL} = 100 μA
		2.7	_	_	0.4		I _{OL} = 12 mA
		3.0	_	_	0.55		I _{OL} = 24 mA
		4.5	_	_	0.55		
Input current	I _{IN}	0 to 5.5	_	_	±5	μΑ	V _{IN} = 0 to 5.5 V
Off state output	l _{OZ}	2.7 to 5.5	_	_	±5	μΑ	$V_{OUT} = 0$ to 5.5 V
current	I _{OZPU}	0 to 1.5	_	_	±5		$V_{OUT} = 0.5 \text{ to } 5.5 \text{ V},$
	I _{OZPD}	1.5 to 0	_	_	±5	<u> </u>	Output enable = don't care
Output leak current	I _{OFF}	0	_	_	±5	μΑ	V_{IN} or $V_O = 5.5 \text{ V}$
Quiescent supply	Icc	2.7 to 3.6	_	_	225	μΑ	$V_{IN} = 3.6 \text{ to } 5.5 \text{ V}^{*1}, I_{O} = 0$
current		2.7 to 5.5	_	_	350	<u> </u>	$V_{IN} = V_{CC}$ or GND
	ΔI_{CC}	2.7 to 3.6	_	_	500	μΑ	V_{IN} = one input at (V_{CC} -0.6) V ,
							other inputs at V _{CC} or GND
Input capacitance	C _{IN}	3.3	_	4.1	_	рF	V _{IN} = V _{CC} or GND
Input / output capacitance	C _{I/O}	3.3	_	9.2	_	pF	$V_{OUT} = V_{CC}$ or GND

Note: 1. This applies in the disabled state only.

Switching Characteristics

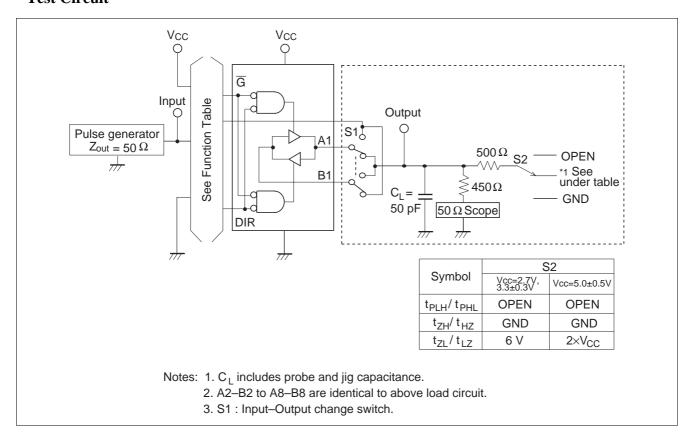
 $(Ta = -40 \text{ to } 85^{\circ}C)$

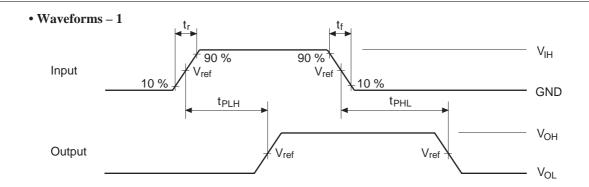
							FROM	то
Item	Symbol	V _{CC} (V)	Min	Тур	Max	Unit	(Input)	(Output)
Propagation delay time	t _{PLH}	2.7	_	_	5.2	ns	A or B	B or A
	t_{PHL}	3.3±0.3	1.0	_	4.6			
		5.0±0.5	_	_	4.0			
Output enable time	t_{ZH}	2.7	_	_	7.3	ns	G	A or B
	t_{ZL}	3.3±0.3	1.5	_	6.3			
		5.0±0.5	_	_	5.2			
Output disable time	t _{HZ}	2.7	_	_	7.5	ns	G	A or B
	t_{LZ}	3.3±0.3	1.5	_	6.9			
		5.0±0.5	_	_	6.0			
Between output pin skew *1	t _{OSLH}	2.7	_	_	_	ns		
	t_{OSHL}	3.3±0.3	_	_	1.0			
		5.0±0.5	_	_	1.0			

Note: 1. This parameter is characterized but not tested.

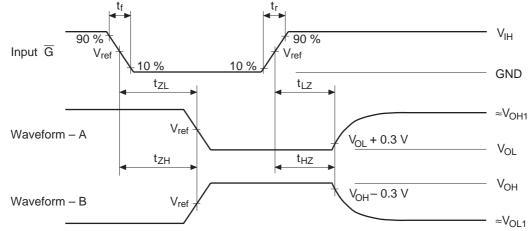
 $t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Test Circuit





• Waveforms – 2

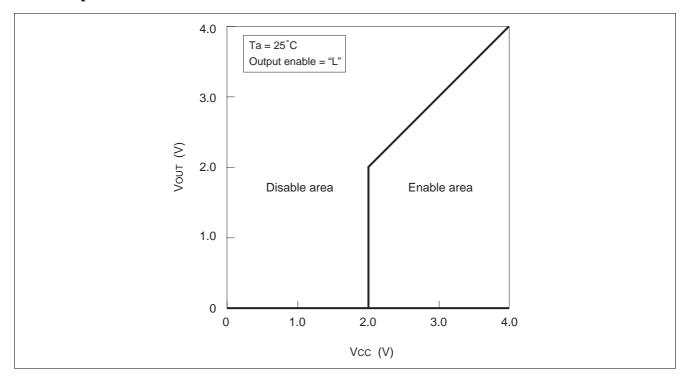


TEST	Vcc=2.7V, 3.3±0.3V	Vcc=5.0±0.5V
V_{IH}	2.7 V	V _{CC}
V_{ref}	1.5 V	50%V _{CC}
V_{OH1}	3 V	V _{CC}
V_{OL1}	GND	GND

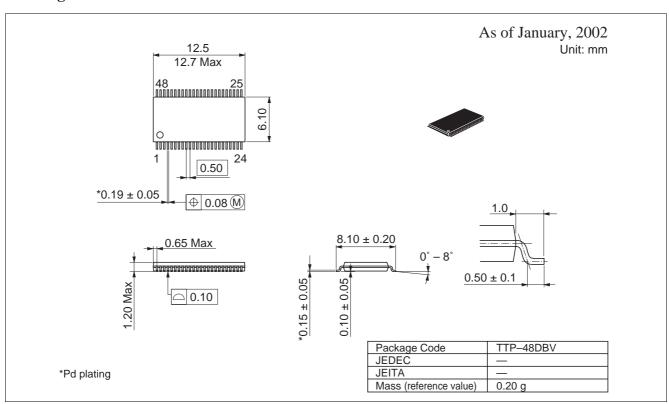
Notes: 1. Input waveform: PRR = 10 MHz, duty cycle 50%, t_r = 2.5 ns, t_f = 2.5 ns

- 2. Waveform A shows input conditions such that the output is "L" level when enabled by the output control.
- 3. Waveform B shows input conditions such that the output is "H" level when enabled by the output control.

Power up / down Characteristics



Package Dimensions



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