HA-4902/883

Precision Quad Comparator

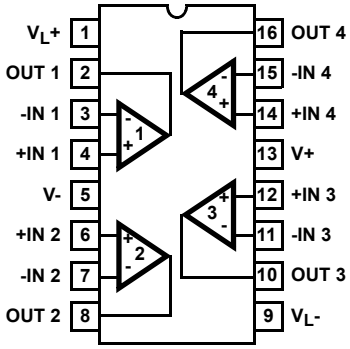
FN3929
Rev.1.00
May 3, 2012

The HA-4902/883 is a monolithic, quad, precision comparator offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. This comparator can sense signals at ground level while being operated from either a single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4902/883 contains a unique current driven output stage which can be connected to logic system supplies (V_{LOGIC}+ and V_{LOGIC}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4902/883 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

This comparators' combination of features make it an ideal component for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

Pin Configuration

HA-4902/883
(16 LD CERDIP)
TOP VIEW



Features

- This circuit is processed in accordance to MIL-STD-883 and is fully conformant under the provisions of Paragraph 1.2.1
- Fast Response Time (+25°C)
  - Maximum 215ns
  - Typical 180ns
- Low Offset Voltage (+25°C)
  - Maximum 5.0mV
  - Typical 2.0mV
- Low Input Sensitivity
  - Maximum 0.5mV
  - Typical 0.05mV
- Low Offset Current (+25°C)
  - Maximum 35nA
  - Typical 10nA
- Single or Dual Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit. No External Resistors Required

Applications

- Threshold Detector
- Zero Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
HA1-4902/883	HA1-4902/883	-55 to +125	16 Ld CERDIP	F16.3

Absolute Maximum Ratings

Voltage (Between V+ and V- Terminals) 35V
Differential Input Voltage . . . . . ±15V
Peak Output Current . . . . . ±50mA
Output Short Circuit Current Duration . . . . . Indefinite
(One Amplifier Shorted to GND)
ESD Rating . . . . . <2000V

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±15V
Logic Supply Voltage (V_L+) . . . . . +5V
Logic Reference Voltage (V_L-) 0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	76	17

Maximum Junction Temperature . . . . . +175°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Package Power Dissipation Limit at +75°C
CerDIP Package 1.31W
Package Power Dissipation Derating Factor Above +75°C
CerDIP Package . . . . . 13.1mW/°C
Lead Temperature (Soldering 10s) . . . . . +300°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L+ = 5V, V_L- = 0V, unless otherwise specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP (°C)	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V, V_{OUT} = 1.4V (See Note 4)	1	+25	-5	5	mV
			2, 3	+125, -55	-8	8	mV
Input Bias Current	$+I_B$	V_{CM} = 0V	1	+25	-150	150	nA
			2, 3	+125, -55	-200	200	nA
	$-I_B$	V_{CM} = 0V	1	+25	-150	150	nA
			2, 3	+125, -55	-200	200	nA
Input Offset Current	I_{IO}	V_{CM} = 0V	1	+25	-35	35	nA
			2, 3	+125, -55	-45	45	nA
Input Sensitivity	IN_{SEN}	(See Note 4)	1	+25	-0.5	0.5	mV
			2, 3	+125, -55	-0.6	0.6	mV
Output Voltage Levels	V_{OL}	I_{SINK} = 3mA	1	+25	-	0.4	V
			2, 3	+125, -55	-	0.4	V
	V_{OH}	I_{SOURCE} = 3mA	1	+25	3.5	-	V
			2, 3	+125, -55	3.5	-	V
Output Current	I_{SINK}	V_{OUT} ≤0.4V	1	+25	3	-	mA
			2, 3	+125, -55	3	-	mA
	I_{SOURCE}	V_{OUT} ≥3.5V	1	+25	-	-3	mA
			2, 3	+125, -55	-	-3	mA
Supply Current	$+I_{CC}$	V_{OUT} = V_{OL}, V_{OH}	1	+25	-	20	mA
			2, 3	+125, -55	-	20	mA
	$-I_{CC}$	V_{OUT} = V_{OL}, V_{OH}	1	+25	-	8	mA
			2, 3	+125, -55	-	10	mA
Logic Current	I_L	V_{OUT} = V_{OL}, V_{OH}	1	+25	-	6	mA
			2, 3	+125, -55	-	8	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally left blank. See A. C. Specifications on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, V_L+ = 5V, V_L- = 0V, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP (°C)	MIN	MAX	UNITS
Response Time	t_{pd0}	+100mV Input Step, +10mV Overdrive	2, 3	+25	-	200	ns
	t_{pd1}	-100mV Input Step, -10mV Overdrive	2, 3	+25	-	200	ns
Common Mode Range	+CMR		2	+25	-	12.4	V
	-CMR		2	+25	-15	-	V

NOTES:

2. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
3. F ≈ 100Hz, duty cycle ≈ 50%, inverting input driven, all unused inverting inputs tie to +5V.
4. Refer to enlarged area of test waveform A. Offset voltage is measured when V_{OUT} = 1.4V. Sensitivity is measured on the transition edge at 0.4V and 3.5V. Sensitivity is the change in differential input voltage required to change the output state. Sensitivity includes the effects of offset voltage, offset current, common mode rejection and voltage gain.

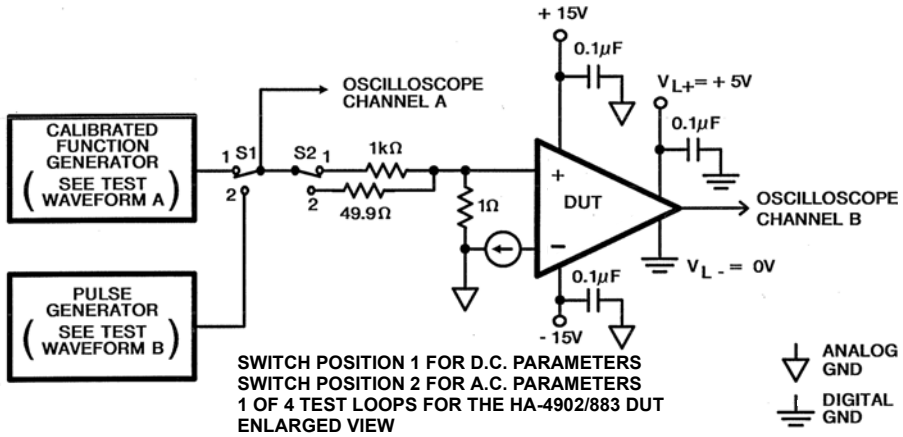
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 5), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

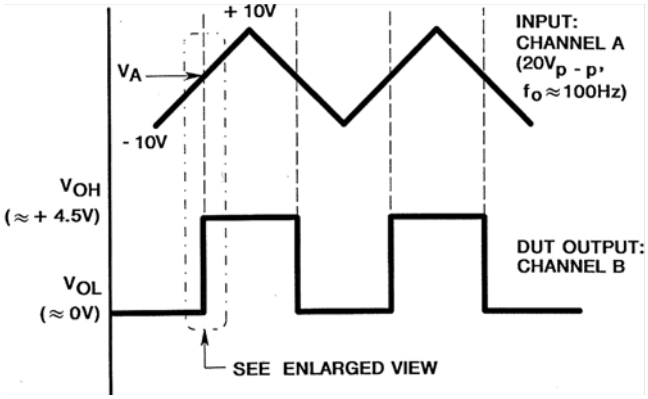
5. PDA applies to Subgroup 1 only.

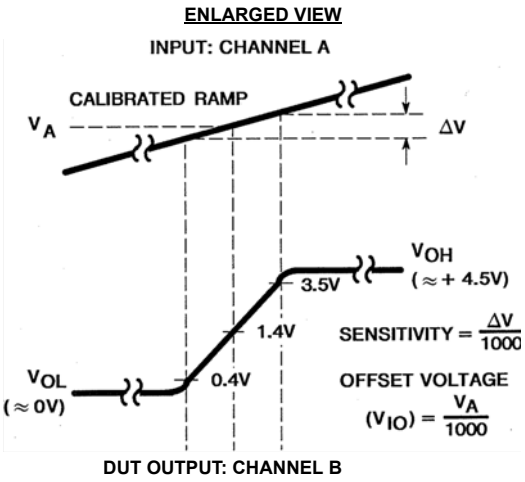
Test Circuit (Applies to Tables 1 and 2)



SWITCH POSITION 1 FOR D.C. PARAMETERS
SWITCH POSITION 2 FOR A.C. PARAMETERS
1 OF 4 TEST LOOPS FOR THE HA-4902/883 DUT
ENLARGED VIEW

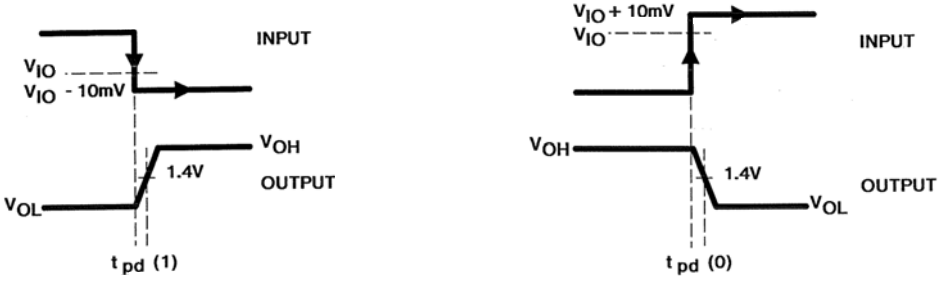
Test Waveform A (Applies to Table 1)





Test Waveform B (Applies to Table 3)

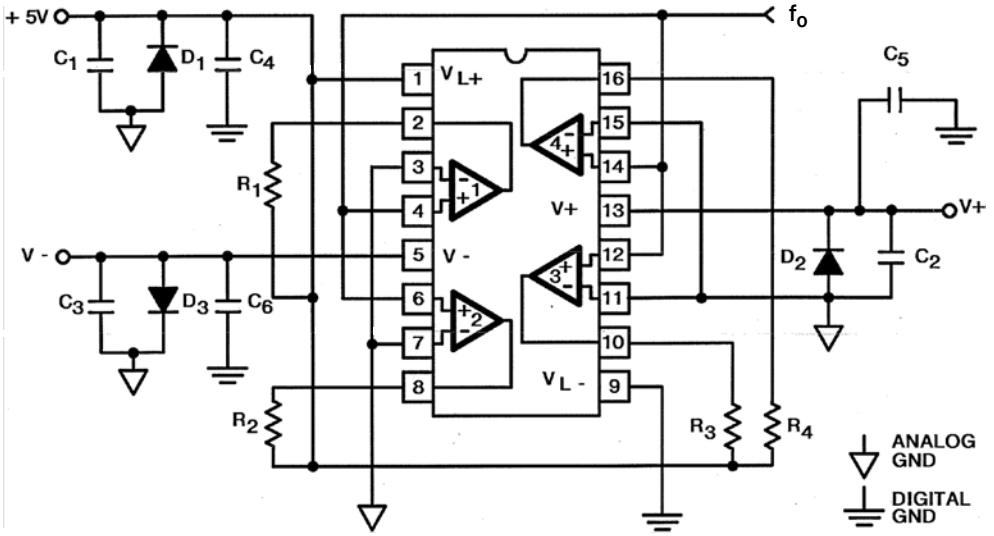
RESPONSE TIME



NOTE: Response time testing is done after V_{IO} testing to acquire the actual device offset voltage. 10mV overdrive is then added (or subtracted depending on state) to this measured V_{IO} value.

Burn-in Circuit

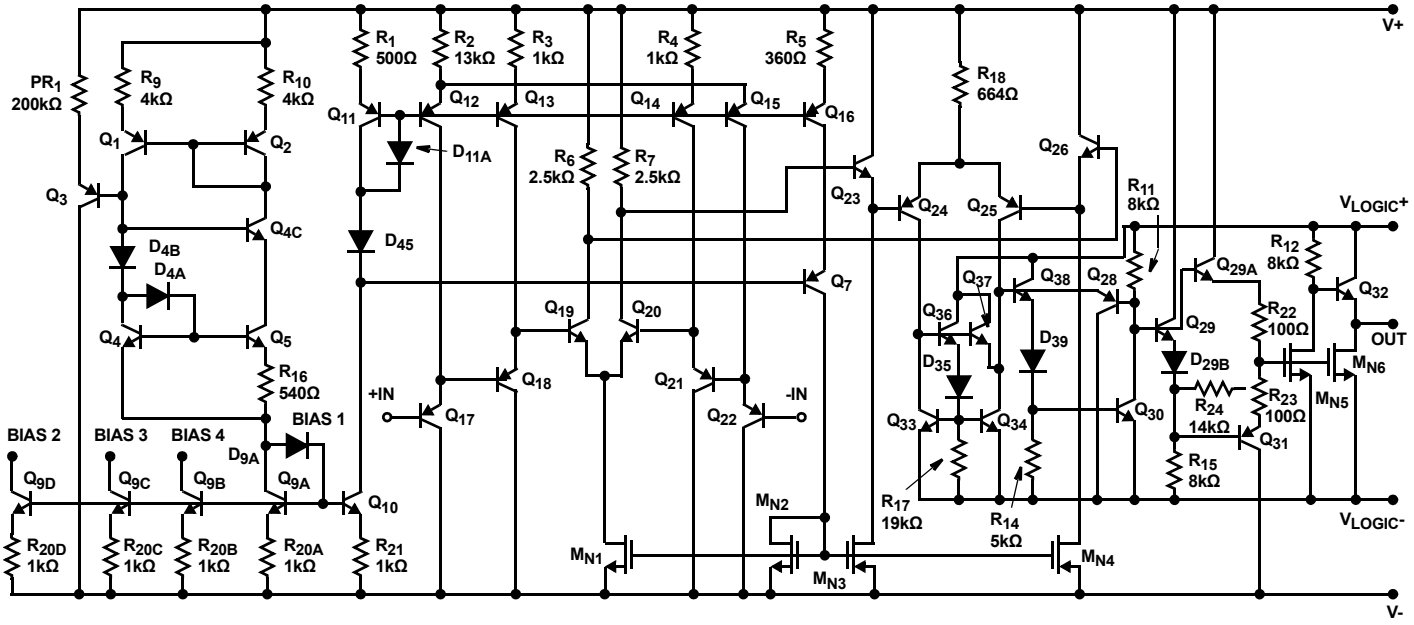
HA1-4902/883 CERAMIC DIP



NOTES:

R_1 = 5kΩ, ±5%
C_1, C_2, C_3 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
C_4, C_5, C_6 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
D_1, D_2, D_3 = 1N4002 or Equivalent/Board
| (V+) - (V-) | = 30V
V_L- = 0V, V_L+ = 0.5V
f_O = 5V (Static Burn-In)

Schematic Diagram (1/4 of HA-4902/883)



Die Characteristics

DIE DIMENSIONS:

90mils x 102mils x 20mils ± 1mil
2280µm x 2600µm x 508µm ± 25.4µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Nitride (Si3N4) over Silox (SiO2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:

$0.4 \times 10^5 A/cm^2$

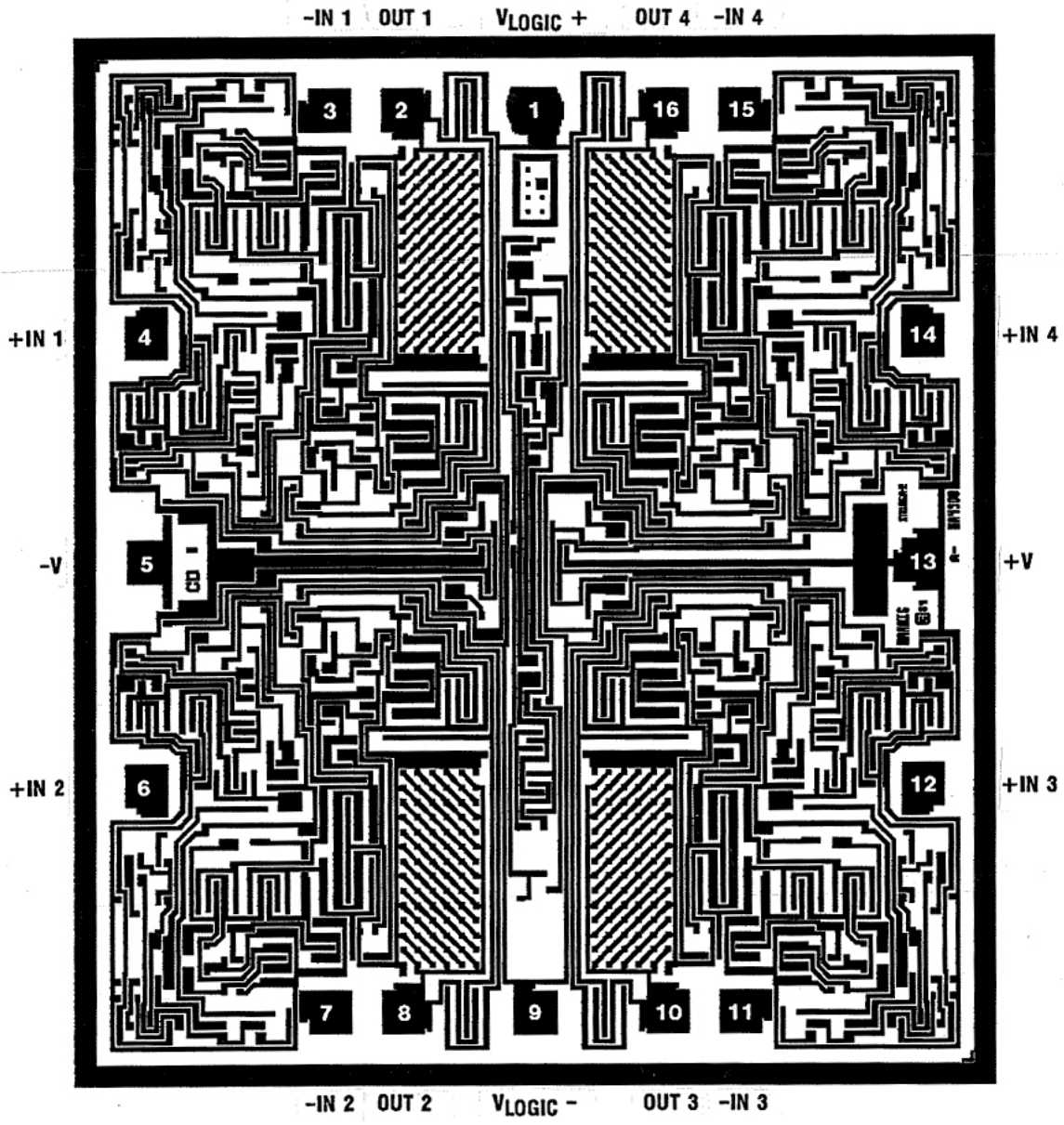
SUBSTRATE POTENTIAL (POWERED UP): V-

TRANSISTOR COUNT: 137

PROCESS: Bipolar and MOS Dielectric Isolation

Metallization Mask Layout

HA-4902/883



Design Information

The information contained in this section has been developed through characterization and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves

T_A = +25°C, V_S = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = 0V, Unless Otherwise Specified

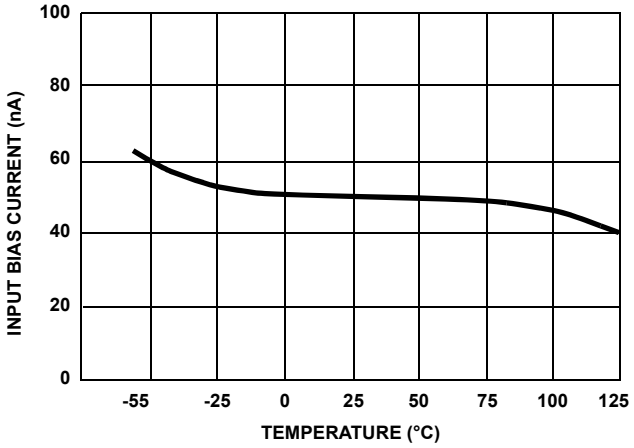


FIGURE 1. INPUT BIAS CURRENT vs TEMPERATURE

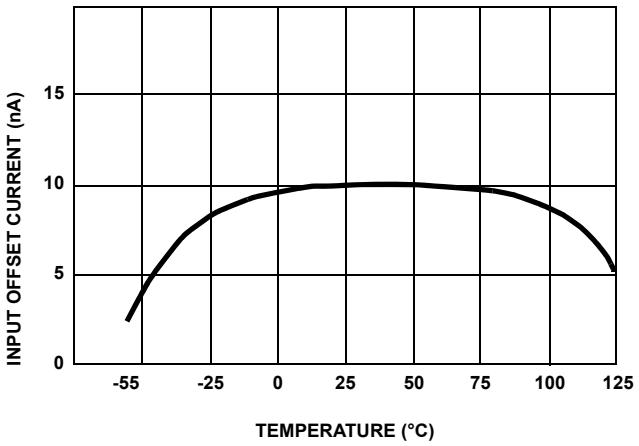


FIGURE 2. INPUT OFFSET CURRENT vs TEMPERATURE

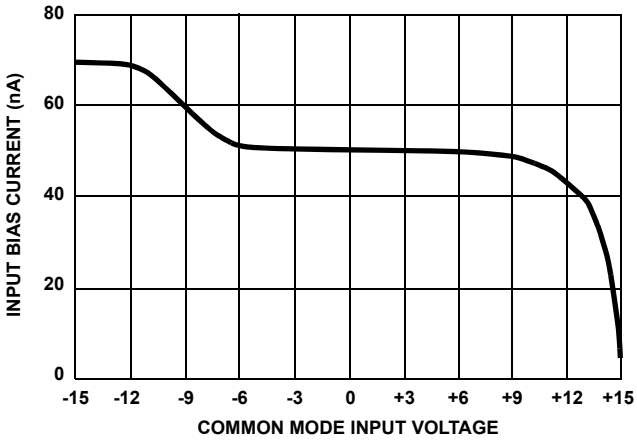


FIGURE 3. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE (V_{DIFF} = 0V)

Design Information (Continued)

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Typical Performance Curves $T_A = +25°C$, $V_S = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$, Unless Otherwise Specified (Continued)

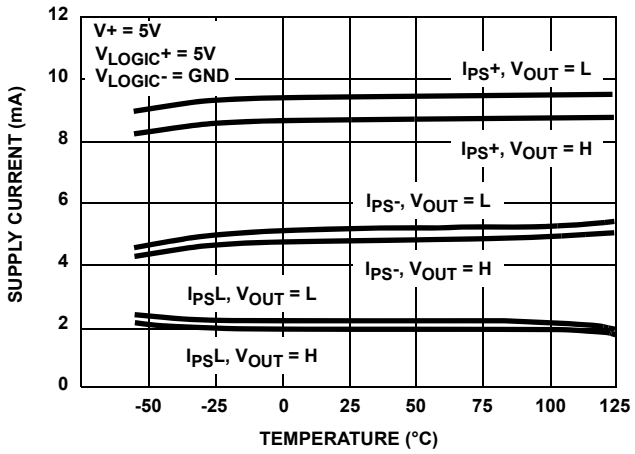

FIGURE 4. SUPPLY CURRENT vs TEMPERATURE (FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY)

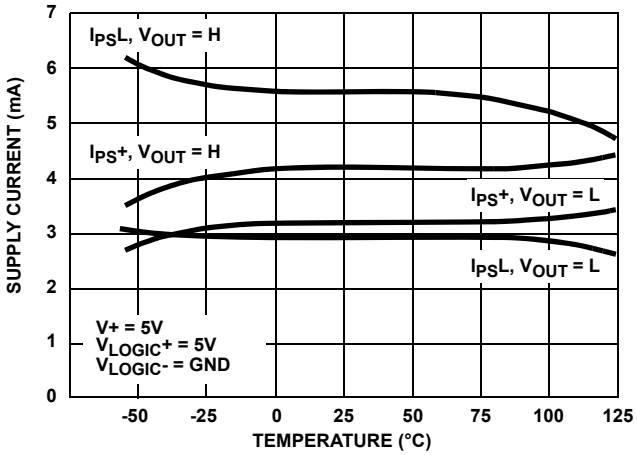

FIGURE 5. SUPPLY CURRENT vs TEMPERATURE (FOR SINGLE +5V OPERATION)

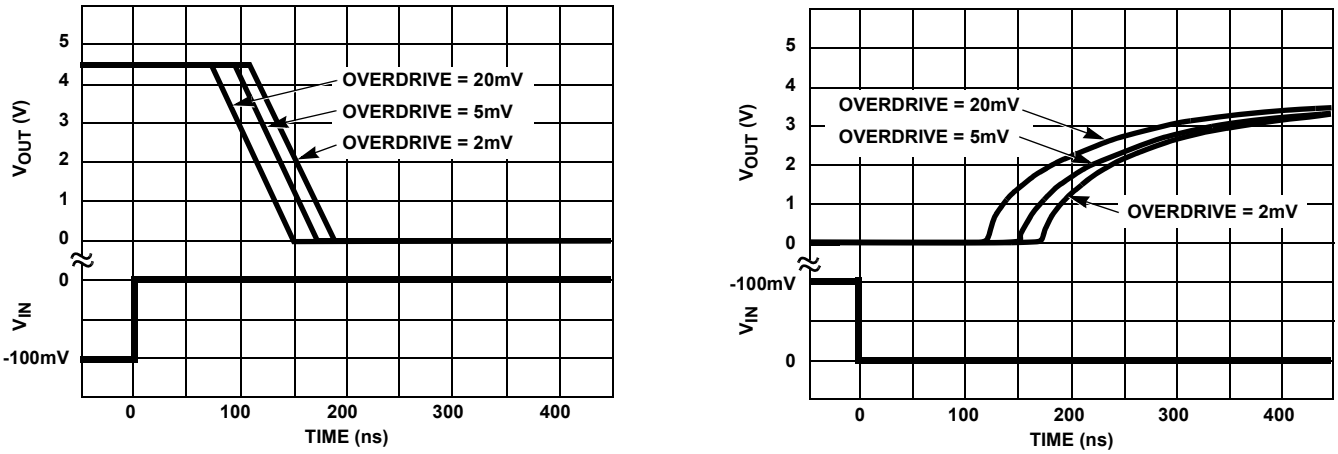

FIGURE 6. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

Design Information (Continued)

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Typical Performance Curves

T_A = +25°C, V_S = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = 0V, Unless Otherwise Specified (Continued)

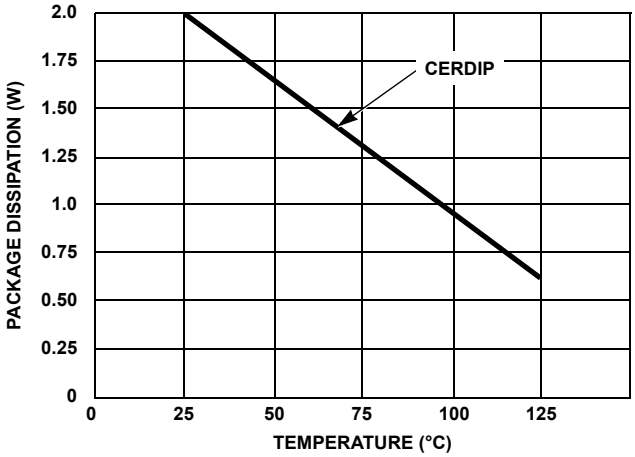

FIGURE 7. MAXIMUM PACKAGE DISSIPATION vs AMBIENT TEMPERATURE

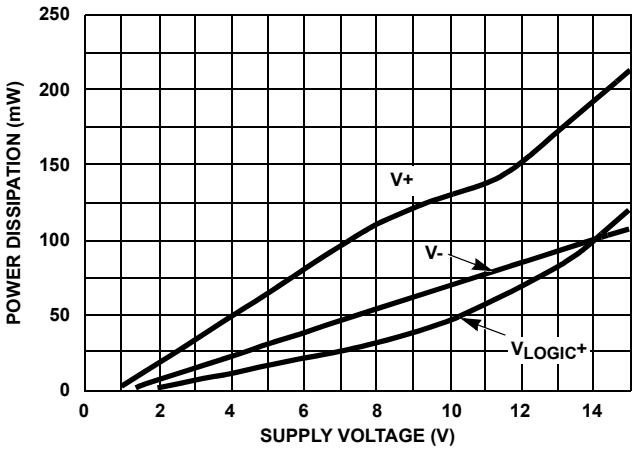

FIGURE 8. POWER DISSIPATION vs SUPPLY VOLTAGE (NO LOAD CONDITION)

NOTE: Total Power Dissipation (TPD) is the sum of individual dissipation contributions of V+, V-, and V_{LOGIC} shown in curves of Power Dissipation vs Supply Voltages. The calculated TPD is then located on the graph of maximum Allowable Package Dissipation vs Ambient Temperature to determine ambient temperature operating limits imposed by the calculated TPD (see Performance Curves). For instance, the combination of ±15V, 5V, 0V (±V, V_{LOGIC}+, V_{LOGIC}-) gives a TPD of 350mW, the combination ±15V, 0V gives a TPD of 450mW.

Design Information

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Typical Performance Characteristics

Device Characterized at: Supply Voltage = ±15V, V_{L+} = 5V, V_{L-} = 0V, unless otherwise specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	Note 4	Full	0.5	Table 1	mV
Input Bias Current		+25°C	50	Table 1	nA
		Full	90	Table 1	nA
Input Offset Current		+25°C	10	Table 1	nA
		Full	20	Table 1	nA
Input Sensitivity	Note 4	Full	50	Table 1	µV
Output Level	V_{OL}; I_{SINK} = 3mA	Full	0.15	Table 1	V
	V_{OH}; I_{SOURCE} = 3mA	Full	4.3	Table 1	V
Supply Current	$+I_{CC}$; $V_{OUT} = V_{OH}$	Full	10	Table 1	mA
	$+I_{CC}$; $V_{OUT} = V_{OL}$	Full	15	Table 1	mA
	$-I_{CC}$; $V_{OUT} = V_{OH}$	Full	-6	Table 1	mA
	$-I_{CC}$; $V_{OUT} = V_{OL}$	Full	-8	Table 1	mA
Logic Current	I_L; $V_{OUT} = V_{OH}$	Full	2	Table 1	mA
	I_L; $V_{OUT} = V_{OL}$	Full	4	Table 1	mA
Response Time	t_{pd0}	Full	150	Table 3	ns
	t_{pd1}	Full	150	Table 3	ns

Applying the HA-4902 Comparator

Supply Connections

This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{LOGIC}+ and V_{LOGIC}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V_{P-P}, Max) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{LOGIC}+ may be connected together to the positive supply while V- and V_{LOGIC}- are grounded. If an input signal could swing negative with respect to the V- terminal, a resistor should be connected in series with the input to limit input current to <5mA since the C-B junction of the input transistor would be forward biased.

Unused Inputs

Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter" ($V_{DIFF} \geq V_{IO}$). All unused inverting inputs may be tied to +5V and non-inverting inputs tied to ground.

Crosstalk

Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{IO}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

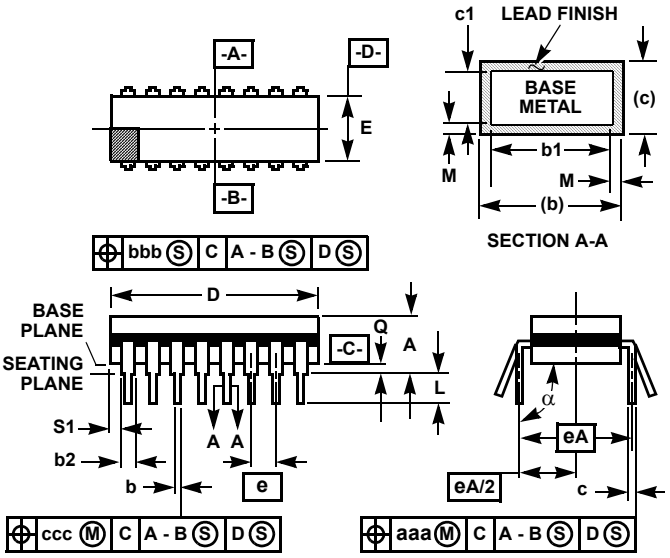
Power Supply Decoupling

Decouple all power supply lines with 0.01µF ceramic capacitors to a ground line located near the package to reduce coupling between channels or from external sources.

Response Time

Fast rise time (<200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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