

Description

The 8V49NS0312 is a Clock Generator with four output dividers: three integer and one that is either integer or fractional. When used with an external crystal, the 8V49NS0312 generates high-performance timing geared towards the communications and datacom markets, especially for applications that demand extremely low phase noise, such as 10, 40, and 100GE.

The 8V49NS0312 provides versatile frequency configurations and output formats and is optimized to deliver excellent phase noise performance. The device delivers an optimum combination of high clock frequency and low phase noise performance, combined with high power supply noise rejection.

The 8V49NS0312 supports two types of output levels: LVPECL or LVDS on eleven of its outputs. In addition, there is a single LVCMOS output that has the option of providing a generated clock or acting as a reference bypass output.

The device can be configured to deliver specific output configurations under pin control only or additional configurations through an I²C serial interface.

It is offered in a lead-free (RoHS6) 64-VFQFPN package.

Features

- Eleven differential LVPECL, LVDS outputs with programmable voltage swings
- One LVCMOS output
 - Input reference maybe bypassed to this output
- The clock input operates in full differential mode (LVDS, LVPECL) or single-ended LVCMOS mode
- Driven from a crystal or differential clock input
- 2.4-2.5GHz PLL frequency range supports Ethernet, SONET and CPRI frequency plans
- Four Integer output dividers with a range of output divide ratios (see [Table 7](#))
- One Fractional Output divider can generate any desired output frequency
- Support of output power-down
- Excellent clock output phase noise

| <u>Offset</u> | <u>Output Frequency</u> | <u>Single-side Band Phase Noise</u> |
|---------------|-------------------------|-------------------------------------|
| 100kHz | 156.25MHz | -143dBc/Hz |
- Phase Noise RMS, 156.25MHz, 12kHz to 20MHz integration range: 110fs (maximum)
- Select configurations may be controlled via the use of control input pins without need for serial port access
- LVCMOS compatible I²C serial interface gives access to additional configurations either alone or in combination with the control input pins
- Single 3.3V supply voltage
- Lead-free (RoHS 6) 64-VFQFPN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram

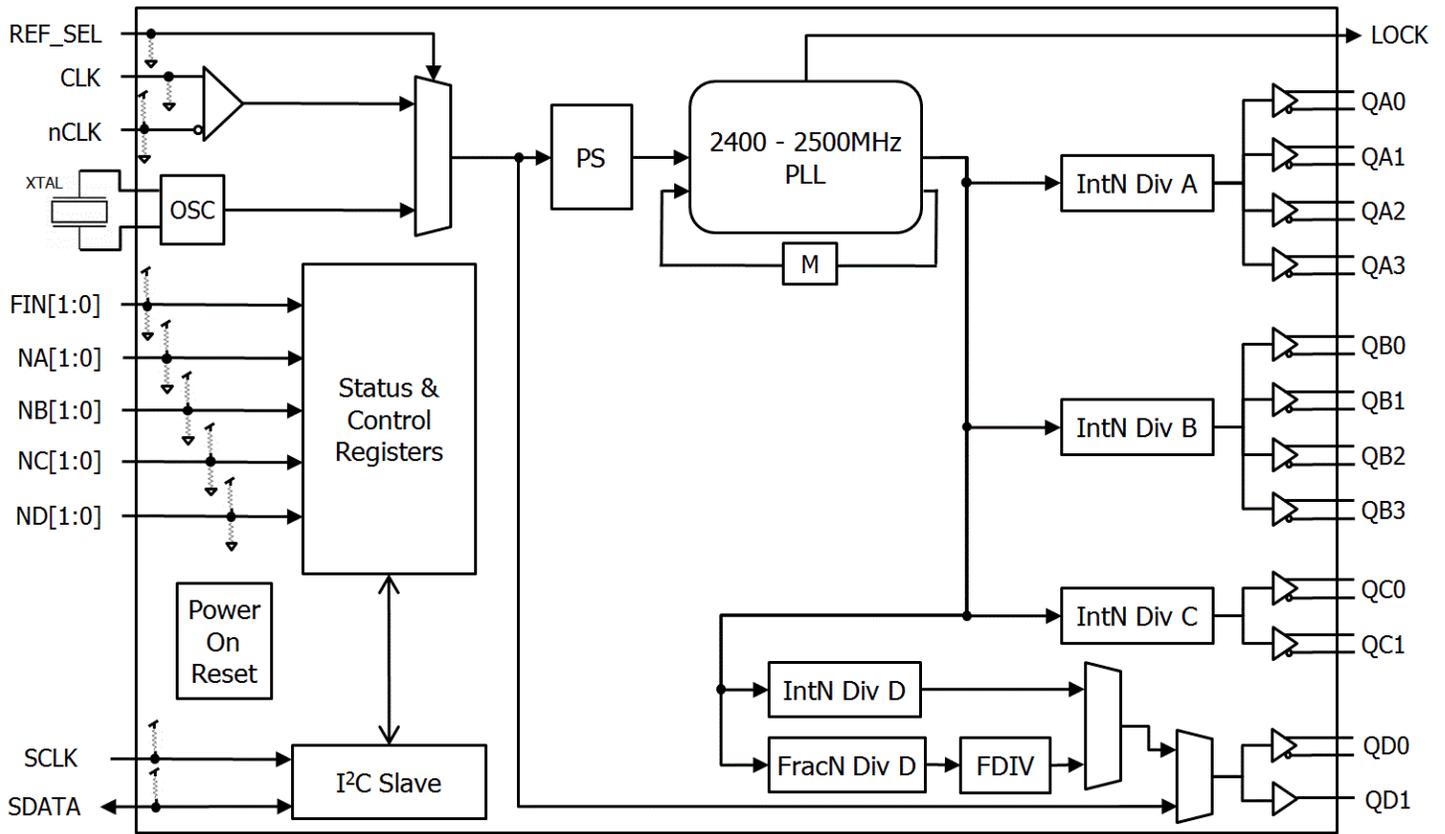
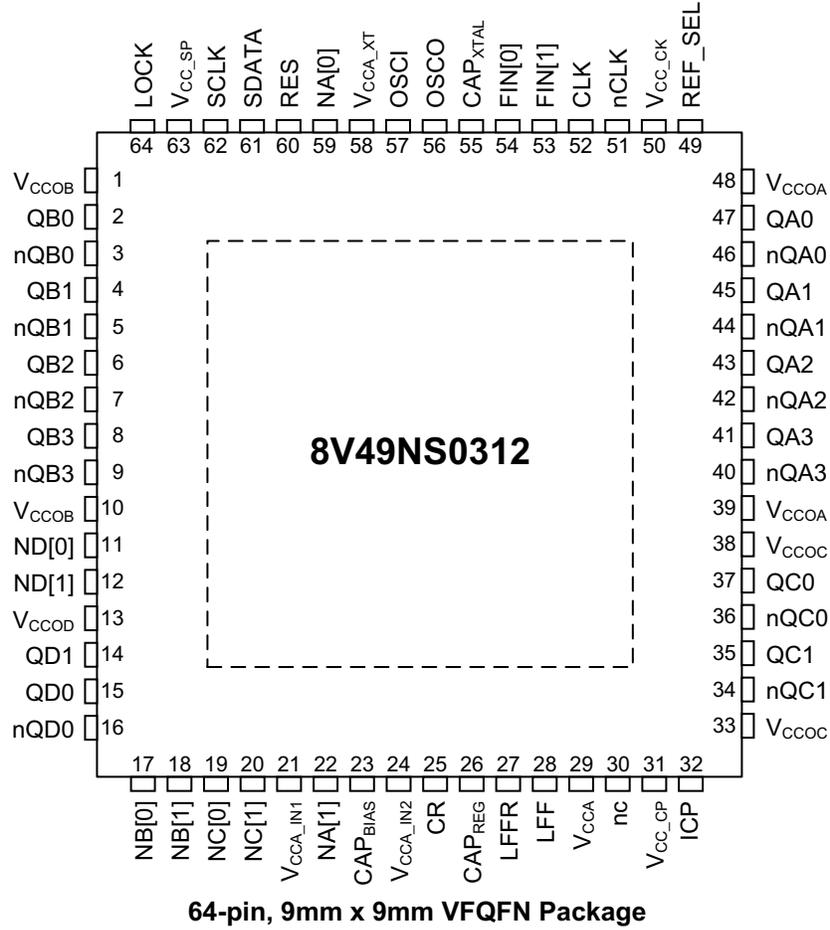


Figure 1: 8V49NS0312 Block Diagram

Pin Assignment



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions^a

| Number | Name | Type | | Description |
|--------|----------------------|--------|-------------------|--|
| 1 | V _{CCOB} | Power | | Power Supply Voltage for Output Bank B (3.3V). |
| 2 | QB0 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 3 | nQB0 | Output | | |
| 4 | QB1 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 5 | nQB1 | Output | | |
| 6 | QB2 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 7 | nQB2 | Output | | |
| 8 | QB3 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 9 | nQB3 | Output | | |
| 10 | V _{CCOB} | Power | | Power Supply Voltage for Output Bank B (3.3V). |
| 11 | ND[0] | Input | Pullup / Pulldown | Control Inputs for Output Bank D. 3-level signals. Refer to Table 12 . |
| 12 | ND[1] | Input | Pullup / Pulldown | Control Inputs for Output Bank D. 3-level signals. Refer to Table 12 . |
| 13 | V _{CCOD} | Power | | Power Supply Voltage for Output Bank D (3.3V). |
| 14 | QD1 | Output | | Single-ended output clock. LVCMOS output levels. |
| 15 | QD0 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 16 | nQD0 | Output | | |
| 17 | NB[0] | Input | Pullup / Pulldown | Control Inputs for Output Bank B. 3-level signals. Refer to Table 10 . |
| 18 | NB[1] | Input | Pullup / Pulldown | Control Inputs for Output Bank B. 3-level signals. Refer to Table 10 . |
| 19 | NC[0] | Input | Pullup / Pulldown | Control Inputs for Output Bank C. 3-level signals. Refer to Table 11 . |
| 20 | NC[1] | Input | Pullup / Pulldown | Control Inputs for Output Bank C. 3-level signals. Refer to Table 11 . |
| 21 | V _{CCA_IN1} | Power | | Analog Power Supply Voltage for PLL (3.3V). |
| 22 | NA[1] | Input | Pullup / Pulldown | Control Inputs for Output Bank A. 3-level signals. Refer to Table 9 . |
| 23 | CAP _{BIAS} | Analog | | Internal VCO bias decoupling capacitor. Use a 4.7μF capacitor between the CAP _{BIAS} terminal and V _{EE} . |
| 24 | V _{CCA_IN2} | Power | | Analog Power Supply Voltage for VCO (3.3V). |
| 25 | CR | Analog | | Internal VCO regulator decoupling capacitor. Use a 1μF capacitor between the CR and the V _{CCA} terminals. |
| 26 | CAP _{REG} | Analog | | Internal VCO regulator decoupling capacitor. Use a 4.7μF capacitor between the CAP _{REG} terminal and V _{EE} . |

Table 1: Pin Descriptions^aCont.

| Number | Name | Type | | Description |
|--------|---------------------|--------|----------------------|---|
| 27 | LFFR | Analog | | Ground return path pin for the PLL loop filter. |
| 28 | LFF | Output | | Loop filter/charge pump output for the FemtoClock NG PLL. Connect to the external loop filter. |
| 29 | V _{CCA} | Power | | Analog Power Supply Voltage for VCO (3.3V). |
| 30 | nc | - | - | No connect. Do not use. |
| 31 | V _{CC_CP} | Power | | Analog Power Supply Voltage for PLL charge pump (3.3V). |
| 32 | ICP | Analog | | Charge pump current input for PLL. Connect to LFF pin (28). |
| 33 | V _{CCOC} | Power | | Power Supply Voltage for Output Bank C (3.3V). |
| 34 | nQC1 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 35 | QC1 | Output | | |
| 36 | nQC0 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 37 | QC0 | Output | | |
| 38 | V _{CCOC} | Power | | Power Supply Voltage for Output Bank C (3.3V). |
| 39 | V _{CCOA} | Power | | Power Supply Voltage for Output Bank A (3.3V). |
| 40 | nQA3 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 41 | QA3 | Output | | |
| 42 | nQA2 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 43 | QA2 | Output | | |
| 44 | nQA1 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 45 | QA1 | Output | | |
| 46 | nQA0 | Output | | Differential device clock output pair. LVPECL or LVDS with configurable amplitude. |
| 47 | QA0 | Output | | |
| 48 | V _{CCOA} | Power | | Power Supply Voltage for Output Bank A (3.3V). |
| 49 | REF_SEL | Input | Pulldown | Selects Input Reference source. LVCMOS interface levels. 0 = Crystal input on pins OSCI, OSCO (default) 1 = Reference clock input on pins CLK, nCLK |
| 50 | V _{CC_CK} | Power | | Power Supply Voltage for input CLK, nCLK (3.3V). |
| 51 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. Internal resistor bias to V _{CC_CK} . |
| 52 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 53 | FIN[1] | Input | Pullup / Pulldown | Control Inputs for Input Reference Frequencies. 3-level signals. Refer to Table 5 . |
| 54 | FIN[0] | Input | Pullup / Pulldown | Control Inputs for Input Reference Frequencies. 3-level signals. Refer to Table 5 . |
| 55 | CAP _{XTAL} | Analog | | Crystal oscillator circuit decoupling capacitor. Use a 4.7μF capacitor between the CAP _{XTAL} and the V _{EE} terminals. |

Table 1: Pin Descriptions^aCont.

| Number | Name | Type | | Description |
|--------|---------------------|--------|-------------------|---|
| 56 | OSCO | Output | | Crystal oscillator interface. |
| 57 | OSCI | Input | | Crystal oscillator interface. |
| 58 | V _{CCA_XT} | Power | | Analog Power Supply Voltage for the Crystal Oscillator (3.3V). |
| 59 | NA[0] | Input | Pullup / Pulldown | Control Inputs for Output Bank A. 3-level signals. Refer to Table 9 . |
| 60 | RES | Analog | | Connect a 2.8 kΩ (1%) resistor to V _{EE} for output current calibration. |
| 61 | SDATA | I/O | Pullup | I ² C data Input/Output: LVCMOS interface levels. Open Drain Pin. |
| 62 | SCLK | Input | Pullup | I ² C clock input. LVCMOS interface levels. |
| 63 | V _{CC_SP} | Power | | Power Supply Voltage for the I ² C port (3.3V). |
| 64 | LOCK | Output | | Lock status output. LVCMOS interface levels. Logic Low = PLL not locked Logic High = PLL locked |
| ePad | V _{EE} | Power | | Negative supply. Exposed pad must be connected to ground |

a. *Pulldown* and *Pullup* refer to internal input resistors. See [Table 2, Input Characteristics](#), for typical values.

Table 2: Input Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--------------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance ^a | | | 3.5 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

a. This specification does not apply to OSCI and OSCO pins.

Table 3: Output Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------|------------------|------|--|---------|---------|---------|-------|
| R _{OUT} | Output Impedance | LOCK | V _{CC} ^a = 3.3V ± 5% | | 20 | | Ω |
| | | QD1 | | | 30 | | Ω |

a. V_{CC} denotes V_{CC_SP}, V_{CCOD}.

Principles of Operation

The 8V49NS0312 can be locked to either an input reference clock or a 10MHz to 50MHz fundamental-mode crystal and generate a wide range of synchronized output clocks. Lock status may be monitored via the LOCK pin.

It could be used for example in either the transmit or receive path of Synchronous Ethernet or SONET/SDH equipment.

The 8V49NS0312 accepts a differential or single-ended input clock ranging from 5MHz up to 1GHz. It generates up to twelve output clocks with up to four different output frequencies, ranging from 10.91MHz up to 2.5GHz.

The device outputs are divided into 4 output banks. Each bank supports conversion of the input frequency to a different output frequency: one independent or integer-related output frequency on Bank D (QD[0:1]) and three more integer-related frequencies on Bank A (QA[0:3]), Bank B (QB[0:3]) and Bank C (QC[0:1]). All outputs within a bank will have the same frequency.

The device is programmable through an I²C serial interface or control input pins.

Pin versus Register Control

The 8V49NS0312 can be configured by the use of input control pins and/or over an I²C serial port. The pins / registers used to control each function are shown in Table 4. At power-up, control of each function is via the control input pins. Access over the serial port can change each function individually to be controlled by registers. This allows for any mixture of register or pin control. However any of the indicated functions can only be controlled by register or by pin at any given time, not by both. Use of register control will allow access to a wider range of configuration options, but values are lost on power-down.

Table 4: Control of Specific Functions

| Function | Control Select Bit | Control Input Pins | Register Fields Affected |
|----------------------------------|--------------------|--------------------|--|
| Prescaler & PLL Feedback Divider | FIN_CTL | FIN[1:0] | PS[5:0], FDP M[8:0] |
| Bank A Divider & Output Type | NA_CTL | NA[1:0] | NA_DIV, PD_A, EN_A, PD_QAx, STY_QAx, AMP_QAx[1:0] |
| Bank B Divider & Output Type | NB_CTL | NB[1:0] | NB_DIV, PD_B, EN_B, PD_QBx, STY_QBx, AMP_QBx[1:0] |
| Bank C Divider & Output Type | NC_CTL | NC[1:0] | NC_DIV, PD_C, EN_C, PD_QCx, STY_QCx, AMP_QCx[1:0] |
| Bank D Divider & Output Type | ND_CTL | ND[1:0] | ND[5:0], ND_FINT[3:0], ND_FRAC[23:0], ND_DIVF[1:0], ND_SRC[1:0], PD_D, EN_D, PD_QDx, STY_QD0, AMP_QD0[1:0] |

Changes to the control input pins while the part is active are allowed, but can not be guaranteed to be glitch-free. It is recommended that any such changes be performed by disabling the outputs using the I²C-accessible registers, then re-enabling once changes are completed. Also, the output dividers, which are synchronized on power-up will not be re-synchronized without an explicit access to the INIT_CLK register bit over the I²C interface.

Any change to the output dividers performed over the I²C interface must be followed by an assertion of the INIT_CLK register bit to force the loading of the new divider values, as well as to synchronize the output dividers.

Input Clock Selection (REF_SEL)

The 8V49NS0312 needs to be provided with an input reference frequency either from its crystal input pins (OSCI, OSCO) or its reference clock input pins (CLK, nCLK). The REF_SEL input pin controls which source is used.

The crystal input on the 8V49NS0312 is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency of 10MHz to 50MHz.

The crystal input also supports being driven by a single-ended crystal oscillator or reference clock, but only a frequency from 10MHz to 50MHz may be used on these pins.

The reference clock input accepts clocks with frequencies ranging from 5MHz up to 1GHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 2.5V or 3.3V logic levels as shown in the Applications Information section of this datasheet.

Prescaler and PLL Configuration

When the input frequency (f_{IN}), whether generated by a crystal or clock input is known, and the desired PLL operating frequency has been determined, several constraints need to be met:

- The Phase / Frequency Detector operating frequency (f_{PFD}) must be within the specified limits shown in [Table 28](#). This is controlled by selecting an appropriate doubler (FDP) and prescaler (PS) value. If multiple values are possible, a higher f_{PFD} will provide better phase noise performance.
- The VCO operating frequency (f_{VCO}) must be within the specified limits shown in [Table 28](#). This is controlled by selecting an appropriate PLL feedback Divider (M) value. Note that it may be necessary to choose a different prescaler value if the limits can not be met by the available values of M. It may also be necessary to select an appropriate input frequency value.

Several preset configurations may be selected directly from the FIN[1:0] control input pins. These configurations are based on a particular input frequency f_{IN} and a particular f_{VCO} (see [Table 5](#)). These selections apply whether the input frequency is provided from the crystal or reference clock inputs

Table 5: Input Selection Control

| FIN[1] | FIN[0] | f_{IN} (MHz) | f_{VCO} (MHz) |
|--------|---------------------|----------------|-----------------|
| High | High | 38.88 | 2488.32 |
| High | Middle ^a | 38.4 | 2457.6 |
| High | Low | 31.25 | 2500 |
| Middle | High | 312.5 | 2500 |
| Middle | Middle | 125 | 2500 |
| Middle | Low | 156.25 | 2500 |
| Low | High | 100 | 2500 |
| Low | Middle | 25 | 2500 |
| Low | Low | 50 | 2500 |

a. A 'middle' voltage level is defined in [Table 22](#). Leaving the input pin open will also generate this level via a weak internal resistor network.

Alternatively the user may directly access the registers for M, FDP & PS over the serial interface for a wider range of options. See [Table 6](#) for some examples.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ± 100 ppm or better.

Table 6: PLL Frequency Control Examples

| f_{IN} (MHz) | PS | FDP | f_{PFD} (MHz) | M | PLL Operating Frequency (MHz) |
|----------------|----|-----|-----------------|----|-------------------------------|
| 25 | 1 | 2 | 50 | 50 | 2500 |
| 39.0625 | 1 | 2 | 78.125 | 32 | 2500 |
| 50 | 1 | 2 | 100 | 25 | 2500 |
| 100 | 1 | 1 | 100 | 25 | 2500 |
| 125 | 1 | 1 | 125 | 20 | 2500 |
| 156.25 | 1 | 1 | 156.25 | 16 | 2500 |
| 200 | 2 | 1 | 100 | 25 | 2500 |
| 250 | 2 | 1 | 125 | 20 | 2500 |
| 312.5 | 2 | 1 | 156.25 | 16 | 2500 |
| 400 | 4 | 1 | 100 | 25 | 2500 |
| 500 | 4 | 1 | 125 | 20 | 2500 |
| 625 | 4 | 1 | 156.25 | 16 | 2500 |
| 19.44 | 1 | 2 | 38.88 | 64 | 2488.32 |
| 38.88 | 1 | 2 | 77.76 | 32 | 2488.32 |
| 38.4 | 1 | 2 | 76.8 | 32 | 2457.6 |

PLL Loop Bandwidth

The 8V49NS0312 uses one external capacitor of fixed value to support its loop bandwidth. A fixed loop bandwidth of approximately 200kHz is provided.

Output Divider Frequency Sources

Output dividers associated with Banks A, B & C take their input frequency directly from the PLL.

Bank D also has the option to bypass the input frequency (after mux) directly to the output.

Integer Output Dividers (Banks A, B, C, and D)

The 8V49NS0312 supports four integer output dividers: one per output bank. Each integer output divider block independently supports one of several divide ratios as shown in their respective register descriptions ([Table 15](#), [Table 16](#), [Table 17](#) or [Table 18](#)). Select divide ratios can be chosen directly from the control input pins for that particular output bank. The remaining ratios can only be selected via the serial interface. Bank D may choose whether to use the integer divider or a separate fractional divider to generate the output.

Some example output frequencies are shown in [Table 7](#) for the minimum f_{VCO} (2400MHz), the maximum f_{VCO} (2500MHz) and two other common VCO frequencies. With appropriate input frequencies and configuration selections, any f_{VCO} and f_{OUT} between the minimum and maximum can be generated.

Table 7: Integer Output Divider Control Examples

| Divide Ratio | f_{OUT} (MHz) | | | |
|--------------|----------------------------|------------------------------|-------------------------------|----------------------------|
| | $f_{VCO} = 2400\text{MHz}$ | $f_{VCO} = 2457.6\text{MHz}$ | $f_{VCO} = 2488.32\text{MHz}$ | $f_{VCO} = 2500\text{MHz}$ |
| 1 | 2400 | 2457.6 | 2488.32 | 2500 |
| 2 | 1200 | 1228.8 | 1244.16 | 1250 |
| 4 | 600 | 614.4 | 622.08 | 625 |
| 5 | 480 | 491.52 | 497.664 | 500 |
| 6 | 400 | 409.6 | 414.72 | 416.667 |
| 8 | 300 | 307.2 | 311.04 | 318.75 |
| 9 | 266.667 | 273.07 | 276.48 | 277.78 |
| 10 | 240 | 245.76 | 248.832 | 250 |
| 12 | 200 | 204.8 | 207.36 | 208.333 |
| 16 | 150 | 153.6 | 155.52 | 156.25 |
| 18 | 133.333 | 136.533 | 138.24 | 138.889 |
| 20 | 120 | 122.88 | 124.416 | 125 |
| 25 | 96 | 98.3 | 99.53 | 100 |
| 32 | 75 | 76.8 | 77.76 | 78.125 |
| 36 | 66.667 | 68.267 | 69.12 | 69.444 |
| 40 | 60 | 61.44 | 62.208 | 62.5 |
| 50 | 48 | 49.152 | 49.766 | 50 |
| 64 | 37.5 | 38.4 | 38.88 | 39.063 |
| 72 | 33.333 | 34.133 | 34.56 | 34.722 |
| 80 | 30 | 30.72 | 31.104 | 31.25 |
| 100 | 24 | 24.576 | 24.883 | 25 |
| 128 | 18.75 | 19.2 | 19.44 | 19.531 |
| 160 | 15 | 15.36 | 15.552 | 15.625 |
| 200 | 12 | 12.29 | 12.44 | 11.36 |
| 220 | 10.91 | 11.17 | 11.31 | 11.36 |

Fractional Output Divider (Bank D)

For the fractional output divider in Bank D, the output divide ratio is given by:

$$f_{OUT} = \frac{f_{VCO}}{2 \times \left(FINT + \frac{FRAC}{2^{24}} \right) \times (FDIV)}$$

Where,

- FINT = Integer Part: 5, 6, ... (2^4-1) - given by ND_FINT[3:0]
- FRAC = Fractional Part: 0, 1, 2, ... $(2^{24}-1)$ - given by ND_FRAC[23:0]
- FDIV = post-divider: 1, 2 or 4- given by ND_DIVF[1:0]

This provides a frequency range of 20MHz to 312.5MHz.

Output Drivers

Each of the four output banks are provided with pin or register-controlled output drivers. Differential outputs may be individually selected as LVDS, LVPECL or POWER-DOWN. When powered down, both outputs of the differential output pair will drive a logic-high level, and the single-ended QD1 output will be in Hi-Z state.

The differential outputs may individually choose one of several different output voltage swings: 350mV, 500mV or 750mV, measured single-ended.

Note that under pin-control, all differential outputs within an output bank will assume the same configuration. Pin-control does not allow configuration of individual outputs within a bank.

Pin Control of the Output Frequencies and Protocols

See [Table 8](#), [Table 9](#), [Table 10](#), [Table 11](#) and [Table 12](#), for pin-control settings. All of the output frequencies assume $f_{VCO} = 2500\text{MHz}$. With different f_{VCO} configurations, the pins may still be used to select the indicated divide ratios for each bank, but the f_{OUT} will be different.

Note that the control pins do not affect the internal register values, but act directly on the output structures. So register values will not change to match the control input pin selections.

Each output bank may be powered-up / down and enabled / disabled by register bits. In the disabled state, an output will drive a logic low level. The default state is all outputs enabled. Pin-control does not require register access to enable the outputs. Additionally, individual outputs within a bank may be powered up / down.

Table 8: Definition of Output Disabled / Power-down

| OUTPUT CONDITION | Q_{MN}^a | nQ_{MN}^b | QD1 |
|--|------------|-------------|------|
| DISABLED (register-control only) | LOW | HIGH | LOW |
| POWER-DOWN (pin-control or register-control) | HIGH | HIGH | Hi-Z |

a. Q_{MN} refers to output pins QA[0:3], QB[0:3], QC[0:1] and QD0.

b. nQ_{MN} refers to output pins nQA[0:3], nQB[0:3], nQC[0:1] and nQD0.

Table 9: Bank A Divider/ Driver Pin-Control
(3-level control signals)

| NA[1] | NA[0] | Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|-------------------------|--------------|------------------------|
| Low | Low | LVPECL ^a | 16 | 156.25 |
| Low | Middle | LVPECL | 20 | 125 |
| Low | High | LVPECL | 25 | 100 |
| Middle | Low | LVPECL | 100 | 25 |
| Middle | Middle | POWER-DOWN ^b | - | - |
| Middle | High | LVDS ^c | 16 | 156.25 |
| High | Low | LVDS | 20 | 125 |
| High | Middle | LVDS | 25 | 100 |
| High | High | LVDS | 50 | 50 |

- a. Under pin control, all outputs of the bank are LVPECL using 750mV output swing.
 b. No active receivers should be connected to QA outputs.
 c. Under pin control, all outputs of the bank are LVDS using 350mV output swing.

Table 10: Bank B Divider/ Driver Pin-Control
(3-level control signals)

| NB[1] | NB[0] | Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|-------------------------|--------------|------------------------|
| Low | Low | LVPECL ^a | 16 | 156.25 |
| Low | Middle | LVPECL | 20 | 125 |
| Low | High | LVPECL | 25 | 100 |
| Middle | Low | LVPECL | 100 | 25 |
| Middle | Middle | POWER-DOWN ^b | - | - |
| Middle | High | LVDS ^c | 16 | 156.25 |
| High | Low | LVDS | 20 | 125 |
| High | Middle | LVDS | 25 | 100 |
| High | High | LVDS | 50 | 50 |

- a. Under pin control, all outputs of the bank are LVPECL using 750mV output swing.
 b. No active receivers should be connected to QB outputs.
 c. Under pin control, all outputs of the bank are LVDS using 350mV output swing.

Table 11: Bank C Divider/ Driver Pin-Control
(3-level control signals)

| NC[1] | NC[0] | Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|-------------------------|--------------|------------------------|
| Low | Low | LVPECL ^a | 8 | 312.5 |
| Low | Middle | LVPECL | 16 | 156.25 |
| Low | High | LVPECL | 20 | 125 |
| Middle | Low | LVPECL | 100 | 25 |
| Middle | Middle | POWER-DOWN ^b | - | - |
| Middle | High | LVDS ^c | 20 | 125 |
| High | Low | LVDS | 25 | 100 |
| High | Middle | LVDS | 50 | 50 |
| High | High | LVDS | 100 | 25 |

- a. Under pin control, all outputs of the bank are LVPECL using 750mV output swing.
 b. No active receivers should be connected to QC outputs.
 c. Under pin control, all outputs of the bank are LVDS using 350mV output swing.

Table 12: Bank D Divider/ Driver Pin-Control
(3-level control signals)

| ND[1] | ND[0] | QD0 Output Type | QD1 Output Type | Divide Ratio | f _{OUT} (MHz) |
|--------|--------|-------------------------|-----------------|--------------------|------------------------------|
| Low | Low | LVDS ^a | Hi-Z | 25 | 100 |
| Low | Middle | LVDS | Hi-Z | 50 | 50 |
| Low | High | LVDS | Hi-Z | 18.75 ^b | 133.333 |
| Middle | Low | LVDS | Hi-Z | 37.5 ^b | 66.667 |
| Middle | Middle | POWER-DOWN ^c | Hi-Z | - | - |
| Middle | High | POWER-DOWN ^c | LVC MOS | 75 | 33.333 |
| High | Low | LVDS | Hi-Z | 100 | 25 |
| High | Middle | LVDS | Hi-Z | 20 | 125 |
| High | High | LVDS | LVC MOS | 1 | f _{IN} ^d |

- a. Under pin control, all outputs of the bank are LVDS using 350mV output swing.
 b. Generated from Fractional divider.
 c. No active receivers should be connected to QD0 output.
 d. This bypasses the input frequency directly to the output.

Device Start-up and Reset Behavior

The 8V49NS0312 has an internal power-on reset (POR) circuit. The POR circuit will remain active for a maximum of 175msec after device power-up.

While in the reset state (POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- All clock outputs will be enabled.
- Lock status will be cleared.

Upon the internal POR circuit expiring, the device will exit reset and begin self-configuration.

Self-configuration will consist of loading appropriate default values into each register as indicated by the control input pins and the defaults indicated in the register descriptions.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock the PLL to the input frequency and begin operation. Once the PLL is locked, all the outputs derived from it will be synchronized.

Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I²C compatible configuration at a base address of 1101100b, to allow access to any of the internal registers for device programming or examination of internal status.

All registers are configured to have default values. See the specifics for each register for details. Default values for registers will be set after reset by the configuration pins.

Any changes to the configuration pins will result in the appropriate register(s) being changed to reflect the new pin-controlled setup. Any such change while the part is operating may result in glitches on output clocks, even if those particular clocks are not being reconfigured.

I²C Mode Operation

The I²C interface is designed to fully support v1.2 of the I²C Specification for Normal and Fast mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using a fixed base address of 1101100b. The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

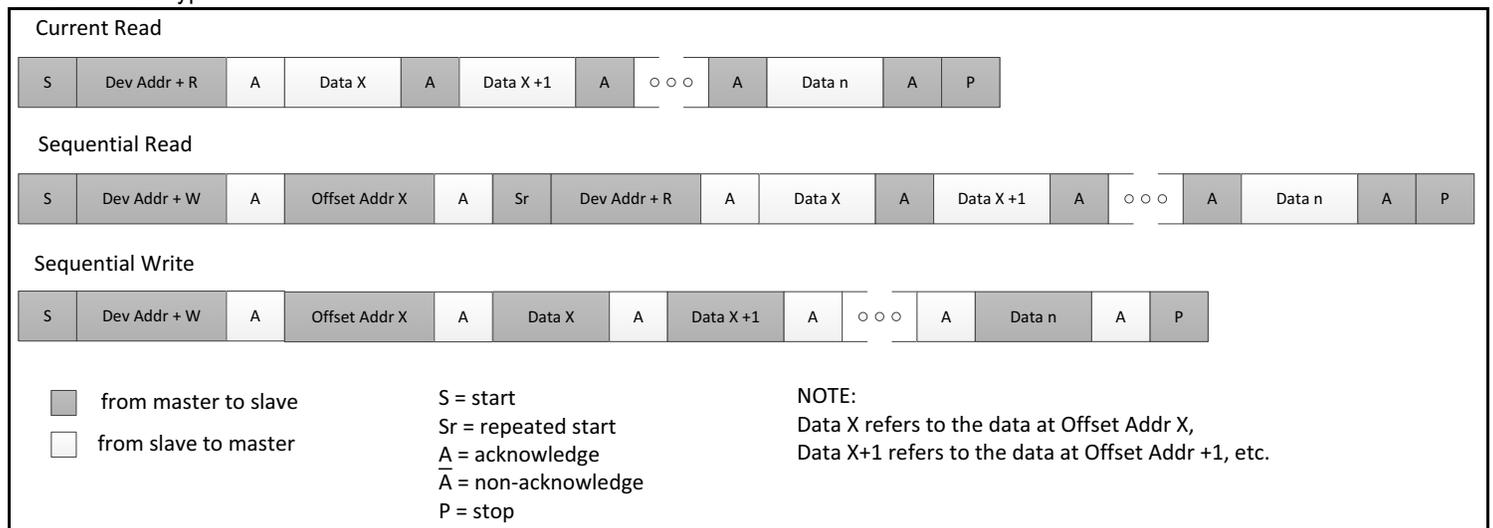


Figure 2: I²C Slave Read and Write Cycle Sequencing

Register Description

Table 13: Register Blocks

| Register Ranges Offset (Hex) | Register Block Description |
|------------------------------|-----------------------------------|
| 00 - 08 | Prescaler & PLL Control Registers |
| 09 - 0F | Reserved ^a |
| 10 - 17 | Bank A Control Registers |
| 18 - 1F | Bank B Control Registers |
| 20 - 27 | Bank C Control Registers |
| 28 - 31 | Bank D Control Registers |
| 32 - 37 | Reserved |
| 38 - 3C | Reserved |
| 3D - 40 | Device Control Registers |
| 41 - 4B | Reserved |
| 4C - 4F | Reserved |
| 50 - FF | Reserved |

a. Reserved registers should not be written to and have indeterminate read values.

Table 14: Prescaler & PLL Control Register Bit Field Locations and Descriptions

| Prescaler & PLL Control Register Block Field Locations | | | | | | | | |
|---|------------|---------------|--|---------|----|---------|---------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 D0 | |
| 00 | Rsvd | Rsvd | PS[5:0] | | | | | |
| 01 | Rsvd | | | | | | FDP | |
| 02 | Rsvd | | | | | FIN_CTL | OSC_LOW | |
| 03 | Rsvd | | | | | | | |
| 04 | Rsvd | | | | | | M[8] | |
| 05 | M[7:0] | | | | | | | |
| 06 | Rsvd | | | | | | | |
| 07 | Rsvd | | | | | | | |
| 08 | Rsvd | | | CP[4:0] | | | | |
| Prescaler & PLL Control Register Block Field Descriptions | | | | | | | | |
| Bit Field Name | Field Type | Default Value | Description | | | | | |
| PS[5:0] | R/W | 000000b | Prescaler - scales input frequency by the value: 00h = Reserved 01h - 7Fh = divide by the value used (e.g. 04 = divide-by-4) | | | | | |
| FDP | R/W | 1b | Input frequency doubler: 0 = disabled 1 = enabled | | | | | |
| FIN_CTL | R/W | 0b | Prescaler and PLL Configuration Control: 0 = PS[5:0], FDP and M settings determined by FIN[1:0] control pins 1 = PS[5:0], FDP and M settings determined by register settings over I ² C | | | | | |
| OSC_LOW | R/W | 0b | Crystal oscillator gain control selection: 0 = normal gain for crystal frequencies of 25MHz and up 1 = low gain for crystal frequencies less than 25MHz | | | | | |
| M[8:0] | R/W | 019h | PLL Feedback divider ratio: 000h - 003h = Reserved (do not use) 004h - 1FFh = divide f_{VCO} by the value | | | | | |
| CP[4:0] | R/W | 11001b | PLL Charge Pump Current Control: $I_{CP} = 200\mu A \times (CP[4:0] + 1)$. Max. charge pump current is 6.4 mA. Default setting is 5.2mA: $((25+1) \times 200\mu A)$. | | | | | |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. | | | | | |

Table 15: Bank A Control Register Bit Field Locations and Descriptions

| Bank A Control Register Block Field Locations | | | | | | | | | |
|---|--------|------|---------|----|---------|------|--------------|--------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 10 | Rsvd | | NA[5:0] | | | | | | |
| 11 | Rsvd | | | | | | | | |
| 12 | PD_A | Rsvd | | | | Rsvd | | NA_CTL | |
| 13 | Rsvd | | | | | | | | |
| 14 | PD_QA0 | Rsvd | | | STY_QA0 | | AMP_QA0[1:0] | | |
| 15 | PD_QA1 | Rsvd | | | STY_QA1 | | AMP_QA1[1:0] | | |
| 16 | PD_QA2 | Rsvd | | | STY_QA2 | | AMP_QA2[1:0] | | |
| 17 | PD_QA3 | Rsvd | | | STY_QA3 | | AMP_QA3[1:0] | | |

| Bank A Control Register Block Field Descriptions | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|----------------|---------------------|---|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|---------------------|----------------|----------------|---------------------|----------------|----------------|---------------------|----------------|----------------|---------------------|
| Bit Field Name | Field Type | Default Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NA[5:0] | R/W | 0Dh | <p>Divider ratio for Bank A: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.</p> <p>00 0000b = Reserved</p> <table border="0"> <tr> <td>00 0001b = +1</td> <td>01 0110b = +30</td> <td>10 1011b = +88</td> </tr> <tr> <td>00 0010b = +2</td> <td>01 0111b = +32</td> <td>10 1100b = +90</td> </tr> <tr> <td>00 0011b = +3</td> <td>01 1000b = +33</td> <td>10 1101b = +96</td> </tr> <tr> <td>00 0100b = +4</td> <td>01 1001b = +35</td> <td>10 1110b = +100</td> </tr> <tr> <td>00 0101b = +5</td> <td>01 1010b = +36</td> <td>10 1111b = +108</td> </tr> <tr> <td>00 0110b = +6</td> <td>01 1011b = +40</td> <td>11 0000b = +110</td> </tr> <tr> <td>00 0111b = +8</td> <td>01 1100b = +42</td> <td>11 0001b = +112</td> </tr> <tr> <td>00 1000b = +9</td> <td>01 1101b = +44</td> <td>11 0010b = +120</td> </tr> <tr> <td>00 1001b = +10</td> <td>01 1110b = +45</td> <td>11 0011b = +128</td> </tr> <tr> <td>00 1010b = +12</td> <td>01 1111b = +48</td> <td>11 0100b = +132</td> </tr> <tr> <td>00 1011b = +14</td> <td>10 0000b = +50</td> <td>11 0101b = +140</td> </tr> <tr> <td>00 1100b = +15</td> <td>10 0001b = +54</td> <td>11 0110b = +144</td> </tr> <tr> <td>00 1101b = +16</td> <td>10 0010b = +55</td> <td>11 0111b = +160</td> </tr> <tr> <td>00 1110b = +18</td> <td>10 0011b = +56</td> <td>11 1000b = +176</td> </tr> <tr> <td>00 1111b = +20</td> <td>10 0100b = +60</td> <td>11 1001b = +180</td> </tr> <tr> <td>01 0000b = +21</td> <td>10 0101b = +64</td> <td>11 1010b = +200</td> </tr> <tr> <td>01 0001b = +22</td> <td>10 0110b = +66</td> <td>11 1011b = +220</td> </tr> <tr> <td>01 0010b = +24</td> <td>10 0111b = +70</td> <td>11 1100b = Reserved</td> </tr> <tr> <td>01 0011b = +25</td> <td>10 1000b = +72</td> <td>11 1101b = Reserved</td> </tr> <tr> <td>01 0100b = +27</td> <td>10 1001b = +80</td> <td>11 1110b = Reserved</td> </tr> <tr> <td>01 0101b = +28</td> <td>10 1010b = +84</td> <td>11 1111b = Reserved</td> </tr> </table> | 00 0001b = +1 | 01 0110b = +30 | 10 1011b = +88 | 00 0010b = +2 | 01 0111b = +32 | 10 1100b = +90 | 00 0011b = +3 | 01 1000b = +33 | 10 1101b = +96 | 00 0100b = +4 | 01 1001b = +35 | 10 1110b = +100 | 00 0101b = +5 | 01 1010b = +36 | 10 1111b = +108 | 00 0110b = +6 | 01 1011b = +40 | 11 0000b = +110 | 00 0111b = +8 | 01 1100b = +42 | 11 0001b = +112 | 00 1000b = +9 | 01 1101b = +44 | 11 0010b = +120 | 00 1001b = +10 | 01 1110b = +45 | 11 0011b = +128 | 00 1010b = +12 | 01 1111b = +48 | 11 0100b = +132 | 00 1011b = +14 | 10 0000b = +50 | 11 0101b = +140 | 00 1100b = +15 | 10 0001b = +54 | 11 0110b = +144 | 00 1101b = +16 | 10 0010b = +55 | 11 0111b = +160 | 00 1110b = +18 | 10 0011b = +56 | 11 1000b = +176 | 00 1111b = +20 | 10 0100b = +60 | 11 1001b = +180 | 01 0000b = +21 | 10 0101b = +64 | 11 1010b = +200 | 01 0001b = +22 | 10 0110b = +66 | 11 1011b = +220 | 01 0010b = +24 | 10 0111b = +70 | 11 1100b = Reserved | 01 0011b = +25 | 10 1000b = +72 | 11 1101b = Reserved | 01 0100b = +27 | 10 1001b = +80 | 11 1110b = Reserved | 01 0101b = +28 | 10 1010b = +84 | 11 1111b = Reserved |
| 00 0001b = +1 | 01 0110b = +30 | 10 1011b = +88 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0010b = +2 | 01 0111b = +32 | 10 1100b = +90 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0011b = +3 | 01 1000b = +33 | 10 1101b = +96 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0100b = +4 | 01 1001b = +35 | 10 1110b = +100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0101b = +5 | 01 1010b = +36 | 10 1111b = +108 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0110b = +6 | 01 1011b = +40 | 11 0000b = +110 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0111b = +8 | 01 1100b = +42 | 11 0001b = +112 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1000b = +9 | 01 1101b = +44 | 11 0010b = +120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1001b = +10 | 01 1110b = +45 | 11 0011b = +128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1010b = +12 | 01 1111b = +48 | 11 0100b = +132 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1011b = +14 | 10 0000b = +50 | 11 0101b = +140 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1100b = +15 | 10 0001b = +54 | 11 0110b = +144 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1101b = +16 | 10 0010b = +55 | 11 0111b = +160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1110b = +18 | 10 0011b = +56 | 11 1000b = +176 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1111b = +20 | 10 0100b = +60 | 11 1001b = +180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0000b = +21 | 10 0101b = +64 | 11 1010b = +200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0001b = +22 | 10 0110b = +66 | 11 1011b = +220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0010b = +24 | 10 0111b = +70 | 11 1100b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0011b = +25 | 10 1000b = +72 | 11 1101b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0100b = +27 | 10 1001b = +80 | 11 1110b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0101b = +28 | 10 1010b = +84 | 11 1111b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD_A | R/W | 0b | <p>Power-down Bank A: 0 = Bank A & all QA outputs powered and operate normally 1 = Bank A & all QA outputs powered-down - no active receivers should be connected to QA outputs. When powering-down the output bank, it is recommended to also write a '1' to the PD_QAx registers.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NA_CTL | R/W | 0b | <p>Bank A Configuration Control: 0 = NA[5:0], PD_A, EN_A, STY_Ax and AMP_Ax[1:0] settings determined by NA[1:0] control pins 1 = NA[5:0], PD_A, EN_A, STY_Ax and AMP_Ax[1:0] settings determined by register settings over I²C</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD_QAx | R/W | 0b | <p>Power-down Output QAx: 0 = QAx output powered and operates normally 1 = QAx output powered-down - no active receivers should be connected to the QAx output</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Bank A Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| STY_QAx | R/W | 0b | Output Style for Output QAx: 0 = QAx is LVDS 1 = QAx is LVPECL |
| AMP_QAx[1:0] | R/W | 00b | Output Amplitude for Output QAx (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 16: Bank B Control Register Bit Field Locations and Descriptions

| Bank B Control Register Block Field Locations | | | | | | | | | |
|---|--------|------|---------|----|----|---------|--------------|--------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 18 | Rsvd | | NB[5:0] | | | | | | |
| 19 | Rsvd | | | | | | | | |
| 1A | PD_B | Rsvd | | | | | | NB_CTL | |
| 1B | Rsvd | | | | | | | | |
| 1C | PD_QB0 | Rsvd | | | | STY_QB0 | AMP_QB0[1:0] | | |
| 1D | PD_QB1 | Rsvd | | | | STY_QB1 | AMP_QB1[1:0] | | |
| 1E | PD_QB2 | Rsvd | | | | STY_QB2 | AMP_QB2[1:0] | | |
| 1F | PD_QB3 | Rsvd | | | | STY_QB3 | AMP_QB3[1:0] | | |

| Bank B Control Register Block Field Descriptions | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|----------------|---------------------|---|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|---------------------|----------------|----------------|---------------------|----------------|----------------|---------------------|----------------|----------------|---------------------|
| Bit Field Name | Field Type | Default Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NB[5:0] | R/W | 0Dh | <p>Divider ratio for Bank B: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.</p> <p>00 0000b = Reserved</p> <table border="0"> <tr> <td>00 0001b = +1</td> <td>01 0110b = +30</td> <td>10 1011b = +88</td> </tr> <tr> <td>00 0010b = +2</td> <td>01 0111b = +32</td> <td>10 1100b = +90</td> </tr> <tr> <td>00 0011b = +3</td> <td>01 1000b = +33</td> <td>10 1101b = +96</td> </tr> <tr> <td>00 0100b = +4</td> <td>01 1001b = +35</td> <td>10 1110b = +100</td> </tr> <tr> <td>00 0101b = +5</td> <td>01 1010b = +36</td> <td>10 1111b = +108</td> </tr> <tr> <td>00 0110b = +6</td> <td>01 1011b = +40</td> <td>11 0000b = +110</td> </tr> <tr> <td>00 0111b = +8</td> <td>01 1100b = +42</td> <td>11 0001b = +112</td> </tr> <tr> <td>00 1000b = +9</td> <td>01 1101b = +44</td> <td>11 0010b = +120</td> </tr> <tr> <td>00 1001b = +10</td> <td>01 1110b = +45</td> <td>11 0011b = +128</td> </tr> <tr> <td>00 1010b = +12</td> <td>01 1111b = +48</td> <td>11 0100b = +132</td> </tr> <tr> <td>00 1011b = +14</td> <td>10 0000b = +50</td> <td>11 0101b = +140</td> </tr> <tr> <td>00 1100b = +15</td> <td>10 0001b = +54</td> <td>11 0110b = +144</td> </tr> <tr> <td>00 1101b = +16</td> <td>10 0010b = +55</td> <td>11 0111b = +160</td> </tr> <tr> <td>00 1110b = +18</td> <td>10 0011b = +56</td> <td>11 1000b = +176</td> </tr> <tr> <td>00 1111b = +20</td> <td>10 0100b = +60</td> <td>11 1001b = +180</td> </tr> <tr> <td>01 0000b = +21</td> <td>10 0101b = +64</td> <td>11 1010b = +200</td> </tr> <tr> <td>01 0001b = +22</td> <td>10 0110b = +66</td> <td>11 1011b = +220</td> </tr> <tr> <td>01 0010b = +24</td> <td>10 0111b = +70</td> <td>11 1100b = Reserved</td> </tr> <tr> <td>01 0011b = +25</td> <td>10 1000b = +72</td> <td>11 1101b = Reserved</td> </tr> <tr> <td>01 0100b = +27</td> <td>10 1001b = +80</td> <td>11 1110b = Reserved</td> </tr> <tr> <td>01 0101b = +28</td> <td>10 1010b = +84</td> <td>11 1111b = Reserved</td> </tr> </table> | 00 0001b = +1 | 01 0110b = +30 | 10 1011b = +88 | 00 0010b = +2 | 01 0111b = +32 | 10 1100b = +90 | 00 0011b = +3 | 01 1000b = +33 | 10 1101b = +96 | 00 0100b = +4 | 01 1001b = +35 | 10 1110b = +100 | 00 0101b = +5 | 01 1010b = +36 | 10 1111b = +108 | 00 0110b = +6 | 01 1011b = +40 | 11 0000b = +110 | 00 0111b = +8 | 01 1100b = +42 | 11 0001b = +112 | 00 1000b = +9 | 01 1101b = +44 | 11 0010b = +120 | 00 1001b = +10 | 01 1110b = +45 | 11 0011b = +128 | 00 1010b = +12 | 01 1111b = +48 | 11 0100b = +132 | 00 1011b = +14 | 10 0000b = +50 | 11 0101b = +140 | 00 1100b = +15 | 10 0001b = +54 | 11 0110b = +144 | 00 1101b = +16 | 10 0010b = +55 | 11 0111b = +160 | 00 1110b = +18 | 10 0011b = +56 | 11 1000b = +176 | 00 1111b = +20 | 10 0100b = +60 | 11 1001b = +180 | 01 0000b = +21 | 10 0101b = +64 | 11 1010b = +200 | 01 0001b = +22 | 10 0110b = +66 | 11 1011b = +220 | 01 0010b = +24 | 10 0111b = +70 | 11 1100b = Reserved | 01 0011b = +25 | 10 1000b = +72 | 11 1101b = Reserved | 01 0100b = +27 | 10 1001b = +80 | 11 1110b = Reserved | 01 0101b = +28 | 10 1010b = +84 | 11 1111b = Reserved |
| 00 0001b = +1 | 01 0110b = +30 | 10 1011b = +88 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0010b = +2 | 01 0111b = +32 | 10 1100b = +90 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0011b = +3 | 01 1000b = +33 | 10 1101b = +96 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0100b = +4 | 01 1001b = +35 | 10 1110b = +100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0101b = +5 | 01 1010b = +36 | 10 1111b = +108 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0110b = +6 | 01 1011b = +40 | 11 0000b = +110 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0111b = +8 | 01 1100b = +42 | 11 0001b = +112 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1000b = +9 | 01 1101b = +44 | 11 0010b = +120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1001b = +10 | 01 1110b = +45 | 11 0011b = +128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1010b = +12 | 01 1111b = +48 | 11 0100b = +132 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1011b = +14 | 10 0000b = +50 | 11 0101b = +140 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1100b = +15 | 10 0001b = +54 | 11 0110b = +144 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1101b = +16 | 10 0010b = +55 | 11 0111b = +160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1110b = +18 | 10 0011b = +56 | 11 1000b = +176 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1111b = +20 | 10 0100b = +60 | 11 1001b = +180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0000b = +21 | 10 0101b = +64 | 11 1010b = +200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0001b = +22 | 10 0110b = +66 | 11 1011b = +220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0010b = +24 | 10 0111b = +70 | 11 1100b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0011b = +25 | 10 1000b = +72 | 11 1101b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0100b = +27 | 10 1001b = +80 | 11 1110b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0101b = +28 | 10 1010b = +84 | 11 1111b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD_B | R/W | 0b | <p>Power-down Bank B: 0 = Bank B & all QB outputs powered and operate normally 1 = Bank B & all QB outputs powered-down - no active receivers should be connected to QB outputs</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NB_CTL | R/W | 0b | <p>Bank A Configuration Control: 0 = NB[5:0], PD_B, EN_B, STY_Bx and AMP_Bx[1:0] settings determined by NB[1:0] control pins 1 = NB[5:0], PD_B, EN_B, STY_Bx and AMP_Bx[1:0] settings determined by register settings over I²C</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD_QBx | R/W | 0b | <p>Power-down Output QBx: 0 = QBx output powered and operates normally 1 = QBx output powered-down - no active receivers should be connected to the QBx output. When powering-down the output bank, it is recommended to also write a '1' to the PD_QBx registers.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Bank B Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| STY_QBx | R/W | 0b | Output Style for Output QBx: 0 = QBx is LVDS 1 = QBx is LVPECL |
| AMP_QBx[1:0] | R/W | 00b | Output Amplitude for Output QBx (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 17: Bank C Control Register Bit Field Locations and Descriptions

| Bank C Control Register Block Field Locations | | | | | | | |
|---|--------|------|---------|----|---------|--------------|-------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 D0 |
| 20 | Rsvd | | NC[5:0] | | | | |
| 21 | Rsvd | | | | | | |
| 22 | PD_C | Rsvd | | | | NC_CTL | |
| 23 | Rsvd | | | | | | |
| 24 | PD_QC0 | Rsvd | | | STY_QC0 | AMP_QC0[1:0] | |
| 25 | PD_QC1 | Rsvd | | | STY_QC1 | AMP_QC1[1:0] | |
| 26 | Rsvd | | | | | | |
| 27 | Rsvd | | | | | | |

| Bank C Control Register Block Field Descriptions | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|----------------|---------------------|---|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|---------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|---------------------|----------------|----------------|---------------------|----------------|----------------|---------------------|----------------|----------------|---------------------|
| Bit Field Name | Field Type | Default Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC[5:0] | R/W | 0Dh | <p>Divider ratio for Bank C: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.</p> <p>00 0000b = Reserved</p> <table border="0"> <tr> <td>00 0001b = +1</td> <td>01 0110b = +30</td> <td>10 1011b = +88</td> </tr> <tr> <td>00 0010b = +2</td> <td>01 0111b = +32</td> <td>10 1100b = +90</td> </tr> <tr> <td>00 0011b = +3</td> <td>01 1000b = +33</td> <td>10 1101b = +96</td> </tr> <tr> <td>00 0100b = +4</td> <td>01 1001b = +35</td> <td>10 1110b = +100</td> </tr> <tr> <td>00 0101b = +5</td> <td>01 1010b = +36</td> <td>10 1111b = +108</td> </tr> <tr> <td>00 0110b = +6</td> <td>01 1011b = +40</td> <td>11 0000b = +110</td> </tr> <tr> <td>00 0111b = +8</td> <td>01 1100b = +42</td> <td>11 0001b = +112</td> </tr> <tr> <td>00 1000b = +9</td> <td>01 1101b = +44</td> <td>11 0010b = +120</td> </tr> <tr> <td>00 1001b = +10</td> <td>01 1110b = +45</td> <td>11 0011b = +128</td> </tr> <tr> <td>00 1010b = +12</td> <td>01 1111b = +48</td> <td>11 0100b = +132</td> </tr> <tr> <td>00 1011b = +14</td> <td>10 0000b = +50</td> <td>11 0101b = +140</td> </tr> <tr> <td>00 1100b = +15</td> <td>10 0001b = +54</td> <td>11 0110b = +144</td> </tr> <tr> <td>00 1101b = +16</td> <td>10 0010b = +55</td> <td>11 0111b = +160</td> </tr> <tr> <td>00 1110b = +18</td> <td>10 0011b = +56</td> <td>11 1000b = +176</td> </tr> <tr> <td>00 1111b = +20</td> <td>10 0100b = +60</td> <td>11 1001b = +180</td> </tr> <tr> <td>01 0000b = +21</td> <td>10 0101b = +64</td> <td>11 1010b = +200</td> </tr> <tr> <td>01 0001b = +22</td> <td>10 0110b = +66</td> <td>11 1011b = +220</td> </tr> <tr> <td>01 0010b = +24</td> <td>10 0111b = +70</td> <td>11 1100b = Reserved</td> </tr> <tr> <td>01 0011b = +25</td> <td>10 1000b = +72</td> <td>11 1101b = Reserved</td> </tr> <tr> <td>01 0100b = +27</td> <td>10 1001b = +80</td> <td>11 1110b = Reserved</td> </tr> <tr> <td>01 0101b = +28</td> <td>10 1010b = +84</td> <td>11 1111b = Reserved</td> </tr> </table> | 00 0001b = +1 | 01 0110b = +30 | 10 1011b = +88 | 00 0010b = +2 | 01 0111b = +32 | 10 1100b = +90 | 00 0011b = +3 | 01 1000b = +33 | 10 1101b = +96 | 00 0100b = +4 | 01 1001b = +35 | 10 1110b = +100 | 00 0101b = +5 | 01 1010b = +36 | 10 1111b = +108 | 00 0110b = +6 | 01 1011b = +40 | 11 0000b = +110 | 00 0111b = +8 | 01 1100b = +42 | 11 0001b = +112 | 00 1000b = +9 | 01 1101b = +44 | 11 0010b = +120 | 00 1001b = +10 | 01 1110b = +45 | 11 0011b = +128 | 00 1010b = +12 | 01 1111b = +48 | 11 0100b = +132 | 00 1011b = +14 | 10 0000b = +50 | 11 0101b = +140 | 00 1100b = +15 | 10 0001b = +54 | 11 0110b = +144 | 00 1101b = +16 | 10 0010b = +55 | 11 0111b = +160 | 00 1110b = +18 | 10 0011b = +56 | 11 1000b = +176 | 00 1111b = +20 | 10 0100b = +60 | 11 1001b = +180 | 01 0000b = +21 | 10 0101b = +64 | 11 1010b = +200 | 01 0001b = +22 | 10 0110b = +66 | 11 1011b = +220 | 01 0010b = +24 | 10 0111b = +70 | 11 1100b = Reserved | 01 0011b = +25 | 10 1000b = +72 | 11 1101b = Reserved | 01 0100b = +27 | 10 1001b = +80 | 11 1110b = Reserved | 01 0101b = +28 | 10 1010b = +84 | 11 1111b = Reserved |
| 00 0001b = +1 | 01 0110b = +30 | 10 1011b = +88 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0010b = +2 | 01 0111b = +32 | 10 1100b = +90 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0011b = +3 | 01 1000b = +33 | 10 1101b = +96 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0100b = +4 | 01 1001b = +35 | 10 1110b = +100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0101b = +5 | 01 1010b = +36 | 10 1111b = +108 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0110b = +6 | 01 1011b = +40 | 11 0000b = +110 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0111b = +8 | 01 1100b = +42 | 11 0001b = +112 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1000b = +9 | 01 1101b = +44 | 11 0010b = +120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1001b = +10 | 01 1110b = +45 | 11 0011b = +128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1010b = +12 | 01 1111b = +48 | 11 0100b = +132 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1011b = +14 | 10 0000b = +50 | 11 0101b = +140 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1100b = +15 | 10 0001b = +54 | 11 0110b = +144 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1101b = +16 | 10 0010b = +55 | 11 0111b = +160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1110b = +18 | 10 0011b = +56 | 11 1000b = +176 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1111b = +20 | 10 0100b = +60 | 11 1001b = +180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0000b = +21 | 10 0101b = +64 | 11 1010b = +200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0001b = +22 | 10 0110b = +66 | 11 1011b = +220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0010b = +24 | 10 0111b = +70 | 11 1100b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0011b = +25 | 10 1000b = +72 | 11 1101b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0100b = +27 | 10 1001b = +80 | 11 1110b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0101b = +28 | 10 1010b = +84 | 11 1111b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD_C | R/W | 0b | <p>Power-down Bank C: 0 = Bank C & all QC outputs powered and operate normally 1 = Bank C & all QC outputs powered-down - no active receivers should be connected to QC outputs</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC_CTL | R/W | 0b | <p>Bank C Configuration Control: 0 = NC[5:0], PD_C, EN_C, STY_Cx and AMP_Cx[1:0] settings determined by NC[1:0] control pins 1 = NC[5:0], PD_C, EN_C, STY_Cx and AMP_Cx[1:0] settings determined by register settings over I²C</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PD_QCx | R/W | 0b | <p>Power-down Output QCx: 0 = QCx output powered and operates normally 1 = QCx output powered-down - no active receivers should be connected to the QCx output. When powering-down the output bank, it is recommended to also write a '1' to the PD_QCx registers.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Bank C Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| STY_QCx | R/W | 0b | Output Style for Output QCx: 0 = QCx is LVDS 1 = QCx is LVPECL |
| AMP_QCx[1:0] | R/W | 00b | Output Amplitude for Output QCx (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 18: Bank D Control Register Bit Field Locations and Descriptions

| Bank D Control Register Block Field Locations | | | | | | | | |
|---|----------------|------|---------|----|--------------|---------|--------------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 28 | ND_FRAC[7:0] | | | | | | | |
| 29 | ND_FRAC[15:8] | | | | | | | |
| 2A | ND_FRAC[23:16] | | | | | | | |
| 2B | Rsvd | | | | ND_FINT[3:0] | | | |
| 2C | Rsvd | | ND[5:0] | | | | | |
| 2D | Rsvd | | | | ND_DIVF[1:0] | | ND_DIV | ND_SRC |
| 2E | PD_D | Rsvd | | | | | | ND_CTL |
| 2F | Rsvd | | | | | | | |
| 30 | PD_QD0 | Rsvd | | | | STY_QD0 | AMP_QD0[1:0] | |
| 31 | PD_QD1 | Rsvd | | | | | | |

| Bank D Control Register Block Field Descriptions | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|-----------------|---------------------|--|----------------|-----------------|-----------------|----------------|-----------------|-----------------|----------------|-----------------|-----------------|----------------|-----------------|------------------|----------------|-----------------|------------------|----------------|-----------------|------------------|----------------|-----------------|------------------|----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|-----------------|---------------------|-----------------|-----------------|---------------------|-----------------|-----------------|---------------------|-----------------|-----------------|---------------------|
| Bit Field Name | Field Type | Default Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ND_FRAC[23:0] | R/W | 600000h | Fractional portion of divider ratio for fractional divider for Bank D: Fraction used in divide ratio = ND_FRAC[23:0] / 2 ²⁴ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ND_FINT[3:0] | R/W | 1001b | Integer portion of divider ratio for fractional divider for Bank D: 0h - 4h= Reserved 5h - Fh = divide by the value used (e.g. 5 = divide-by-5) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ND[5:0] | R/W | 0Dh | <p>Divider ratio for Bank D: Any changes made to this register will not take effect until the INIT_CLK register bit is toggled.</p> <p>00 0000b = Reserved</p> <table border="0"> <tr> <td>00 0001b = ÷ 1</td> <td>01 0110b = ÷ 30</td> <td>10 1011b = ÷ 88</td> </tr> <tr> <td>00 0010b = ÷ 2</td> <td>01 0111b = ÷ 32</td> <td>10 1100b = ÷ 90</td> </tr> <tr> <td>00 0011b = ÷ 3</td> <td>01 1000b = ÷ 33</td> <td>10 1101b = ÷ 96</td> </tr> <tr> <td>00 0100b = ÷ 4</td> <td>01 1001b = ÷ 35</td> <td>10 1110b = ÷ 100</td> </tr> <tr> <td>00 0101b = ÷ 5</td> <td>01 1010b = ÷ 36</td> <td>10 1111b = ÷ 108</td> </tr> <tr> <td>00 0110b = ÷ 6</td> <td>01 1011b = ÷ 40</td> <td>11 0000b = ÷ 110</td> </tr> <tr> <td>00 0111b = ÷ 8</td> <td>01 1100b = ÷ 42</td> <td>11 0001b = ÷ 112</td> </tr> <tr> <td>00 1000b = ÷ 9</td> <td>01 1101b = ÷ 44</td> <td>11 0010b = ÷ 120</td> </tr> <tr> <td>00 1001b = ÷ 10</td> <td>01 1110b = ÷ 45</td> <td>11 0011b = ÷ 128</td> </tr> <tr> <td>00 1010b = ÷ 12</td> <td>01 1111b = ÷ 48</td> <td>11 0100b = ÷ 132</td> </tr> <tr> <td>00 1011b = ÷ 14</td> <td>10 0000b = ÷ 50</td> <td>11 0101b = ÷ 140</td> </tr> <tr> <td>00 1100b = ÷ 15</td> <td>10 0001b = ÷ 54</td> <td>11 0110b = ÷ 144</td> </tr> <tr> <td>00 1101b = ÷ 16</td> <td>10 0010b = ÷ 55</td> <td>11 0111b = ÷ 160</td> </tr> <tr> <td>00 1110b = ÷ 18</td> <td>10 0011b = ÷ 56</td> <td>11 1000b = ÷ 176</td> </tr> <tr> <td>00 1111b = ÷ 20</td> <td>10 0100b = ÷ 60</td> <td>11 1001b = ÷ 180</td> </tr> <tr> <td>01 0000b = ÷ 21</td> <td>10 0101b = ÷ 64</td> <td>11 1010b = ÷ 200</td> </tr> <tr> <td>01 0001b = ÷ 22</td> <td>10 0110b = ÷ 66</td> <td>11 1011b = ÷ 220</td> </tr> <tr> <td>01 0010b = ÷ 24</td> <td>10 0111b = ÷ 70</td> <td>11 1100b = Reserved</td> </tr> <tr> <td>01 0011b = ÷ 25</td> <td>10 1000b = ÷ 72</td> <td>11 1101b = Reserved</td> </tr> <tr> <td>01 0100b = ÷ 27</td> <td>10 1001b = ÷ 80</td> <td>11 1110b = Reserved</td> </tr> <tr> <td>01 0101b = ÷ 28</td> <td>10 1010b = ÷ 84</td> <td>11 1111b = Reserved</td> </tr> </table> <p>NOTE: QD1 CMOS output should be powered-off or disabled for output frequencies greater than the maximum listed for it in Table 28.</p> | 00 0001b = ÷ 1 | 01 0110b = ÷ 30 | 10 1011b = ÷ 88 | 00 0010b = ÷ 2 | 01 0111b = ÷ 32 | 10 1100b = ÷ 90 | 00 0011b = ÷ 3 | 01 1000b = ÷ 33 | 10 1101b = ÷ 96 | 00 0100b = ÷ 4 | 01 1001b = ÷ 35 | 10 1110b = ÷ 100 | 00 0101b = ÷ 5 | 01 1010b = ÷ 36 | 10 1111b = ÷ 108 | 00 0110b = ÷ 6 | 01 1011b = ÷ 40 | 11 0000b = ÷ 110 | 00 0111b = ÷ 8 | 01 1100b = ÷ 42 | 11 0001b = ÷ 112 | 00 1000b = ÷ 9 | 01 1101b = ÷ 44 | 11 0010b = ÷ 120 | 00 1001b = ÷ 10 | 01 1110b = ÷ 45 | 11 0011b = ÷ 128 | 00 1010b = ÷ 12 | 01 1111b = ÷ 48 | 11 0100b = ÷ 132 | 00 1011b = ÷ 14 | 10 0000b = ÷ 50 | 11 0101b = ÷ 140 | 00 1100b = ÷ 15 | 10 0001b = ÷ 54 | 11 0110b = ÷ 144 | 00 1101b = ÷ 16 | 10 0010b = ÷ 55 | 11 0111b = ÷ 160 | 00 1110b = ÷ 18 | 10 0011b = ÷ 56 | 11 1000b = ÷ 176 | 00 1111b = ÷ 20 | 10 0100b = ÷ 60 | 11 1001b = ÷ 180 | 01 0000b = ÷ 21 | 10 0101b = ÷ 64 | 11 1010b = ÷ 200 | 01 0001b = ÷ 22 | 10 0110b = ÷ 66 | 11 1011b = ÷ 220 | 01 0010b = ÷ 24 | 10 0111b = ÷ 70 | 11 1100b = Reserved | 01 0011b = ÷ 25 | 10 1000b = ÷ 72 | 11 1101b = Reserved | 01 0100b = ÷ 27 | 10 1001b = ÷ 80 | 11 1110b = Reserved | 01 0101b = ÷ 28 | 10 1010b = ÷ 84 | 11 1111b = Reserved |
| 00 0001b = ÷ 1 | 01 0110b = ÷ 30 | 10 1011b = ÷ 88 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0010b = ÷ 2 | 01 0111b = ÷ 32 | 10 1100b = ÷ 90 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0011b = ÷ 3 | 01 1000b = ÷ 33 | 10 1101b = ÷ 96 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0100b = ÷ 4 | 01 1001b = ÷ 35 | 10 1110b = ÷ 100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0101b = ÷ 5 | 01 1010b = ÷ 36 | 10 1111b = ÷ 108 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0110b = ÷ 6 | 01 1011b = ÷ 40 | 11 0000b = ÷ 110 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 0111b = ÷ 8 | 01 1100b = ÷ 42 | 11 0001b = ÷ 112 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1000b = ÷ 9 | 01 1101b = ÷ 44 | 11 0010b = ÷ 120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1001b = ÷ 10 | 01 1110b = ÷ 45 | 11 0011b = ÷ 128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1010b = ÷ 12 | 01 1111b = ÷ 48 | 11 0100b = ÷ 132 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1011b = ÷ 14 | 10 0000b = ÷ 50 | 11 0101b = ÷ 140 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1100b = ÷ 15 | 10 0001b = ÷ 54 | 11 0110b = ÷ 144 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1101b = ÷ 16 | 10 0010b = ÷ 55 | 11 0111b = ÷ 160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1110b = ÷ 18 | 10 0011b = ÷ 56 | 11 1000b = ÷ 176 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 1111b = ÷ 20 | 10 0100b = ÷ 60 | 11 1001b = ÷ 180 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0000b = ÷ 21 | 10 0101b = ÷ 64 | 11 1010b = ÷ 200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0001b = ÷ 22 | 10 0110b = ÷ 66 | 11 1011b = ÷ 220 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0010b = ÷ 24 | 10 0111b = ÷ 70 | 11 1100b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0011b = ÷ 25 | 10 1000b = ÷ 72 | 11 1101b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0100b = ÷ 27 | 10 1001b = ÷ 80 | 11 1110b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 0101b = ÷ 28 | 10 1010b = ÷ 84 | 11 1111b = Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ND_DIVF[1:0] | R/W | 00b | <p>Post-divider ratio for fractional divider for Bank D:</p> <p>00 = ÷1 01 = ÷2 10 = ÷4 11 = Reserved</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Bank D Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|--|
| ND_DIV | R/W | 0b | Control which divider is used to provide output frequency for Bank D: 0 = Integer divider D (ND configures this) 1 = Fractional mode (ND_FINT, ND_FRAC and ND_DIVF configure this) |
| ND_SRC | R/W | 0b | Output Source Selection for Bank D: 0 = Bank D is driven from the integer or fractional divider as selected by ND_SRC 1 = Bank D is driven from the input reference (after the mux) with f_{IN} |
| PD_D | R/W | 0b | Power-down Bank D: 0 = Bank D & all QD outputs powered and operate normally 1 = Bank D & all QD outputs powered-down - no active receivers should be connected to QD0 output. QD1 output is in High-Impedance. |
| ND_CTL | R/W | 0b | Bank D Configuration Control: 0 = ND[5:0], ND_FRAC[23:0], ND_FINT[3:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, EN_D, STY_D0 and AMP_D0[1:0] settings determined by ND[1:0] control pins 1 = ND[5:0], ND_FRAC[23:0], ND_FINT[3:0], ND_DIVF[1:0], ND_DIV, ND_SRC, PD_D, EN_D, STY_D0 and AMP_D0[1:0] settings determined by register settings over I ² C |
| PD_QDx | R/W | 0b | Power-down Output QDx: 0 = QD[0:1] outputs powered and operate normally 1 = QD0 output powered-down - no active receivers should be connected to the QD0 output, QD1 output is in High-Impedance. When powering-down the output bank, it is recommended to also write a '1' to the PD_QDx registers. |
| STY_QD0 | R/W | 0b | Output Style for Output QD0: 0 = QD0 is LVDS 1 = QD0 is LVPECL |
| AMP_QD0[1:0] | R/W | 00b | Output Amplitude for Output QD0 (measured single-ended): 00 = 350mV 01 = 500mV 10 = 750mV 11 = Reserved |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 19: Device Control Register Bit Field Locations and Descriptions

| Device Control Register Block Field Locations | | | | | | | | |
|---|----------|----|----|----|------|------|------|------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 3D | INIT_CLK | | | | | | | Rsvd |
| 3E | RELOCK | | | | | | | Rsvd |
| 3F | PB_CAL | | | | | | | Rsvd |
| 40 | | | | | EN_A | EN_B | EN_C | EN_D |

| Device Control Register Block Field Descriptions | | | |
|--|------------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| INIT_CLK | W/O ^a | 0b | Writing a '1' to this bit location will cause output dividers to be synchronized. Must be done every time a divider value is changed if output divider synchronization is desired. This bit will auto-clear after output divider synchronization is completed. |
| RELOCK | W/O ^a | 0b | Writing a '1' to this bit location will cause the PLL to re-lock. This bit will auto-clear. |
| PB_CAL | W/O ^a | 0b | Precision Bias Calibration: Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS and for as reference for the charge pump currents. This bit will auto-clear after the calibration is completed. |
| EN_A | R/W | 1b | Output Enable control for Bank A: 0 = Bank A outputs QA[0:3] disabled to logic-low state (QA _x = 0, nQA _x = 1) 1 = Bank A outputs QA[0:3] enabled |
| EN_B | R/W | 1b | Output Enable control for Bank B: 0 = Bank B outputs QB[0:3] disabled to logic-low state (QB _x = 0, nQB _x = 1) 1 = Bank B outputs QB[0:3] enabled |
| EN_C | R/W | 1b | Output Enable control for Bank C: 0 = Bank C outputs QC[0:1] disabled to logic-low state (QC _x = 0, nQC _x = 1) 1 = Bank C outputs QC[0:1] enabled |
| EN_D | R/W | 1b | Output Enable control for Bank D: 0 = Bank D outputs QD[0:1] disabled to logic-low state (QD ₀ = 0, nQD ₀ = 1, QD ₁ = 0) Note that if Bank D is powered down via the PD_D bit or the QD1 output is powered down by the PD_QD1 bit, then QD1 will be in High-Impedance regardless of the state of this bit. 1 = Bank D outputs QD[0:1] enabled |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

a. These bits are read as '0'. When a '1' is written to them, it will have the indicated effect and then self-clear back to '0'.

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 20: Absolute Maximum Ratings

| Item | Rating |
|--|--------------------------------|
| Supply Voltage, V_{CC} | 3.6V |
| Inputs, V_I OSCI Other Inputs | -0.5V to 3.6V -0.5V to 3.6V |
| Outputs, V_O (LVCMOS) | -0.5V to 3.6V |
| Outputs, I_O (LVPECL) Continuous Current Surge Current | 50mA 100mA |
| Outputs, I_O (LVDS) Continuous Current Surge Current | 50mA 100mA |
| Maximum Junction Temperature, t_{JMAX} | 125°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 21: Power Supply DC Characteristics, $V_{CC_X}^a = V_{CCOX}^b = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$,

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|------------------------------|--------|--|---------|---------|---------|-------|
| V_{CC_X} | Core Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA_X}^c$ | Analog Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| V_{CCOX} | Output Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| $I_{CC_X}^d$ | Core Supply Current | LVPECL | All Outputs Enabled & Terminated ^e | | 73 | 100 | mA |
| | | LVDS | All Outputs Enabled & Terminated ^f | | 73 | 100 | mA |
| $I_{CCA_X}^g$ | Analog Supply Current | LVPECL | All Outputs Enabled & Terminated ^e | | 141 | 169 | mA |
| | | LVDS | All Outputs Enabled & Terminated ^f | | 141 | 167 | mA |
| I_{CCOA}^h | Bank A Output Supply Current | LVPECL | 350mV, Outputs Enabled & Terminated ^e | | 189 | 226 | mA |
| | | | 500mV, Outputs Enabled & Terminated ^e | | 183 | 217 | mA |
| | | | 750mV, Outputs Enabled & Terminated ^e | | 172 | 205 | mA |
| | | LVDS | 350mV, Outputs Enabled & Terminated ^f | | 84 | 103 | mA |
| | | | 500mV, Outputs Enabled & Terminated ^f | | 101 | 124 | mA |
| | | | 750mV, Outputs Enabled & Terminated ^f | | 130 | 161 | mA |
| | | LVPECL | 350mV, Outputs Disabled & Unterminated | | 8 | 10 | mA |
| | | | 500mV, Outputs Disabled & Unterminated | | 10 | 12 | mA |
| | | | 750mV, Outputs Disabled & Unterminated | | 12 | 15 | mA |
| | | LVDS | 350mV, Outputs Disabled & Unterminated | | 26 | 32 | mA |
| | | | 500mV, Outputs Disabled & Unterminated | | 36 | 43 | mA |
| | | | 750mV, Outputs Disabled & Unterminated | | 51 | 62 | mA |

Table 21: Power Supply DC Characteristics, $V_{CC_X}^a = V_{CCOX}^b = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$, Cont.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | | | | |
|--------------|------------------------------|-----------------|--|--|---------|--|-----|----|----|----|
| I_{CCOB}^h | Bank B Output Supply Current | LVPECL | 350mV, Outputs Enabled & Terminated ^e | | 196 | 234 | mA | | | |
| | | | 500mV, Outputs Enabled & Terminated ^e | | 188 | 224 | mA | | | |
| | | | 750mV, Outputs Enabled & Terminated ^e | | 177 | 211 | mA | | | |
| | | LVDS | | 350mV, Outputs Enabled & Terminated ^f | | 86 | 105 | mA | | |
| | | | | 500mV, Outputs Enabled & Terminated ^f | | 103 | 126 | mA | | |
| | | | | 750mV, Outputs Enabled & Terminated ^f | | 132 | 163 | mA | | |
| | | LVPECL | | 350mV, Outputs Disabled & Unterminated | | 9 | 11 | mA | | |
| | | | | 500mV, Outputs Disabled & Unterminated | | 10 | 13 | mA | | |
| | | | | 750mV, Outputs Disabled & Unterminated | | 13 | 16 | mA | | |
| | | | | LVDS | | 350mV, Outputs Disabled & Unterminated | | 27 | 33 | mA |
| | | | | | | 500mV, Outputs Disabled & Unterminated | | 36 | 44 | mA |
| | | | | | | 750mV, Outputs Disabled & Unterminated | | 52 | 62 | mA |
| I_{CCOC}^h | Bank C Output Supply Current | LVPECL | 350mV, Outputs Enabled & Terminated ^e | | 109 | 131 | mA | | | |
| | | | 500mV, Outputs Enabled & Terminated ^e | | 106 | 127 | mA | | | |
| | | | 750mV, Outputs Enabled & Terminated ^e | | 100 | 120 | mA | | | |
| | | LVDS | | 350mV, Outputs Enabled & Terminated ^f | | 55 | 67 | mA | | |
| | | | | 500mV, Outputs Enabled & Terminated ^f | | 64 | 78 | mA | | |
| | | | | 750mV, Outputs Enabled & Terminated ^f | | 78 | 95 | mA | | |
| | | LVPECL | | 350mV, Outputs Disabled & Unterminated | | 1 | 2 | mA | | |
| | | | | 500mV, Outputs Disabled & Unterminated | | 1 | 2 | mA | | |
| | | | | 750mV, Outputs Disabled & Unterminated | | 1 | 2 | mA | | |
| | | | | LVDS | | 350mV, Outputs Disabled & Unterminated | | 1 | 2 | mA |
| | | | | | | 500mV, Outputs Disabled & Unterminated | | 1 | 2 | mA |
| | | | | | | 750mV, Outputs Disabled & Unterminated | | 1 | 2 | mA |

Table 21: Power Supply DC Characteristics, $V_{CC_X}^a = V_{CCOX}^b = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$, Cont.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|--------------|-----------------------------------|-----------------|--|---------|---------|-------|----|
| I_{CCOD}^h | Bank D Output Supply Current | LVPECL | 350mV, Outputs Enabled & Terminated ^e | | 91 | 114 | mA |
| | | | 500mV, Outputs Enabled & Terminated ^e | | 89 | 112 | mA |
| | | | 750mV, Outputs Enabled & Terminated ^e | | 86 | 109 | mA |
| | | LVDS | 350mV, Outputs Enabled & Terminated ^f | | 57 | 69 | mA |
| | | | 500mV, Outputs Enabled & Terminated ^f | | 62 | 75 | mA |
| | | | 750mV, Outputs Enabled & Terminated ^f | | 70 | 85 | mA |
| | | LVPECL | 350mV, Outputs Disabled & Unterminated | | 3 | 5 | mA |
| | | | 500mV, Outputs Disabled & Unterminated | | 3 | 5 | mA |
| | | | 750mV, Outputs Disabled & Unterminated | | 3 | 5 | mA |
| | | LVDS | 350mV, Outputs Disabled & Unterminated | | 3 | 5 | mA |
| | | | 500mV, Outputs Disabled & Unterminated | | 3 | 5 | mA |
| | | | 750mV, Outputs Disabled & Unterminated | | 3 | 5 | mA |
| I_{EE}^h | Power Supply Current for V_{EE} | LVPECL | 350mV, Outputs Enabled & Terminated ^e | | 385 | 470 | mA |
| | | | 500mV, Outputs Enabled & Terminated ^e | | 394 | 481 | mA |
| | | | 750mV, Outputs Enabled & Terminated ^e | | 407 | 497 | mA |
| | | LVPECL | 350mV, Outputs Disabled & Unterminated | | 233 | 277 | mA |
| | | | 500mV, Outputs Disabled & Unterminated | | 236 | 280 | mA |
| | | | 750mV, Outputs Disabled & Unterminated | | 241 | 286 | mA |

a. V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

b. V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

c. V_{CCA_X} denotes V_{CCA_IN1} , V_{CCA_IN2} , V_{CCA} , V_{CCA_XT} .

d. I_{CC_X} denotes I_{CC_CP} , I_{CC_CK} , I_{CC_SP} .

e. Differential outputs terminated 50Ω to $V_{CCOX} - 2V$. QD1 output terminated 50Ω to $V_{CCOD}/2$.

f. Differential outputs terminated 100Ω across Q and nQ. QD1 output terminated 50Ω to $V_{CCOD}/2$.

g. I_{CCA_X} denotes I_{CCA_IN1} , I_{CCA_IN2} , I_{CCA} , I_{CCA_XT} .

h. Internal maximum dynamic switching current is included.

Table 22: LVCMOS DC Characteristics for 3-level Pins, $V_{CC_X}^a = V_{CCOX}^b = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|--|----------------------------------|------------------|---------|------------------|---------|
| V_{IH} | Input High Voltage | | | $0.7 * V_{CC}^c$ | | 3.465 | V |
| V_{IM} | Input Middle Voltage | FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0] | | $0.4 * V_{CC}^c$ | | $0.6 * V_{CC}^c$ | V |
| V_{IL} | Input Low Voltage | | | -0.3 | | $0.3 * V_{CC}^c$ | V |
| I_{IH} | Input High Current | FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0] | $V_{CC}^c = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IM} | Input Middle Current | FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0] | $V_{IN} = V_{CC}^c / 2$ | | ± 1 | | μA |
| I_{IL} | Input Low Current | FIN[1:0], NA[1:0], NB[1:0], NC[1:0], ND[1:0] | $V_{CC}^c = 3.465V, V_{IN} = 0V$ | -150 | | | μA |

a. V_{CC_X} denotes $V_{CC_CP}, V_{CC_CK}, V_{CC_SP}$.

b. V_{CCOX} denotes $V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCOD}$.

c. V_{CC} denotes V_{CCA_IN1}, V_{CC_CK} .

Table 23: LVCMOS DC Characteristics for 2-level Pins, $V_{CC_X}^a = V_{CCOX}^b = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|-------------|----------------------------------|------------------|---------|-------------------|---------|
| V_{IH} | Input High Voltage | | | $0.7 * V_{CC}^c$ | | 3.465 | V |
| V_{IL} | Input Low Voltage | REF_SEL | | -0.3 | | $0.3 * V_{CC}^c$ | V |
| | | SDATA, SCLK | | -0.3 | | $0.15 * V_{CC}^c$ | V |
| I_{IH} | Input High Current | SCLK, SDATA | $V_{CC}^c = V_{IN} = 3.465V$ | | | 5 | μA |
| | | REF_SEL | $V_{CC}^c = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | SCLK, SDATA | $V_{CC}^c = 3.465V, V_{IN} = 0V$ | -150 | | | μA |
| | | REF_SEL | $V_{CC}^c = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| V_{OH} | Output High Voltage | LOCK | $I_{OH} = -4mA$ | 2.2 | | | V |
| V_{OL} | Output Low Voltage | SDATA, LOCK | $I_{OL} = 4mA$ | | | 0.45 | V |

a. V_{CC_X} denotes $V_{CC_CP}, V_{CC_CK}, V_{CC_SP}$.

b. V_{CCOX} denotes $V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCOD}$.

c. V_{CC} denotes V_{CC_CK} .

Table 24: Differential Input DC Characteristics, $V_{CC_X}^a = V_{CCOX}^b = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|--|----------------|---------|------------------|---------|
| I_{IH} | Input High Current | CLK_IN, nCLK_IN $V_{CC}^c = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLK_IN $V_{CC}^c = 3.465V, V_{IN} = 0V$ | -5 | | | μA |
| | | nCLK_IN $V_{CC}^c = 3.465V, V_{IN} = 0V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Voltage ^{d, e} | CLK_IN, nCLK_IN | 0.2 | | 1.4 | V |
| V_{CMR} | Common Mode Input Voltage ^{d, e} | CLK_IN, nCLK_IN | $V_{EE} + 1.1$ | | $V_{CC}^c - 0.3$ | V |

a. V_{CC_X} denotes $V_{CC_CP}, V_{CC_CK}, V_{CC_SP}$.

b. V_{CCOX} denotes $V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCOD}$.

c. V_{CC} denotes V_{CC_CK} .

d. Common mode voltage is defined as the cross point.

e. Input voltage cannot be less than $V_{EE} - 300mV$ or more than V_{CC} .

Table 25: LVPECL Output DC Characteristics (Qmn^a), $V_{CC_X}^b = V_{CCOX}^c = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|--|-------------------------|------------------|---------|------------------|-------|
| V_{OH} | Output High Voltage ^d | 350mV Amplitude setting | $V_{CCOX} - 1.1$ | | $V_{CCOX} - 0.8$ | V |
| | | 500mV Amplitude setting | $V_{CCOX} - 1.1$ | | $V_{CCOX} - 0.8$ | |
| | | 750mV Amplitude setting | $V_{CCOX} - 1.1$ | | $V_{CCOX} - 0.8$ | |
| V_{OL} | Output Low Voltage ^d | 350mV Amplitude setting | $V_{CCOX} - 1.5$ | | $V_{CCOX} - 1.1$ | V |
| | | 500mV Amplitude setting | $V_{CCOX} - 1.6$ | | $V_{CCOX} - 1.3$ | |
| | | 750mV Amplitude setting | $V_{CCOX} - 1.8$ | | $V_{CCOX} - 1.5$ | |
| V_{SWING} | Single-ended Peak-to-Peak Output Voltage Swing | 350mV Amplitude setting | 280 | 350 | 420 | mV |
| | | 500mV Amplitude setting | 430 | 500 | 570 | |
| | | 750mV Amplitude setting | 630 | 700 | 770 | |

a. In this table, Qmn denotes the differential outputs QA[0:3], QB[0:3], QC[0:1] or QD0. Note that QD1 is not included because it is not differential.

b. V_{CC_X} denotes $V_{CC_CP}, V_{CC_CK}, V_{CC_SP}$.

c. V_{CCOX} denotes $V_{CCOA}, V_{CCOB}, V_{CCOC}, V_{CCOD}$.

d. Outputs terminated with 50Ω to $V_{CCOX} - 2V$.

Table 26: LVDS Output DC Characteristics (Q_{mn}^a), $V_{CC_X}^b = V_{CCOX}^c = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------------|-------------------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | 350mV Amplitude setting | 0.27 | 0.32 | 0.37 | V |
| | | 500mV Amplitude setting | 0.39 | 0.46 | 0.53 | |
| | | 750mV Amplitude setting | 0.62 | 0.69 | 0.76 | |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage ^{d, e, f} | 350mV Amplitude setting | 1.9 | 2.3 | 2.7 | V |
| | | 500mV Amplitude setting | 1.8 | 2.2 | 2.6 | |
| | | 750mV Amplitude setting | 1.7 | 2.1 | 2.5 | |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

a. In this table, Q_{mn} denotes the differential outputs QA[0:3], QB[0:3], QC[0:1] or QD0. Note that QD1 is not included because it is not differential.

b. V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

c. V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

d. No external DC pulldown resistor.

e. Loading condition is with 100Ω across the differential output.

f. Offset voltage (V_{OS}) changes with supply voltage V_{CCOX} .

Table 27: Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 10 | | 50 | MHz |
| Equivalent Series Resistance (ESR) | $C_L = 12pF$ | | | 60 | Ω |
| | $C_L = 18pF$ | | 15 | 30 | Ω |
| Load Capacitance (C_L) | | | 12 | | pF |
| Maximum Crystal Drive Level | | | 200 | | μW |
| Frequency Stability (total) | | -100 | | 100 | ppm |

AC Electrical Characteristics

Table 28: AC Characteristics, ^a $V_{CC_X}^b = V_{CCOX}^c = 3.3V+5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|-----------------------------|--------------------------------------|---|---|---------|---------|-------|-----|
| f_{VCO} | VCO Frequency | | 2400 | | 2500 | MHz | |
| f_{PFD} | Phase / Frequency Detector Frequency | | 5 | | 200 | MHz | |
| f_{OUT} | Output Frequency | QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1] | 10.91 | | 2500 | MHz | |
| | | QD0, nQD0 | Integer Divider Selected | | 10.91 | 2500 | MHz |
| | | | Fractional Divider Selected | | 20 | 138 | MHz |
| | | QD1 | Integer Divider Selected | | 10.91 | 250 | MHz |
| Fractional Divider Selected | | | 20 | 138 | MHz | | |
| $t_{sk}(b)$ | Bank Skew ^{d, e, f} | Bank A | Same Frequency and Output Type Only valid for skew between outputs in the same bank | | 45 | ps | |
| | | Bank B | | 45 | | | |
| | | Bank C | | 20 | | | |
| t_R / t_F | Output Rise/Fall Time | QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1] | 30% to 70% | 30 | 60 | 110 | ps |
| | | QD0, nQD0 | 30% to 70% | 30 | 90 | 200 | |
| | | QD1 | 30% to 70% | 220 | 375 | 600 | |
| odc | Output Duty Cycle ^g | QA[0:3] nQA[0:3] QB[0:3] nQB[0:3] QC[0:1] nQC[0:1], QD0, nQD0 | $F_{OUT} \leq 1250MHz$ | 45 | 50 | 55 | % |
| | | | $F_{OUT} > 1250MHz$ | 40 | 50 | 60 | % |
| | | QD1 | $F_{OUT} < 156.25MHz$ | 45 | 50 | 55 | % |
| | | | $F_{OUT} \geq 156.25MHz$ | 40 | 50 | 60 | % |
| t_{LOCK} | PLL Lock Time ^h | | | 40 | 100 | ms | |

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

c. V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

d. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

e. This parameter is defined in accordance with JEDEC Standard 65.

f. This parameter is guaranteed by characterization. Not tested in production

g. Duty Cycle of bypassed signals (input reference clock or crystal input) is not adjusted by the device.

h. PLL Lock Time is defined as time from input clock availability to frequency locked output. The following loop filter component values may be used: $R_Z = 221\Omega$, $C_Z = 4.7\mu F$, $C_P = 30pf$. Refer to [Applications Information](#).

Table 29: Qmn^a and QD1 Phase Noise and Jitter Characteristics, $V_{CC_X}^b = V_{CCOX}^c = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ ^{d, e, f, g, h, i}

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------|---|---|----------------------------------|---------|---------|---------|--------|
| $f_{jit}(\emptyset)^j$ | RMS Phase Jitter Random | Qmn = 156.25MHz ^k | Integration Range: 12kHz – 20MHz | | 87 | 110 | fs |
| | RMS Phase Jitter Random | Qmn = 125MHz | Integration Range: 12kHz – 20MHz | | 84 | | fs |
| | RMS Phase Jitter Random | Qmn = 100MHz | Integration Range: 12kHz – 20MHz | | 94 | | fs |
| | RMS Phase Jitter Random | Qmn = 25MHz | Integration Range: 12kHz – 5MHz | | 126 | | fs |
| | RMS Phase Jitter Random | QD0 = 133.33MHz (fractional) ^l | Integration Range: 12kHz – 20MHz | | 180 | | fs |
| | RMS Phase Jitter Random | QD1 = 125MHz | Integration Range: 12kHz – 20MHz | | 170 | | fs |
| | RMS Phase Jitter Random ^m | QAn = 125MHz | Integration Range: 12kHz – 20MHz | | 85 | | fs |
| | | QBn = 100MHz | Integration Range: 12kHz – 20MHz | | 88 | | fs |
| QCn = 25MHz | | Integration Range: 12kHz – 5MHz | | 137 | | fs | |
| QD0 = 133.33MHz (fractional) | | Integration Range: 12kHz – 20MHz | | 170 | | fs | |
| $\Phi_N(10)^n$ | Single-Side Band Noise Power, 10Hz from Carrier | | Qmn = 156.25MHz | | -75.1 | | dBc/Hz |
| $\Phi_N(100)^n$ | Single-Side Band Noise Power, 100Hz from Carrier | | Qmn = 156.25MHz | | -109.6 | | dBc/Hz |
| $\Phi_N(1k)^n$ | Single-Side Band Noise Power, 1kHz from Carrier | | Qmn = 156.25MHz | | -128.9 | | dBc/Hz |
| $\Phi_N(10k)^n$ | Single-Side Band Noise Power, 10kHz from Carrier | | Qmn = 156.25MHz | | -137.6 | | dBc/Hz |
| $\Phi_N(100k)^n$ | Single-Side Band Noise Power, 100kHz from Carrier | | Qmn = 156.25MHz | | -143.0 | | dBc/Hz |
| $\Phi_N(1M)^n$ | Single-Side Band Noise Power, 1MHz from Carrier | | Qmn = 156.25MHz | | -157.5 | | dBc/Hz |
| $\Phi_N(10M)^n$ | Single-Side Band Noise Power, 10MHz from Carrier | | Qmn = 156.25MHz | | -163.1 | | dBc/Hz |
| $\Phi_N(\infty)^n$ | Noise Floor (≥ 30 MHz from Carrier) | | Qmn = 156.25MHz | | -163.1 | | dBc/Hz |

a. In this table, Qmn denotes the differential outputs QA[0:3], QB[0:3], QC[0:1] or QD0. Note that QD1 is not included because it is not differential.

b. V_{CC_X} denotes V_{CC_CP} , V_{CC_CK} , V_{CC_SP} .

c. V_{CCOX} denotes V_{CCOA} , V_{CCOB} , V_{CCOC} , V_{CCOD} .

d. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

e. All outputs enabled and configured for the same output frequency unless otherwise noted.

f. Characterized using a 50MHz, $C_L = 18$ pF crystal, unless otherwise noted.

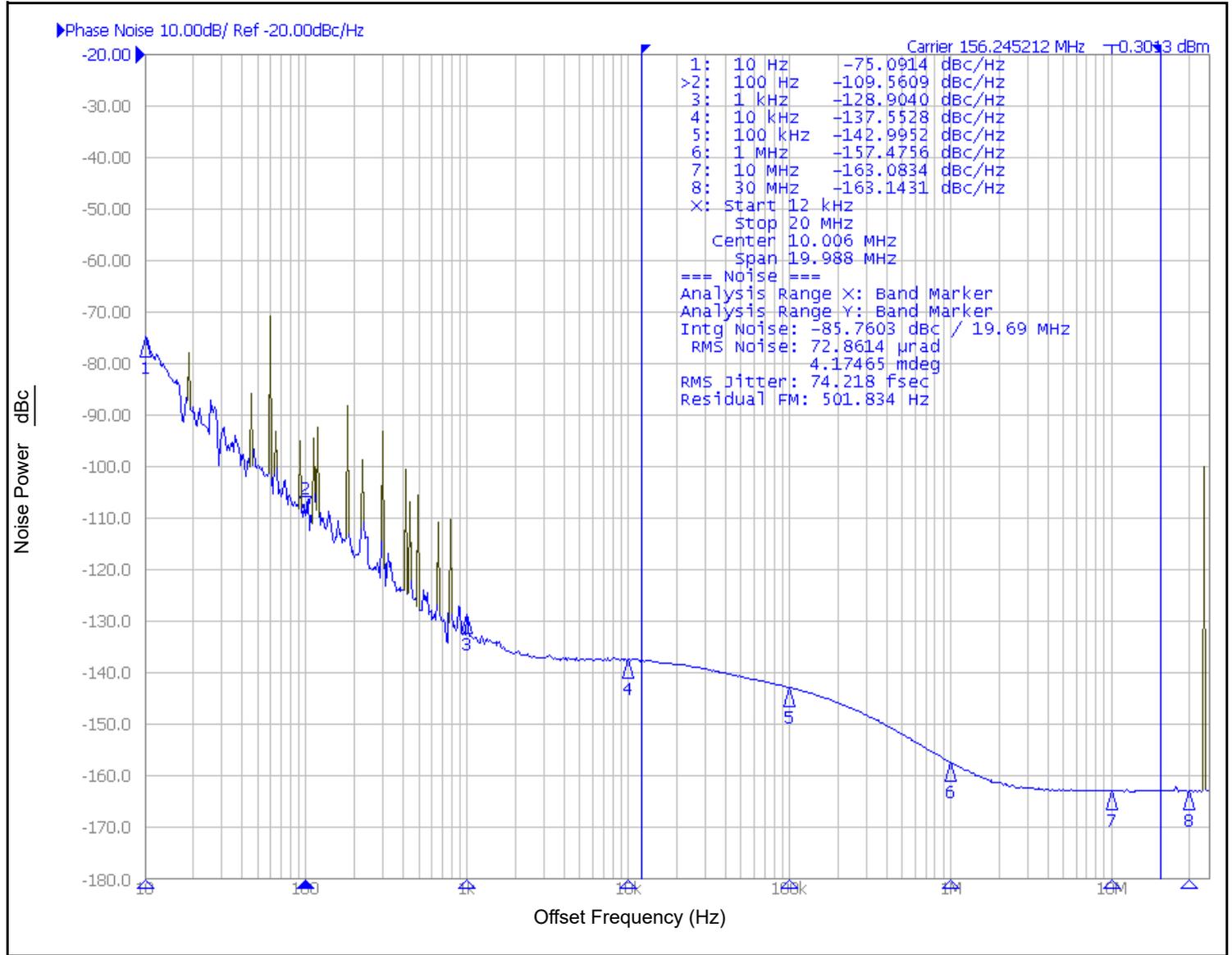
g. Measured on Qmn configured as ± 16 and ± 20 .

h. V_{CCA} requires a voltage regulator. Voltage supplied to V_{CCA} should be derived from a regulator with a typical power supply rejection ratio of 80dB at 1kHz and ultra low noise generation with a typical value of 3nV/ \sqrt{Hz} at 10kHz and 7nV/ \sqrt{Hz} at 1kHz.

i. Characterized with 750mV output voltage swing configuration for all differential outputs.

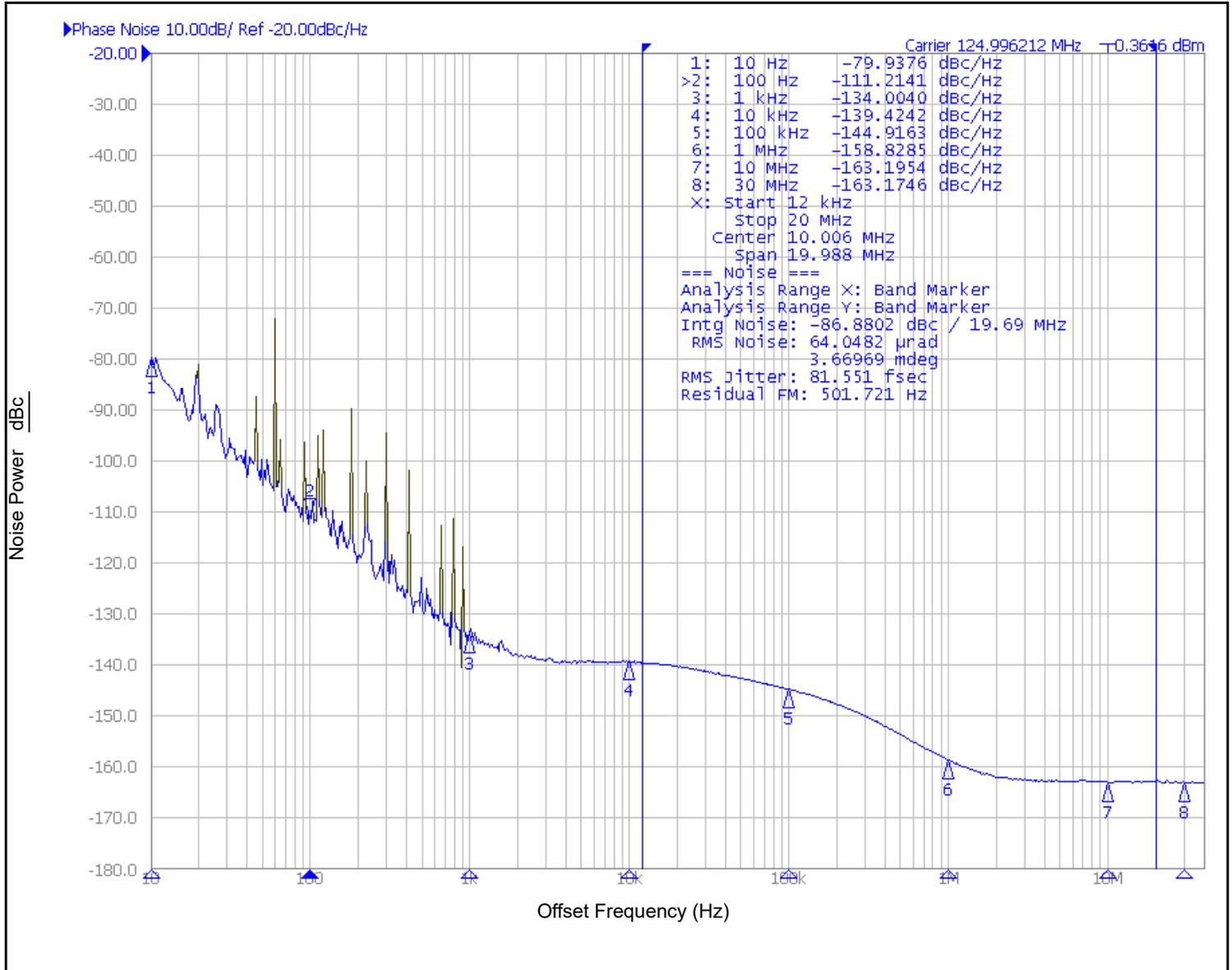
- j. The following loop filter component values were used: $R_Z = 221\Omega$, $C_Z = 4.7\mu\text{F}$, $CP = 30\text{pF}$. PLL Charge Pump Current Control set at 5.2mA.
- k. Characterized using a 31.25MHz, $C_L = 18\text{pF}$ crystal, (FOX P/N FX277LF-31.25-1).
- l. $QAx = 156.25\text{MHz}$, $QBx = 156.25\text{MHz}$, $QCx = 156.25\text{MHz}$.
- m. $QAx = 156.25\text{MHz}$, $QBx = 100\text{MHz}$, $QCx = 25\text{MHz}$, $QD0 = 133.33\text{MHz}$ (fractional).
- n. Measured using a 50MHz, 12pF crystal as input reference. The following loop filter components were used: $R_Z = 150\Omega$, $C_Z = 0.1\mu\text{F}$, $CP = 200\text{pF}$. PLL Charge Pump Current Control set at 6.4mA.

Typical Phase Noise at 156.25MHz^a



a: Measured using a 50MHz, 12pF crystal as input reference. The following loop filter components were used: $R_Z = 150\Omega$, $C_Z = 0.1\mu\text{F}$, $CP = 200\text{pF}$. PLL Charge Pump Current Control set at 6.4mA.

Typical Phase Noise at 125MHz^a



a. Measured using a 50MHz, 12pF crystal as input reference. The following loop filter components were used: $R_z = 150\Omega$, $C_z = 0.1\mu F$, $C_P = 200pF$. PLL Charge Pump Current Control set at 6.4mA.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pull-up and/or pull-down resistors; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs should be left floating. It is recommended that there is no trace attached.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating there should be no trace attached.

LVC MOS Outputs

QD1 output can be left floating if unused. There should be no trace attached.

Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals 90Ω . In addition, matched termination at the crystal input will further attenuate the signal. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω . This can also be accomplished by removing R_1 and changing R_2 to 50Ω . The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

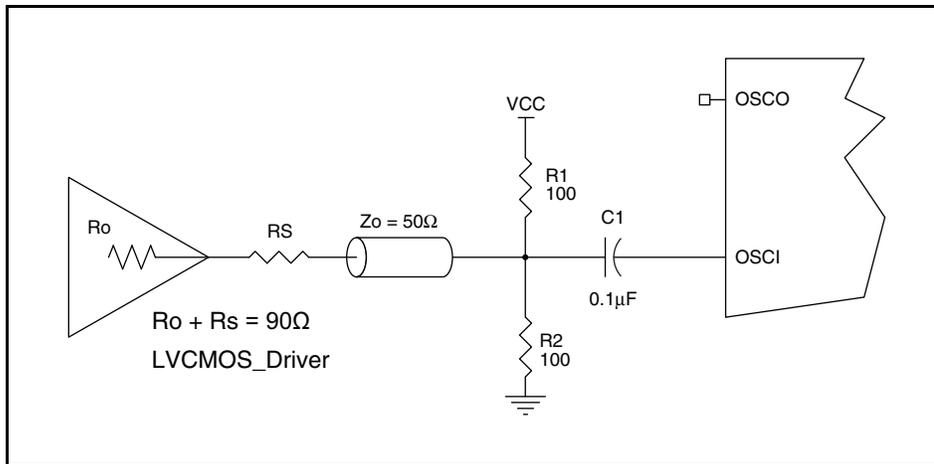


Figure 3: General Diagram for LVCMOS Driver to XTAL Input Interface

Figure 4 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSCI input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

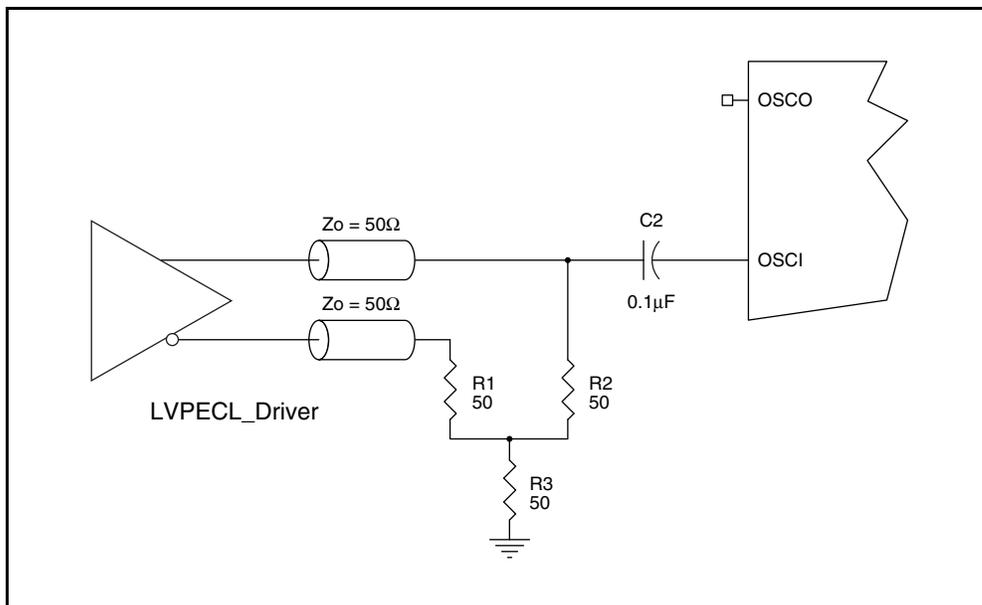


Figure 4: General Diagram for LVPECL Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single-Ended Levels

Figure 5 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than $-0.3V$ and V_{IH} cannot be more than $V_{CC} + 0.3V$. Suggested edge rate faster than $1V/ns$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

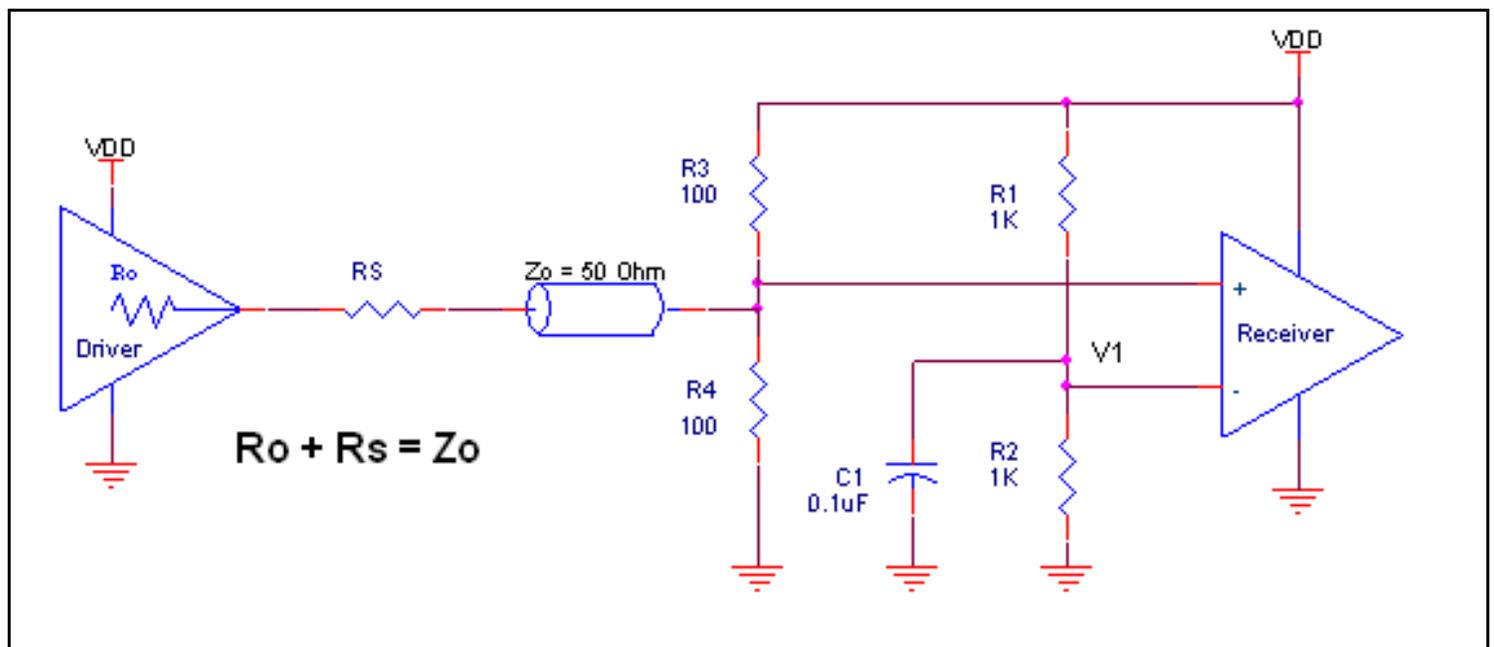


Figure 5: Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

CLK/nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 6* to *Figure 10* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 6*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

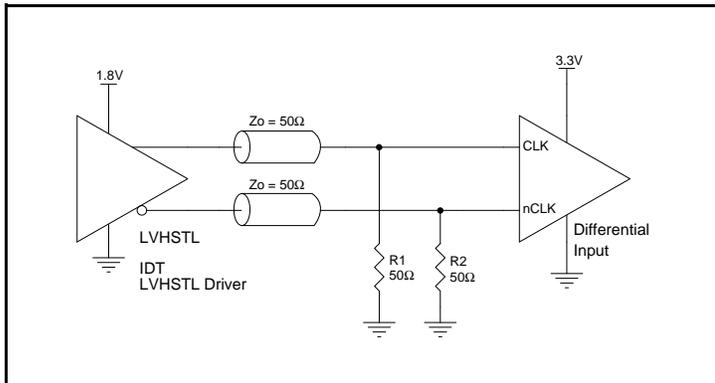


Figure 6: CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

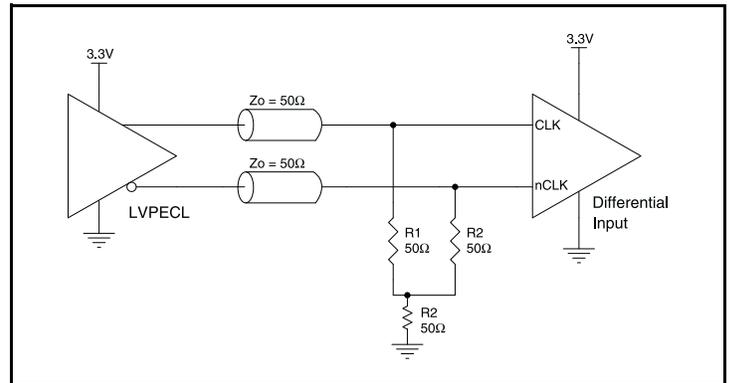


Figure 9: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

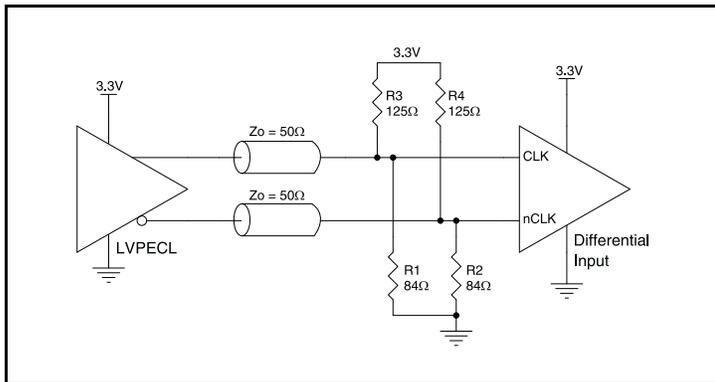


Figure 7: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

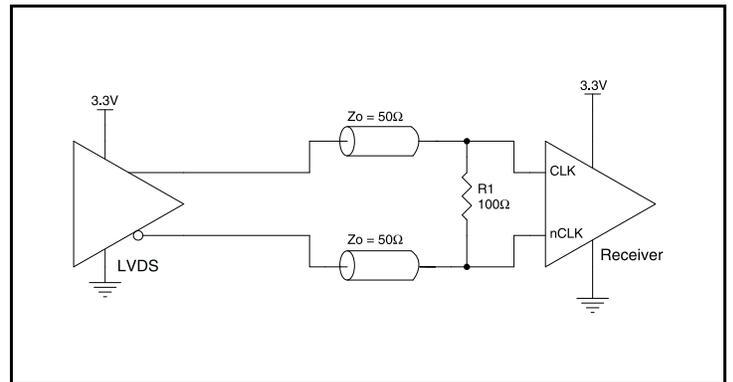


Figure 10: CLK/nCLK Input Driven by a 3.3V LVDS Driver

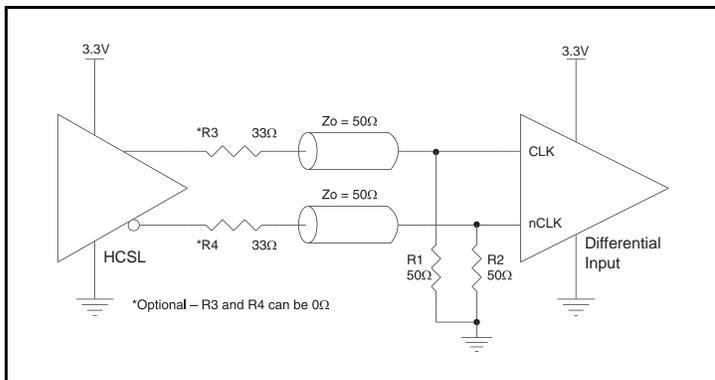


Figure 8: CLK/nCLK Input Driven by a 3.3V HCSL Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in [Figure 11](#) can be used with either type of output structure. [Figure 12](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Refer to [Figure 13](#), [Figure 14](#) and [Figure 15](#) for additional details on the recommended termination schemes.

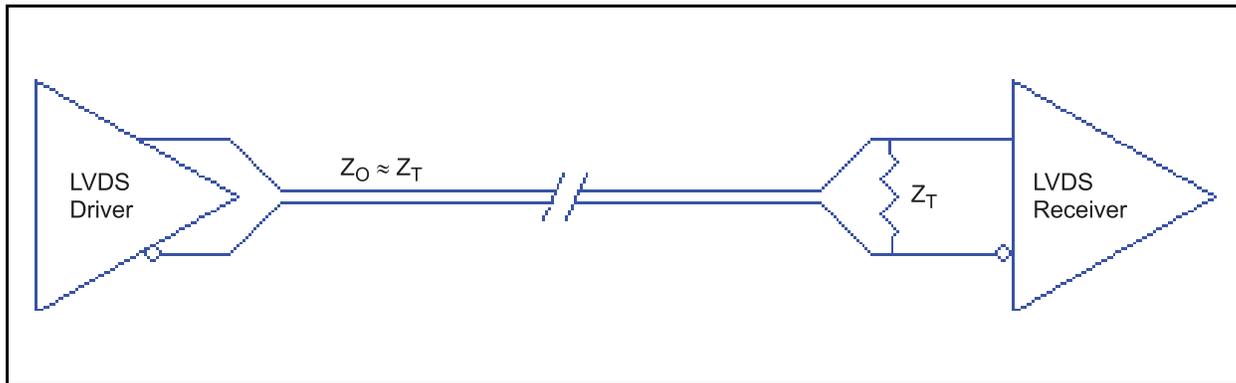


Figure 11: Standard LVDS Termination

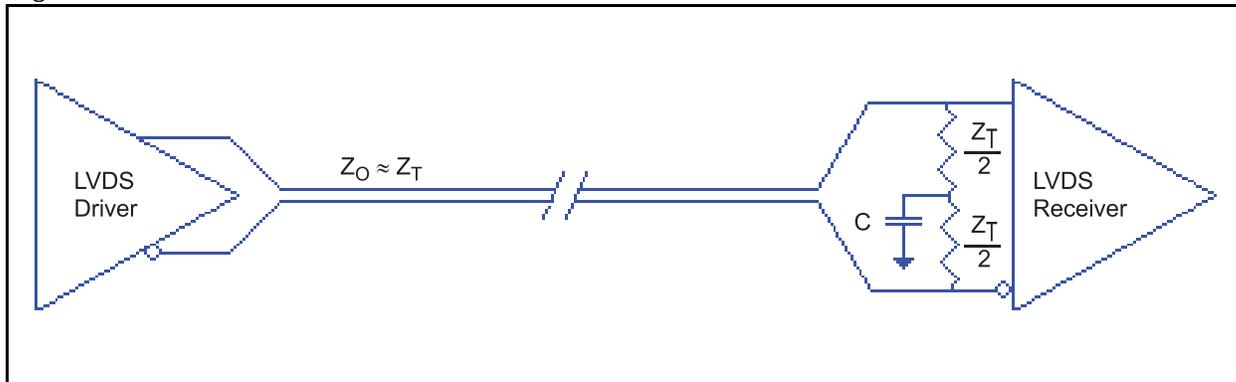


Figure 12: Optional LVDS Termination

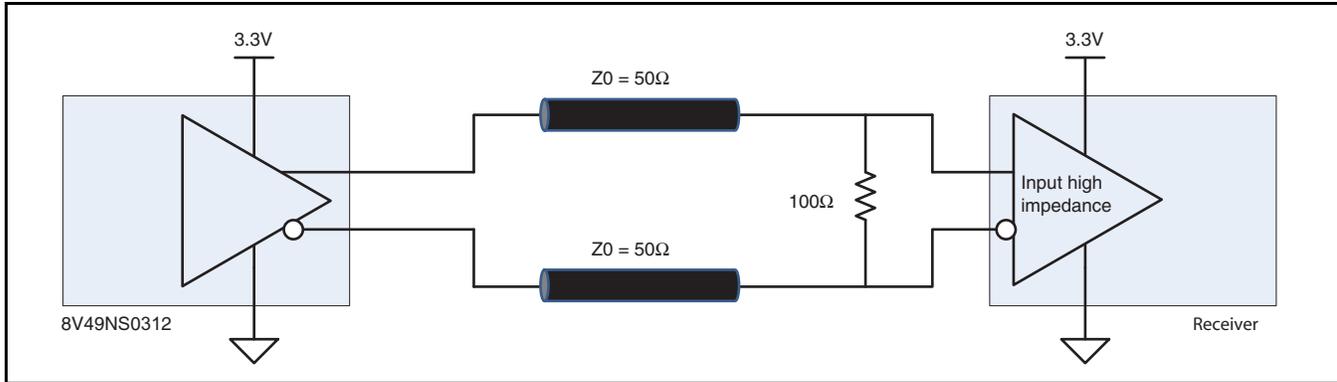


Figure 13: DC Termination for LVDS Outputs

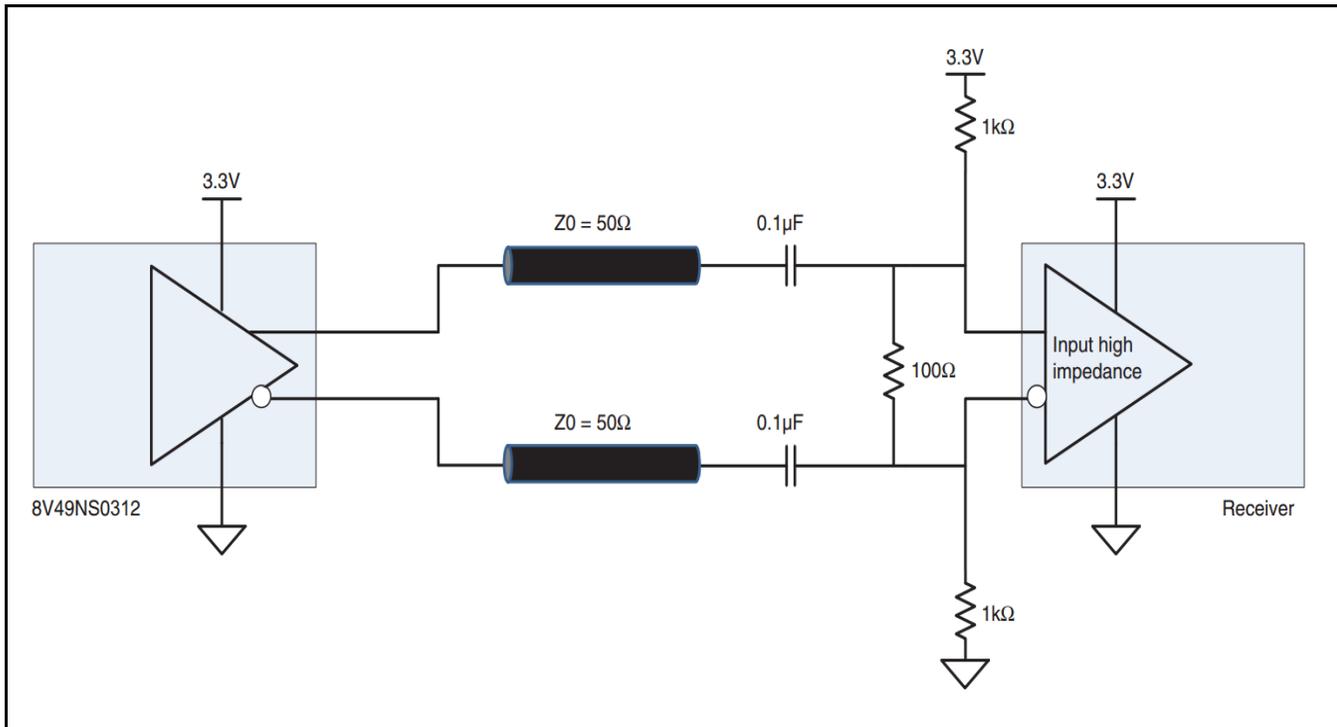


Figure 14: AC Termination for LVDS Outputs

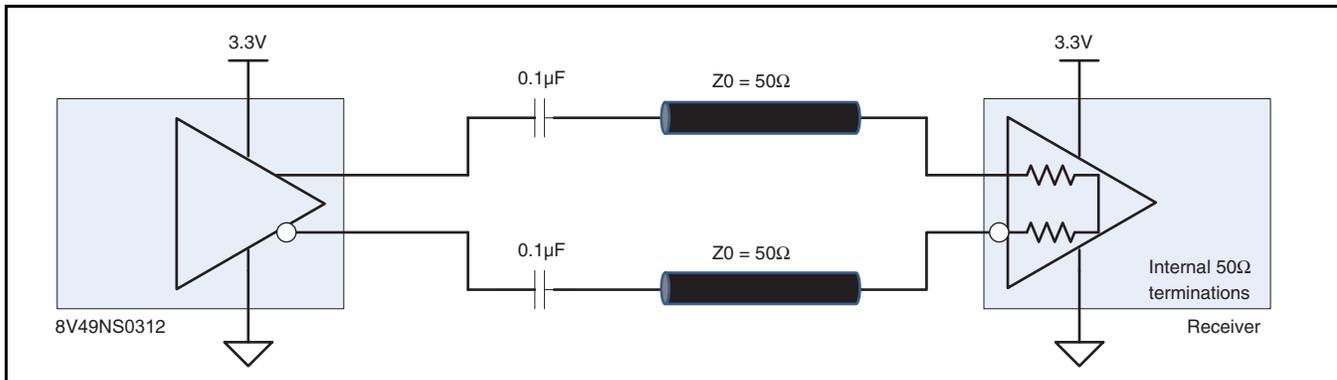


Figure 15: AC Termination for LVDS outputs used with an Input Clock Receiver with Internal 50Ω Terminations and DC Bias.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize

operating frequency and minimize signal distortion. *Figure 16 and Figure 17* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

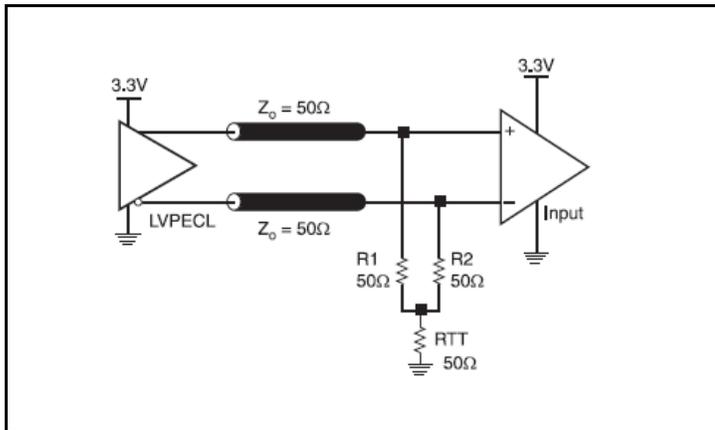


Figure 16: 3.3V LVPECL Output Termination

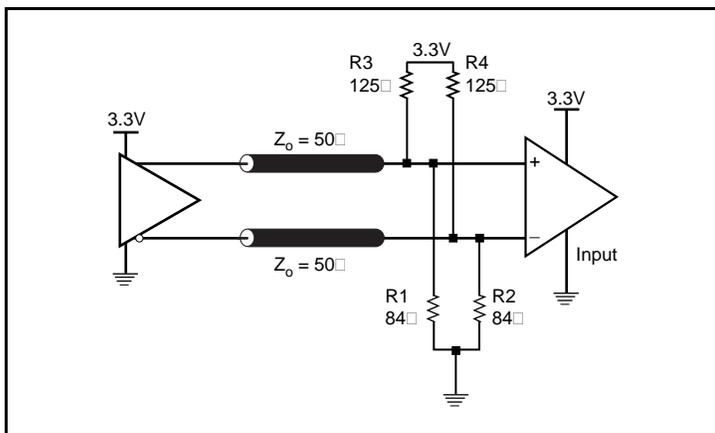


Figure 17: 3.3V LVPECL Output Termination

Figure 16 and *Figure 19* show two different LVPECL termination schemes for 750mV amplitude setting which are recommended only as guidelines. Recommended values of R1/R2/R3/R4 for LVPECL termination (*Figure 19*; Thevenin Equivalent) for 350mV and 500mV amplitude settings can be found in the following table.

Table 1. LVPECL Output Termination, $V_{CCOX} = 3.3V \pm 5\%$

| Test Conditions | Bias Voltage | R1 [Ω] | R2 [Ω] | R3 [Ω] | R4 [Ω] |
|-------------------------|--------------------|--------|--------|--------|--------|
| 350mV Amplitude Setting | $V_{CCOX} - 1.6V$ | 105 | 105 | 97.6 | 97.6 |
| 500mV Amplitude Setting | $V_{CCOX} - 1.75V$ | 95.3 | 95.3 | 107 | 107 |
| 750mV Amplitude Setting | $V_{CCOX} - 2.0V$ | 84 | 84 | 125 | 125 |

With a fast ramp up VDD, power-up to lock time is:

- When CR (pin 25) = 1.0uF, typical lock time is around 108ms
- When CR (pin 25) = 0.1uF, typical lock time is around 30ms

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in [Figure 18](#). The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

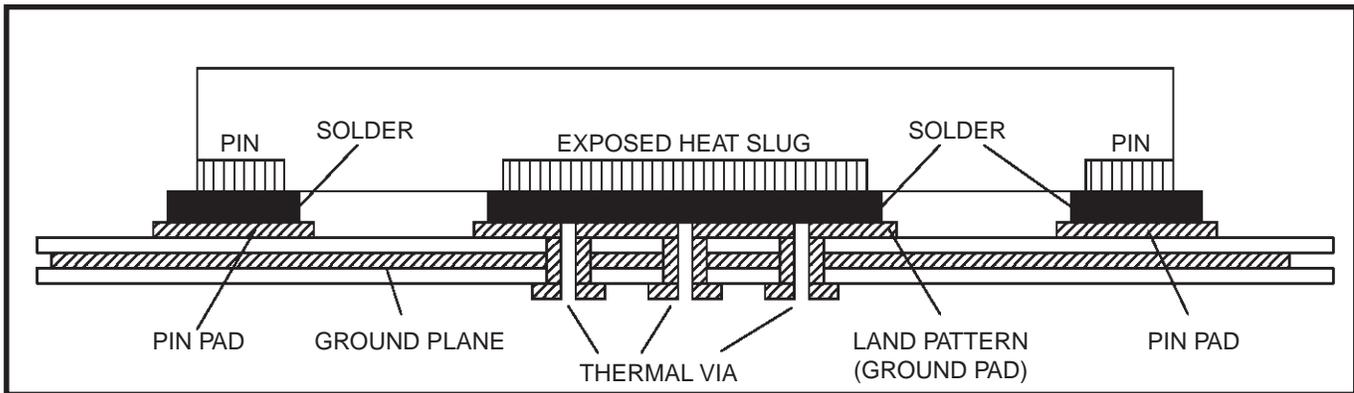


Figure 18: P.C. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Layout

Figure 19 shows an example 8V49NS0312 application schematic operating the device at $V_{CC} = 3.3V$. This example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

To demonstrate the range of output stage configurations possible, the application schematic assumes that the 8V49NS0312 is programmed over I²C. For alternative DC coupled LVPECL options please see IDT Application Note, AN-828; for AC coupling options use IDT Application Note, AN-844.

For a 12pF parallel resonant crystal, tuning capacitors C145 and C146 are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C145 and C146. For this device, the crystal tuning capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I²C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I²C transition times are short enough to capacitively couple into the crystal-oscillator loop if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the OSC1 and OSC0 pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 8V49NS0312. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 8V49NS0312 as possible as shown in the schematic.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V49NS0312 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. The ferrite bead and the 0.1uF capacitor in each power pin filter should always be placed on the device side of the board. The other components can be on the opposite side of the PCB if space on the top side is limited. Pull up and pull down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. Depending on the application, the filter may need to be adjusted to get a lower cutoff frequency to adequately attenuate low-frequency noise. Additionally, good general design practices for power plane voltage stability suggest adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

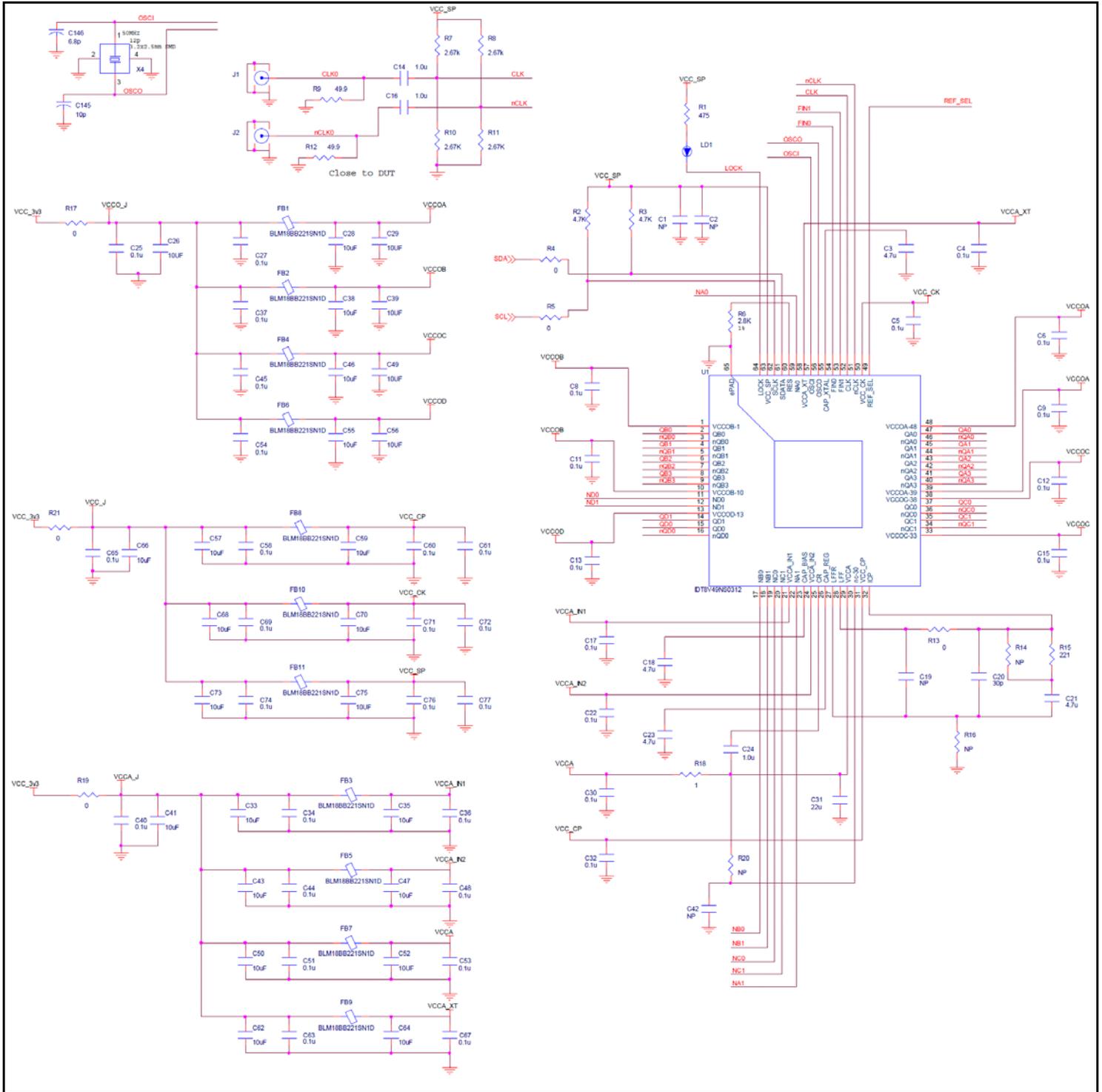


Figure 19: 8V49NS0312 Application Schematic

Power Dissipation and Thermal Considerations

The 8V49NS0312 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The 8V49NS0312 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Example 1. LVPECL, 750mV Output Swing

This section provides information on power dissipation and junction temperature when the device differential outputs are configured for LVPECL level, 750mV output swing. Equations and example calculations are also provided.

Table 30: Power Calculations Configuration #1

| Output | Output Style | Output Swing |
|--------|--------------|--------------|
| QA0 | LVPECL | 750mV |
| QA1 | LVPECL | 750mV |
| QA2 | LVPECL | 750mV |
| QA3 | LVPECL | 750mV |
| QB0 | LVPECL | 750mV |
| QB1 | LVPECL | 750mV |
| QB2 | LVPECL | 750mV |
| QB3 | LVPECL | 750mV |
| QC0 | LVPECL | 750mV |
| QC1 | LVPECL | 750mV |
| QD0 | LVPECL | 750mV |
| QD1 | LVC MOS | N/A |

1a. Power Dissipation.

The total power dissipation is the sum of the core power plus the power dissipated due to output loading. The following is the power dissipation for $V_{CC} = 3.465V$, which gives worst case results.

- $\text{Power}(\text{core})_{\text{MAX}} = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 497mA = 1722.1mW$
- $\text{Power}(\text{LVPECL outputs})_{\text{MAX}} = 34.2mW/\text{Loaded Output pair}$. Refer to [Section 1c](#).
If all outputs are loaded, the total power is $11 * 34.2mW = 376.2mW$
- $\text{Power}(\text{LVC MOS output})_{\text{MAX}}$ (Power dissipation due to loading 50Ω to $V_{CCO} / 2$)
Output Current: $I_{OUT} = V_{CCOD_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 30\Omega)] = 21.66mA$
Power Dissipation on the R_{OUT} : $\text{Power}(R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 30\Omega * (21.66mA)^2 = 14.07mW$
- $\text{Total Power}_{\text{MAX}} = \text{Power}(\text{core}) + \text{Power}(\text{LVPECL outputs}) + \text{Power}(\text{LVC MOS output})$
 $= 1722.1mW + 376.2mW + 14.07mW = 2112.37mW = 2.112W$

1b. Junction Temperature.

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = T_A + P_D * \theta_{JA}$:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation (W) in desired operating configuration

θ_{JA} = Junction-to-Ambient Thermal Resistance

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance must be used. Assuming no air flow and a multi-layer board, the appropriate value is 15.6°C/W per [Table 32](#).

Therefore, assuming $T_A = 85^\circ\text{C}$ and all outputs switching, T_J will be:

$$85^\circ\text{C} + 2.112\text{W} * 15.6^\circ\text{C/W} = 117.95^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

1c. Power Dissipation due to output loading.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in [Figure 20](#).

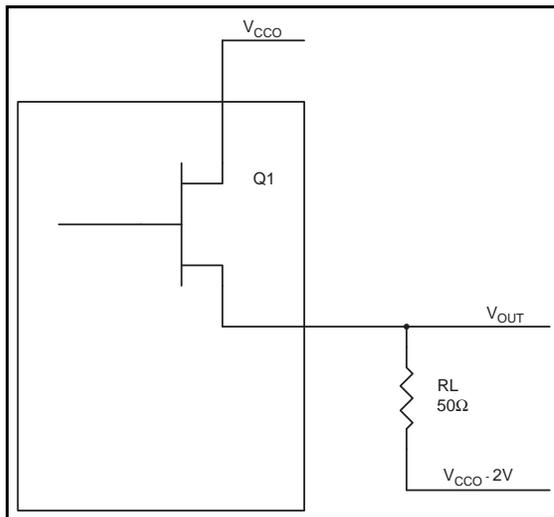


Figure 20: LVPECL Driver Circuit and Termination

To calculate worst case power dissipation at the output(s), use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCOX} - 2V$. These are typical calculations.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCOX_MAX} - 0.8V$
 $(V_{CCOX_MAX} - V_{OH_MAX}) = 0.8V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCOX_MAX} - 1.5V$
 $(V_{CCOX_MAX} - V_{OL_MAX}) = 1.5V$

P_{d_H} is the power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCOX_MAX} - 2V))/R_L] * (V_{CCOX_MAX} - V_{OH_MAX}) = [(2V - (V_{CCOX_MAX} - V_{OH_MAX}))/R_L] * (V_{CCOX_MAX} - V_{OH_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = 19.2mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCOX_MAX} - 2V))/R_L] * (V_{CCOX_MAX} - V_{OL_MAX}) = [(2V - (V_{CCOX_MAX} - V_{OL_MAX}))/R_L] * (V_{CCOX_MAX} - V_{OL_MAX}) = [(2V - 1.5V)/50\Omega] * 1.5V = 15mW$$

Total Power Dissipation per output pair = Pd_H + Pd_L = 34.2mW

Example 2. LVDS, 350mV Output Swing

This section provides information on power dissipation and junction temperature when the device differential outputs are configured for LVDS levels, 350mV output swing. Equations and example calculations are also provided.

Table 31: Power Calculations Configuration #2

| Output | Output Style | Output Swing |
|--------|--------------|--------------|
| QA0 | LVDS | 350mV |
| QA1 | LVDS | 350mV |
| QA2 | LVDS | 350mV |
| QA3 | LVDS | 350mV |
| QB0 | LVDS | 350mV |
| QB1 | LVDS | 350mV |
| QB2 | LVDS | 350mV |
| QB3 | LVDS | 350mV |
| QC0 | LVDS | 350mV |
| QC1 | LVDS | 350mV |
| QD0 | LVDS | 350mV |
| QD1 | LVC MOS | N/A |

2a. Power Dissipation.

The total power dissipation is the sum of the core power plus the power dissipation due to output loading.

The following is the power dissipation for $V_{CCX} = V_{CCA_X} = V_{CCOX} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- $$Power_{MAX} = V_{CCX_MAX} * I_{CCX_MAX} + V_{CCA_X_MAX} * I_{CCA_X_MAX} + V_{CCOX_MAX} * I_{CCOX_MAX}$$

$$= 3.465V * 100mA + 3.465V * 167mA + 3.465V (103mA + 105mA + 67mA + 69mA)$$

$$= 346.5mW + 578.66mW + 1191.96mW = 2117.12mW = 2.117W$$

2b. Junction Temperature.

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = T_A + P_D * \theta_{JA}$:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation (W) in desired operating configuration

θ_{JA} = Junction-to-Ambient Thermal Resistance

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance must be used. Assuming no air flow and a multi-layer board, the appropriate value is 15.6°C/W per [Table 32](#).

Therefore, assuming $T_A = 85^\circ\text{C}$ and all outputs switching, T_J will be:

$$85^\circ\text{C} + 2.117\text{W} * 15.6^\circ\text{C/W} = 118.03^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Reliability Information

Table 32: Thermal Resistance Table for 64-pin VFQFN Package

| Symbol | Thermal Parameter | Condition | Value | Unit |
|-----------------|---------------------|-------------|-------|------|
| θ_{JA}^a | Junction-to-Ambient | No air flow | 15.6 | °C/W |
| θ_{JC} | Junction-to-Case | | 15.3 | °C/W |
| θ_{JB} | Junction-to-Board | | 0.6 | °C/W |

a. Theta J_A (θ_{JA}) values calculated using an 8-layer PCB (114.3mm x 101.6mm), with 2oz. (70µm) copper plating on all 8 layers, with ePad connected to 4 ground planes.

Transistor Count

The transistor count for the 8V49NS0312 is: 143,063

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

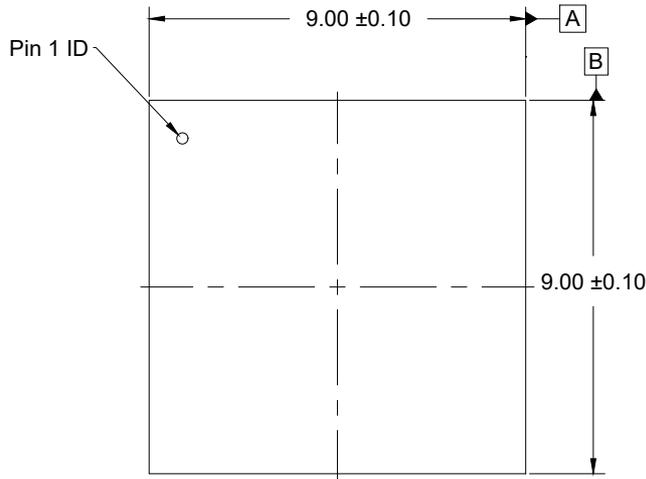
www.idt.com/document/psc/64-vfqfn-package-outline-drawing-90-x-90-x-09-mm-body-05mm-pitch-epad-60-x-60-mm-nlg64p5

Ordering Information

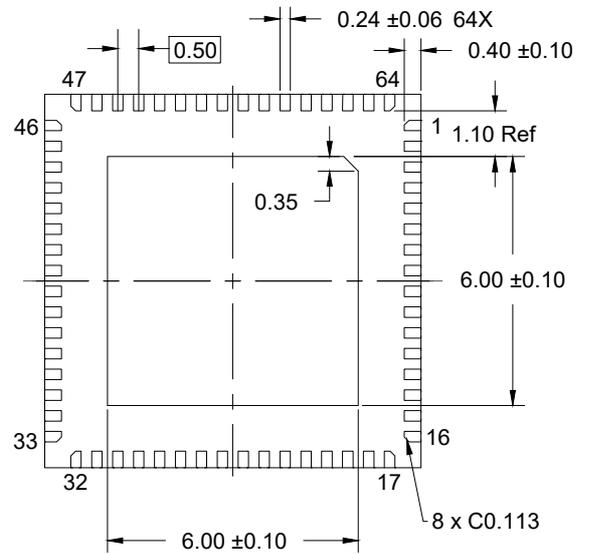
| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|-------------------|----------------------|--------------------|----------------|
| 8V49NS0312NLGI | IDT8V49NS0312NLGI | 64-VFQFPN, Lead-Free | Tray | -40°C to +85°C |
| 8V49NS0312NLGI8 | IDT8V49NS0312NLGI | 64-VFQFPN, Lead-Free | Tape & Reel | -40°C to +85°C |

Revision History

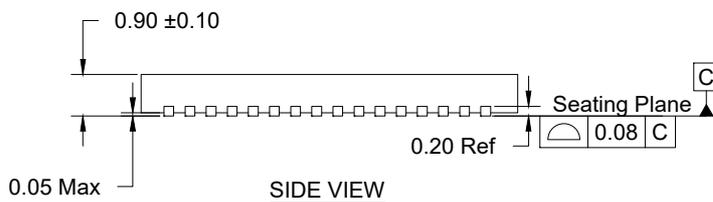
| Revision Date | Description of Change |
|-------------------|---|
| April 24, 2019 | <ul style="list-style-type: none"> ▪ Updated Overdriving the XTAL Interface ▪ Updated Termination for 3.3V LVPECL Outputs ▪ Updated the Package Outline Drawings; however, no mechanical changes |
| November 14, 2017 | <ul style="list-style-type: none"> ▪ Updated the QD fractional output divider's maximum frequency to 138MHz to meet period jitter compliance (see Table 28) ▪ Updated the Package Outline Drawings; however, no mechanical changes ▪ Completed other minor changes |
| September 2, 2016 | Page 32, Table 27 Crystal Characteristics - added additional spec to Equivalent Series Resistance row. |
| August 1, 2016 | Page 50, Power Dissipation due to output loading . - typographical error replaced "-" with "=": For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCOX_MAX} - 1.5V$, $(V_{CCOX_MAX} - V_{OL_MAX}) = 1.5V$. |
| July 11, 2016 | Initial release. |



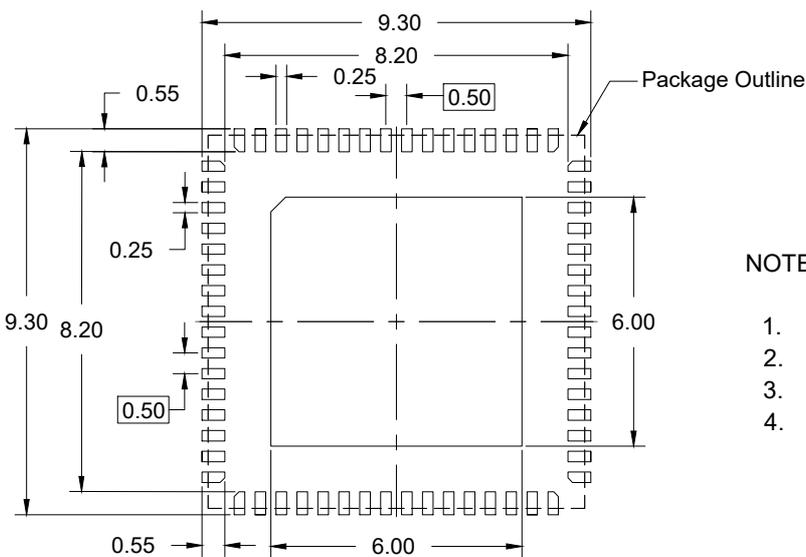
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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