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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR 2SK4075B

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4075B is N-channel MOS FET designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4075B-ZK-E1-AY	Pure Sn (Tin)	Tape	TO-2 <mark>52 (MP-</mark> 3ZK)
2SK4075B-ZK-E2-AY		2500 p/reel	typ. 0.27 g

FEATURES

Low on-state resistance

 $R_{DS(on)1} = 7.9 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, Ip} = 25 \text{ A)}$

 $R_{DS(on)2} = 10 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = 4.5 \text{ V, I}_D = 13 \text{ A)}$

• Low Ciss: Ciss = 2230 pF TYP.

Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±50	Α
Drain Current (pulse) Note1	ID(pulse)	±120	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	36	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current Note2	las	20.8	Α
Single Avalanche Energy Note2	Eas	43	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	3.47	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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ELECTRICAL CHARACTERISTICS (TA = 25°C)

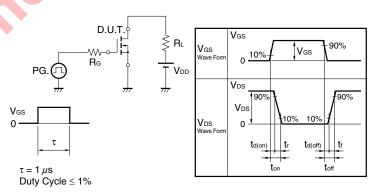
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			1	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 13 A	7.0			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 25 A		5.9	7.9	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 13 A		7.5	10	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		2230		pF
Output Capacitance	Coss	V _{GS} = 0 V		319		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		171		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V		15		ns
Rise Time	t r	lo = 25 A		17		ns
Turn-off Delay Time	t d(off)	V _{GS} = 10 V		51		ns
Fall Time	t _f	$R_G = 0 \Omega$		5		ns
Total Gate Charge	Q _G	V _{DD} = 32 V		44		nC
Gate to Source Charge	Qgs	V _{GS} = 10 V		8		nC
Gate to Drain Charge	Q _{GD}	I _D = 50 A		12		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 50 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	IF = 50 A, VGS = 0 V		30		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A /μs		25		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

TEST CIRCUIT 2 SWITCHING TIME

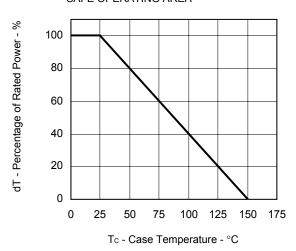


TEST CIRCUIT 3 GATE CHARGE

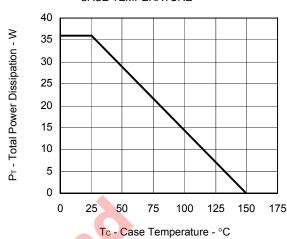


TYPICAL CHARACTERISTICS (TA = 25°C)

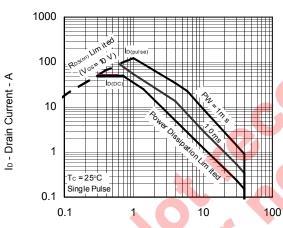
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



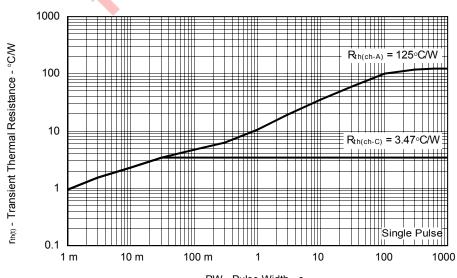
FORWARD BIAS SAFE OPERATING AREA



V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

11.1.065



PW - Pulse Width - s

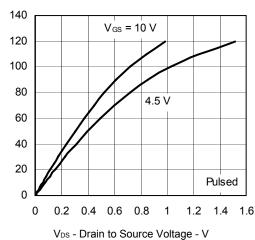
3



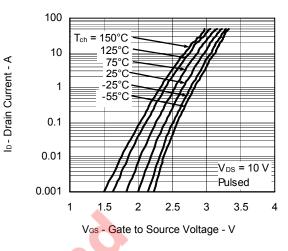
Ip - Drain Current - A

VGS(off) - Gate Cut-off Voltage - V

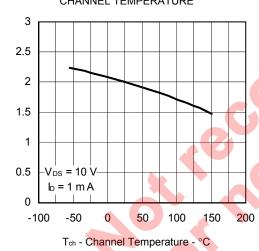
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



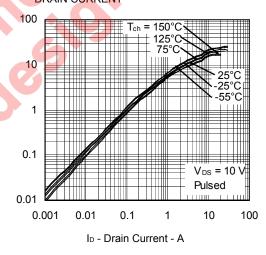
FORWARD TRANSFER CHARACTERISTICS



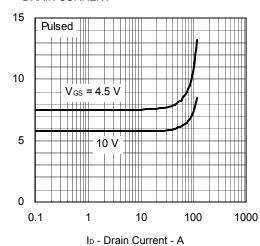
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



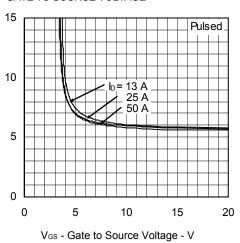
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATERESISTANCE vs. GATE TO SOURCE VOLTAGE



 $\mathsf{R}_{\mathsf{DS}(m)}$ - Drain to Source On-state Resistance - $m\Omega$

S

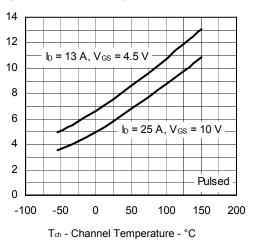
| yfs | - Forward Transfer Admittance -

 $R_{DS(m)}$ - Drain to Source On-state Resistance - $m\Omega$

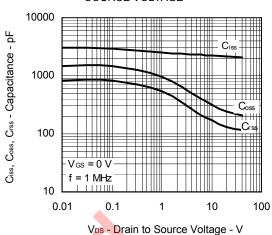




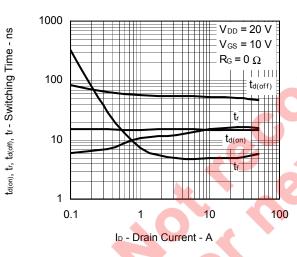
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



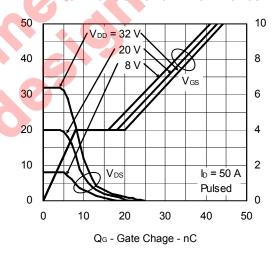
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



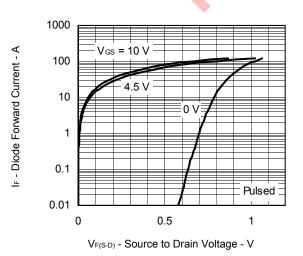
SWITCHING CHARACTERISTICS



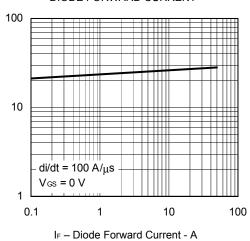
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



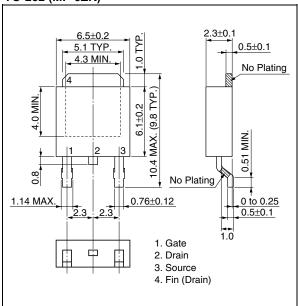
Vps - Drain to Source Voltage -

tr - Reverse Recovery Time - ns

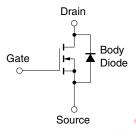


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



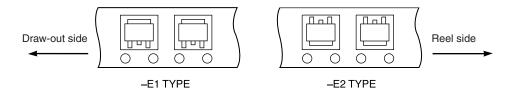
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

6

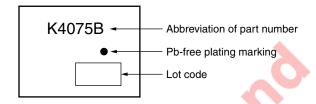


TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The 2SK4075B should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

Data Sheet D20258EJ1V0DS 7

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