To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

DATA SHEET

MOS FIELD EFFECT TRANSISTOR
2SK4075B

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4075B is N-channel MOS FET designed for high current switching applications.

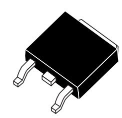
ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4075B-ZK-E1-AY	Pure Sn (Tin)	Tape	TO-252 (MP-3ZK)
2SK4075B-ZK-E2-AY		2500 p/reel	typ. 0.27 g

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 7.9 mΩ MAX. (V_{GS} = 10 V, I_D = 25 A)
  $R_{DS(on)2}$ = 10 mΩ MAX. (V_{GS} = 4.5 V, I_D = 13 A)
- Low C_{iss}: C_{iss} = 2230 pF TYP.
- Logic level drive type

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±50	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±120	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	36	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	20.8	A
Single Avalanche Energy Note2	E_{AS}	43	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 20 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	3.47	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

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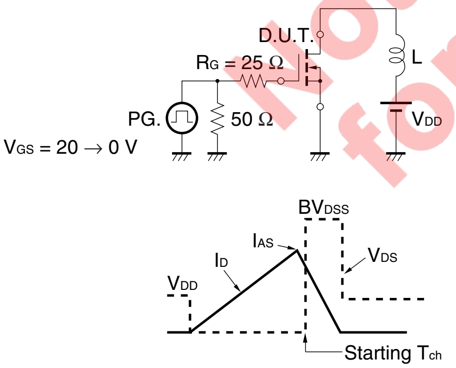
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

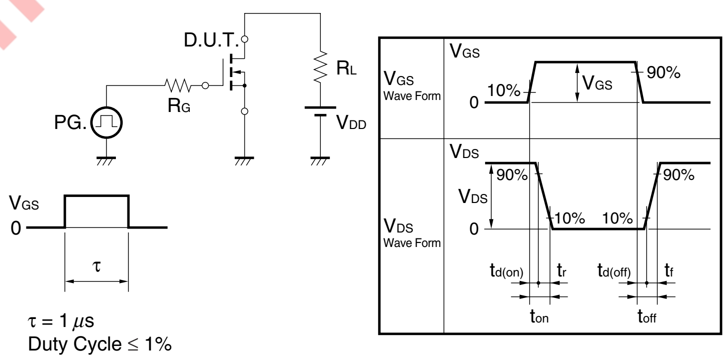
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 13 A	7.0			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 25 A		5.9	7.9	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 13 A		7.5	10	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		2230		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		319		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		171		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V		15		ns
Rise Time	t_r	I_D = 25 A		17		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = 10 V		51		ns
Fall Time	t_f	R_G = 0 Ω		5		ns
Total Gate Charge	Q_G	V_{DD} = 32 V		44		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		8		nC
Gate to Drain Charge	Q_{GD}	I_D = 50 A		12		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 50 A, V_{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, V_{GS} = 0 V		30		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		25		nC

Note Pulsed

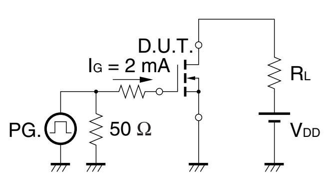
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

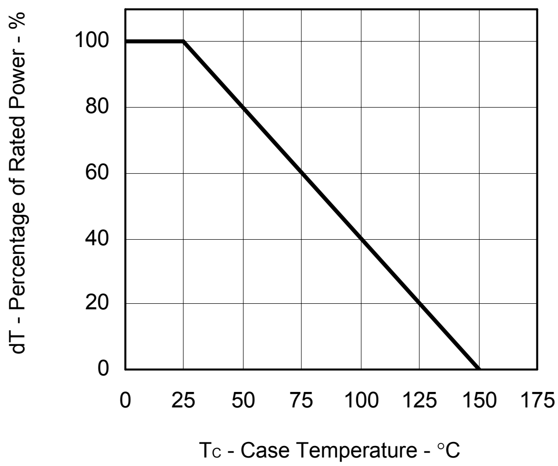


TEST CIRCUIT 3 GATE CHARGE

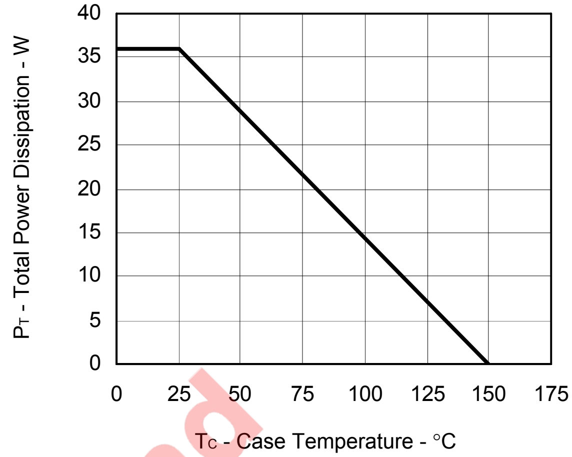


TYPICAL CHARACTERISTICS (T_A = 25°C)

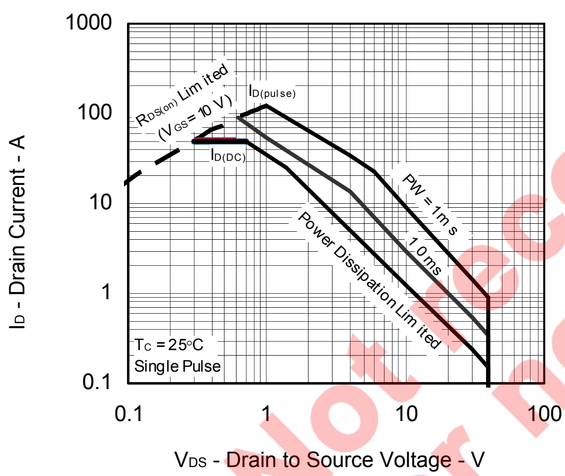
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



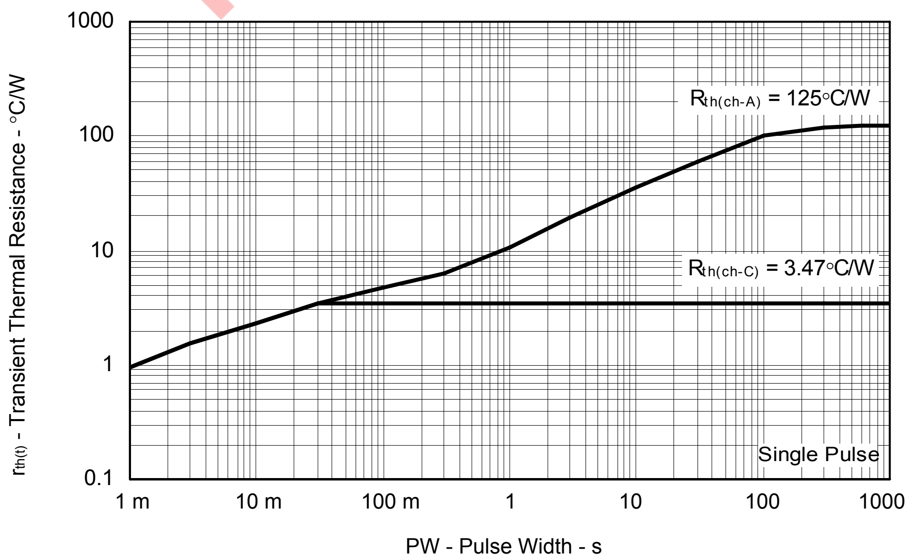
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



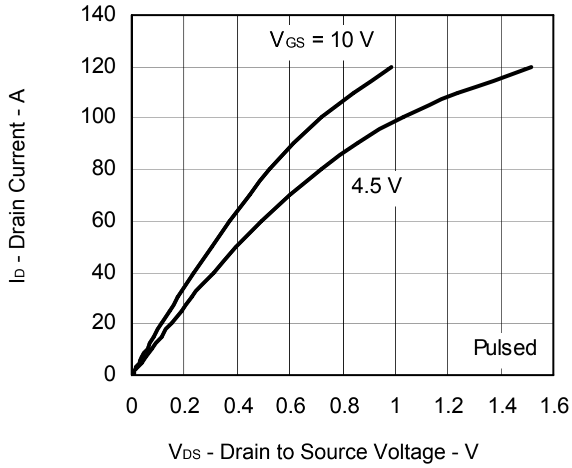
FORWARD BIAS SAFE OPERATING AREA



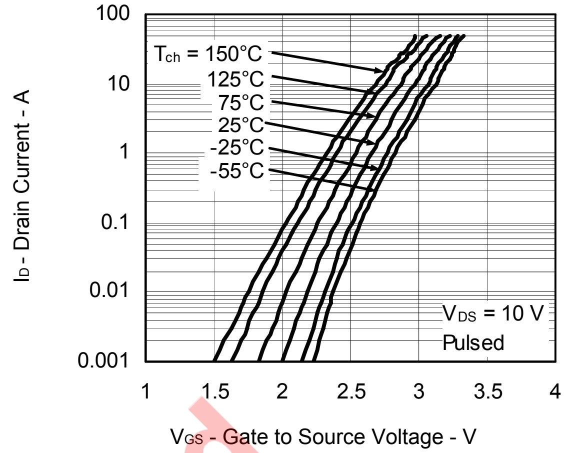
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



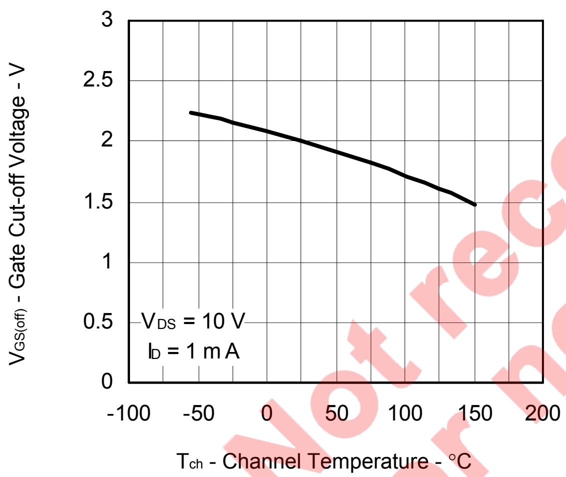
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



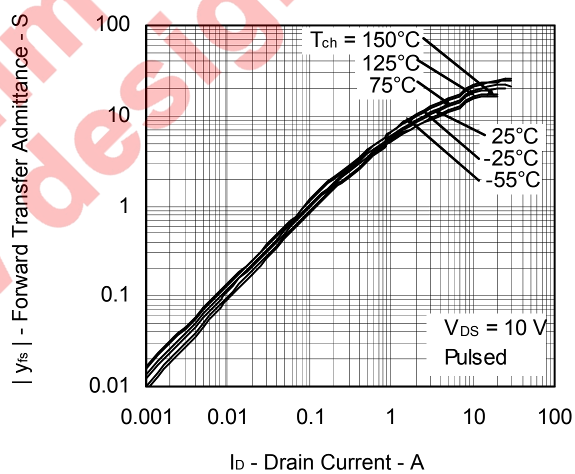
FORWARD TRANSFER CHARACTERISTICS



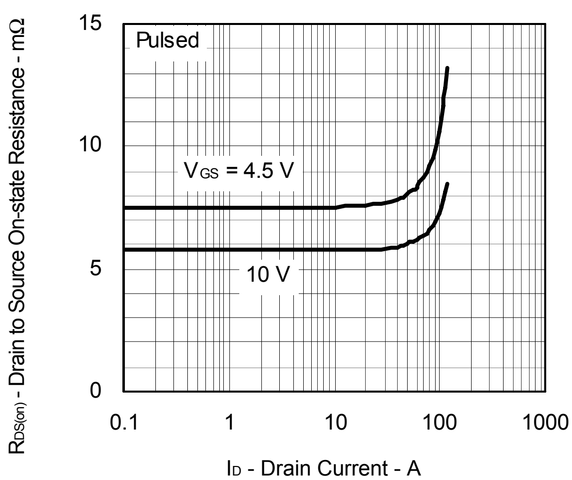
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



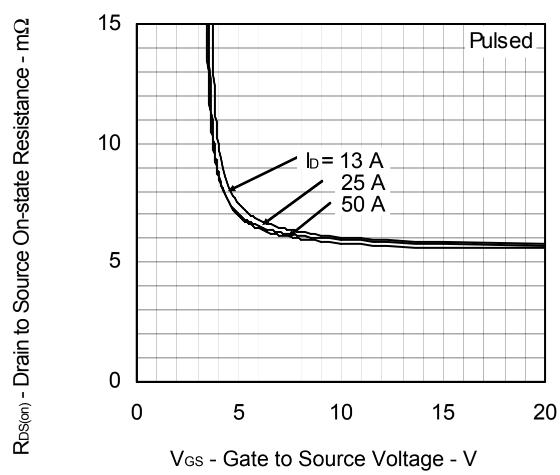
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



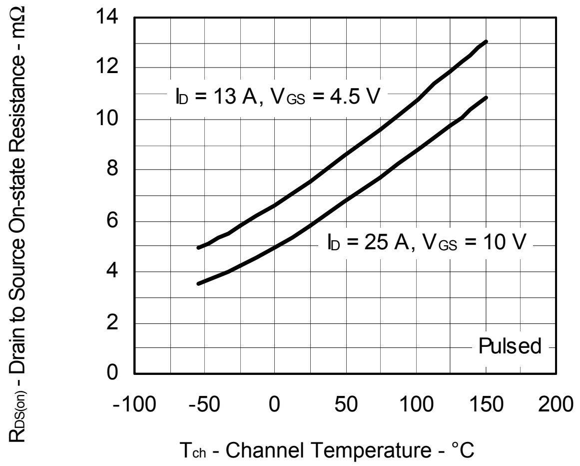
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



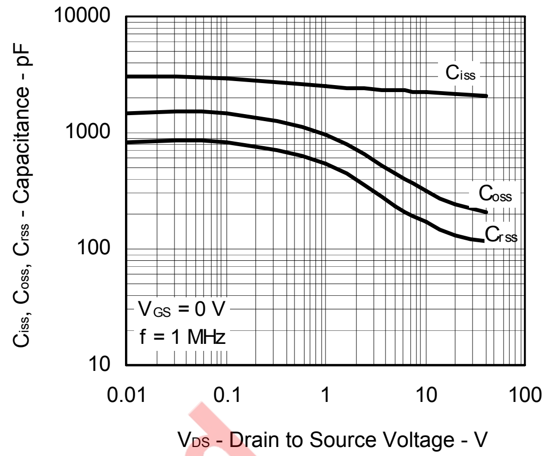
DRAIN TO SOURCE ON-STATERESISTANCE vs.
GATE TO SOURCE VOLTAGE



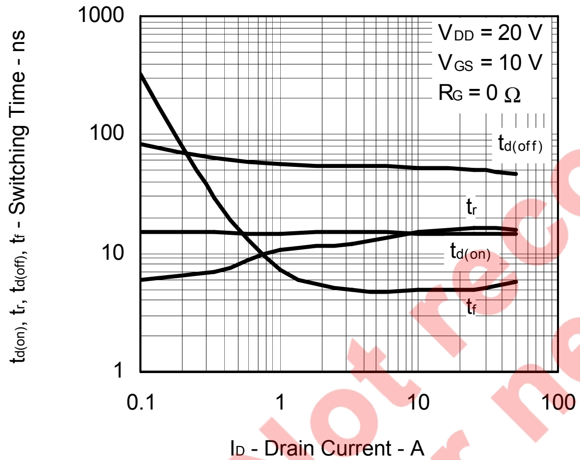
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



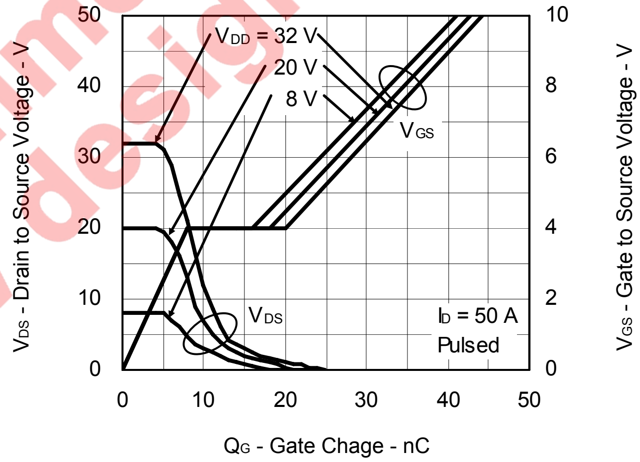
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



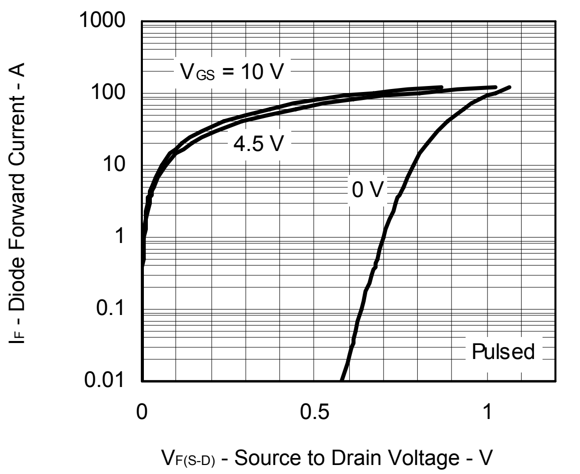
SWITCHING CHARACTERISTICS



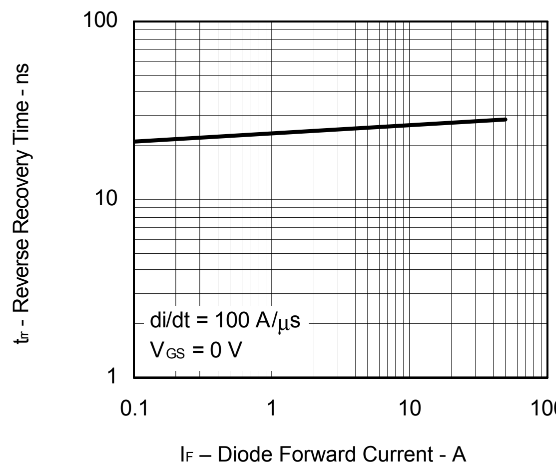
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

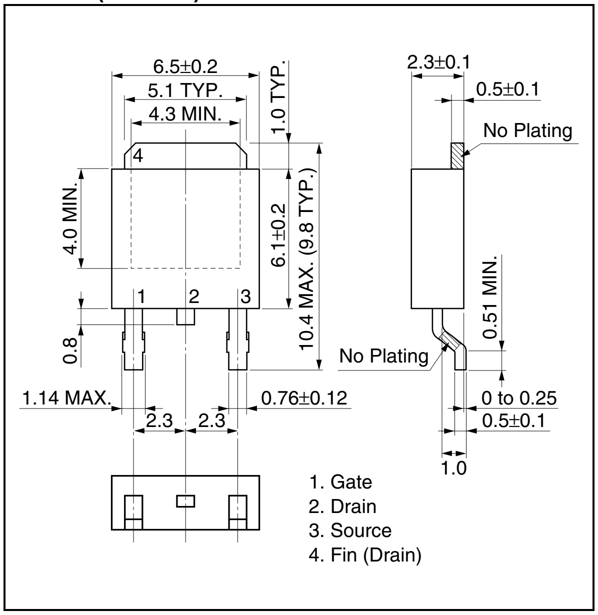


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

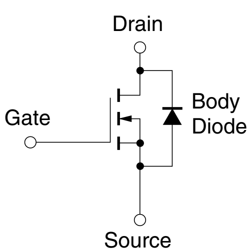


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



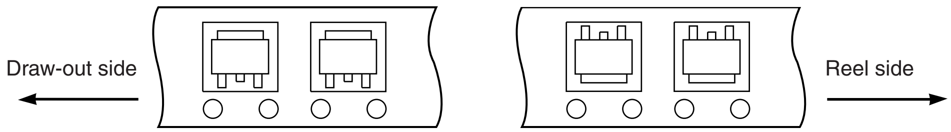
EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

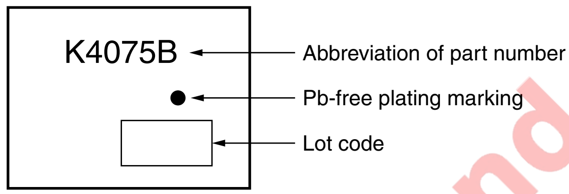
TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



–E1 TYPE –E2 TYPE

MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The 2SK4075B should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).