IDT82P2282 Data Sheet Change Notice

Supplemental Information

This notice describes the differences between the updated version (Version 10, dated August 20, 2009) and its previous version (Version 9, dated October 29, 2008) of the IDT82P2282 Data Sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Date Code	Changed Items
August 20, 2009	-	-	32-31
October 29, 2008	-	-	30-29
Feb 26, 2008	-	-	28
May 31, 2007	-	-	27
April 6, 2007	-	-	26-17
August 1, 2006	-	-	16
April 12, 2006	-	-	15-12
September 1, 2004	-	-	11 ~ 1

Changed Items

Aug 20, 2009

Item 32: Added clock recovery bullet point in APPLICATIONS portion. (Page 12)

Item 31: Added clock recovery paragraph in section '3.12 BIT-ORIENTED MESSAGE RECEIVER'. (Page 59)

Oct 29, 2008

Item 30: Added SSM bullet point in FEATURES portion. (Page 12)

Item 29: Added SSM paragraph in section '3.12 BIT-ORIENTED MESSAGE RECEIVER'. (Page 59)

Feb 26, 2008

Item 28: Updated Figure 21~24 and Figure 28~31 to clarify the F-bit in T1/J1 mode. (Pages 68, 69, 76, 77)

May 31, 2007

Item 27: Added E1 Reference Clock Output Control (03EH, 13EH) register. (Pages 241, 265)

April 6, 2007

Item 26: Removed the functional descriptions of the SS7 protocol support. (Pages 54,84, 193, 199, 201, 309, 316)

Item 25: Added the section '3.2.1 Line Monitor'. (Pages 24, 25, 26)

Item 24: Changed the E1 mode 'CRCM, SIGEN, GENCRC' bite control table. (Page 293)

Item 23: Changed the figure 'Read Operation In SPI Mode' and figure 'Write Operation In SPI Mode'. (Page 107)

Item 22: Added line driver set to '3.27.2.6 Analog Loopback'. (Page 102)

Item 21: Changed the paragragh about transmit clock slave mode and transmit clock master mode. (Page 72)

Item 20: Changed the paragragh about non-multiplexed mode. (Pages 70, 72)

Item 19: Changed the paragragh about receive clock slave mode and receive clock master mode. (Page 65)

Item 18: Added bit 'REFH_LOS' row to table 5. (Page 27)

Item 17: Changed REFA_OUT and REFB_OUT pin description. (Page 18)

August 1, 2006

Item 16: Changed package characteristics from PF to PK. (Page 381)

April 12, 2006

Item 15: Changed REFA_OUT and REFB_OUT pin description. (Page 18)

Item 14: Changed description of internal counters update methods. (Pages 48, 50)

Item 13: Added T1/J1 Reference Clock Output Control Register (03EH) (Page 150)

Item 12: Added green package information (Page 382)

September 1, 2004

Item 11: The description of the DDSINV bit (b3, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 6-bit DDS pattern and this bit is cleared when the inversion is completed. (Page 69, 166)

Item 10: The description of the CRCINV bit (b2, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 6-bit CRC pattern and this bit is cleared when the inversion is completed. (Page 69, 166)

Item 9: The description of the FsINV bit (b1, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one Fs bit in SF and T1 DM formats, invert one Frame Alignment bit in ESF format or invert one Synchronization Fs bit in SLC-96 format and this bit is cleared when the inversion is completed. (Page 166)

Item 8: The description of the FtINV bit (b0, T1/J1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one Ft bit in SF, T1 DM and SLC-96 formats and this bit is cleared when the inversion is completed. (Page 166)

Item 7: The description of the CRCINV bit (b5, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert all 4 calculated CRC bits in one Sub-Multi-Frame and this bit is cleared when the inversion is completed. (Page 71, 291)

Item 6: The description of the CRCPINV bit (b4, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 6-bit CRC Multi-Frame alignment pattern and this bit is cleared when the inversion is completed. (Page 71, 291)

Item 5: The description of the CASPINV bit (b3, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 4-bit Signaling Multi-Frame alignment pattern and this bit is cleared when the inversion is completed. (Page 71, 291)

Item 4: The description of the NFASINV bit (b2, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one NFAS bit and this bit is cleared when the inversion is completed. (Page 71, 291)

Item 3: The description of the FASALLINV bit (b1, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one 7-bit FAS pattern and this bit is cleared when the inversion is completed. (Page 71, 291)

Item 2: The description of the FAS1INV bit (b0, E1-06FH,...) is changed. A transition from '0' to '1' on this bit will invert one FAS bit and this bit is cleared when the inversion is completed. (Page 291)

Item 1: In 'Ordering Information', the package is changed to 'PF'. (Page 370)

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