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H8SX Family

Vector Table Address Switching

Introduction

This application note describes how to change the vector table address.

Target Devices

H8SX family

Contents

1. Overview	2
2. Applicable Conditions	2
3. Configuration.....	3
4. Sample Program	5

1. Overview

The H8SX CPU used in H8SX-family products has a function to allocate the exception handling vector table at a desired address. With the earlier H8/300, H8/300H, and H8S CPUs, the vector table is fixed at address 0. The H8SX CPU provides the vector base register (VBR) to change the vector table address. This application note describes an example of VBR usage.

2. Applicable Conditions

Table 1 Applicable Conditions

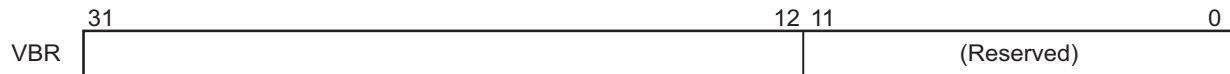
Item	Contents
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Assembler	H8S, H8/300 Series Cross Assembler Version 6.01.01 (from Renesas Technology Corp.)
H8S compiler options	-cpu = h8sxa:24:md, -code = asmcode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area

3. Configuration

VBR is a 32-bit register in which the upper 20 bits are valid. The lower 12 bits of this register are reserved and read as 0s.



As the upper 20 bits of VBR are valid, the address of the exception handling vector table can be specified as a multiple of H'1000. Different vector table address offsets (H'0000 to H'03FF) are assigned to different exception sources, and the address of each exception handling vector in the vector table is calculated from VBR contents and the vector table address offset for the exception source. Note that the vector addresses for the reset and CPU address error are fixed regardless of the VBR value. Table 3 shows the calculation method for exception handling vector addresses.

Table 3 Calculation Method for Exception Handling Vector Addresses

Exception Source	Instruction Length
Reset	Vector address = Vector table address offset (fixed value: H'0000 to H'0003)
CPU address error	Vector address = Vector table address offset (fixed value: H'0030 to H'0033)
Others	Vector address = VBR + vector table address offset

The capability of vector table allocation at a desired address using VBR provides the following advantages.

- The user program can dynamically change the location of the exception handling vector table. (The user program can dynamically switch between different interrupt handling routines.)
- Allocating the exception handling vector table in the on-chip RAM area can accelerate the response to interrupts (high-speed operation can be achieved even with the MCU without on-chip ROM).

Figure 1 shows an example of changing the address of the exception handling vector table through the VBR setting.

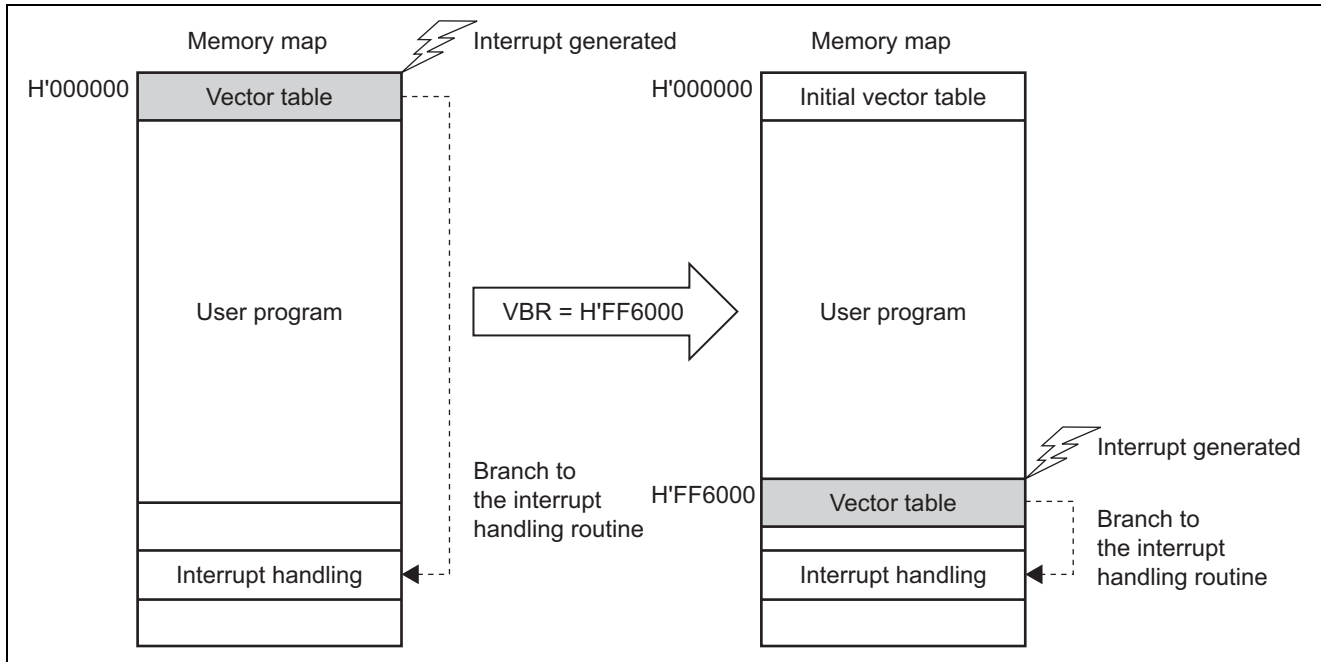


Figure 1 Example of VBR Setting

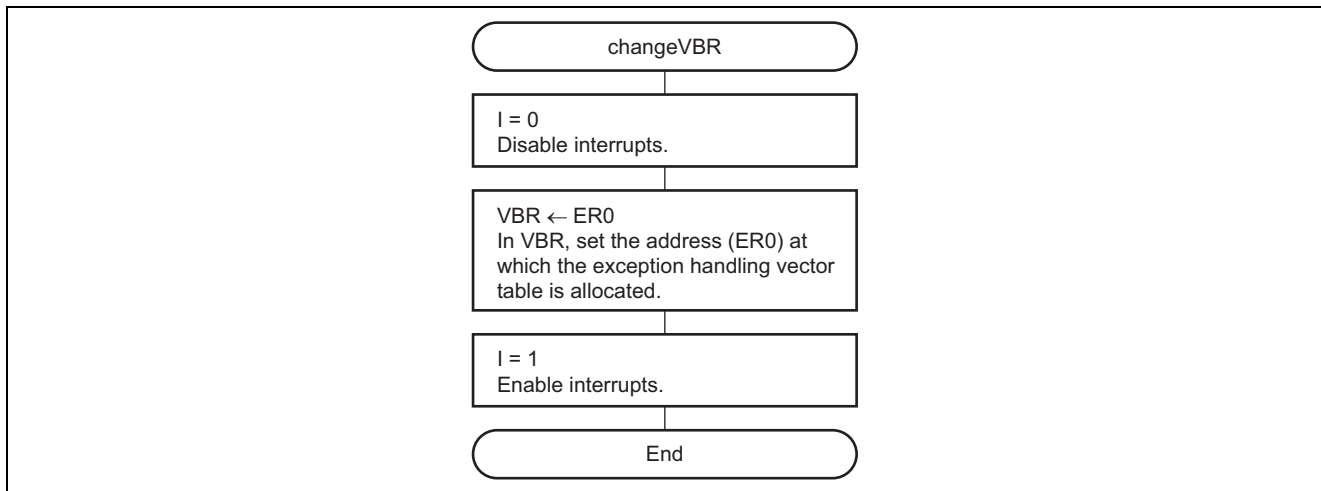
4. Sample Program

4.1 Flowchart

VBR should be accessed through assembly-language instructions because VBR cannot be directly accessed through the C programming language. This sample program is an example of writing assembly code within a C-language program.

The VBR value should be modified while interrupts are disabled. If an interrupt occurs while VBR is being modified with interrupts enabled, the H8SX CPU does not operate correctly.

The assembly code embedding function of the compiler allows assembly-language code to be written between `#pragma asm` and `#pragma endasm`. For details, refer to the H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual.



4.2 Program Listing

```

/*****/
/* Application Note */
/*****/

#include <machine.h>

/*****/
/* RAM allocation */
/*****/
#define VECTOR_ADDRESS 0xFF6000 /* Vector table address */

/*****/
/* function prototype */
/*****/
void main ( void );
void changeVBR ( unsigned long vector_adrs );

/*****/
/* Vector Address */
/*****/
#pragma entry main(sp=0xFFC000,vect=0) /* H'0000 : Reset */

#pragma section /* P */
/*****/
/* Main Program */
/*****/
void main ( void )
{
    changeVBR( (unsigned long)VECTOR_ADDRESS );

    while(1);
}

/*****/
/* Change VBR */
/*****/
void changeVBR ( unsigned long vector_adrs )
{
    set_imask_ccr(1); /* Disable interrupts */
#pragma asm
    LDC.L ER0,VBR ; set VBR
#pragma endasm
    set_imask_ccr(0); /* Enable interrupts */
}

```


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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.11.06	—	First edition issued

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