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H8/300L Super Low Power Series

Using Timer F to Implement Clock Operation (H8/3867)

Introduction

A sub-clock (ϕw) of 38.4 kHz is used to perform the timer operation by timer F. The timer counter specified in the RAM is incremented by generating a timer F interrupt every second.

When incrementing up to 59 minutes59 seconds, it is initialized to 00 minute 00 second.

Target Device

H8/3867

Contents

1. Specifications

1. A sub-clock of 38.4 kHz is used to perform the timer operation by timer F.
2. The timer counter specified in the RAM is incremented by generating a timer F interrupt every second.
3. The counter specified in the RAM is comprised of 8 bits for counting seconds and 8 bits for counting minutes. It is initialized to 00 minute 00 second before incrementing, incrementing up to 59 minutes 59 seconds, and then initializing to 00 minute 00 second to restart incrementation.
4. After initialization, a transition from active (high speed) mode to watch mode occurs, then a transition to sub-active mode occurs by a timer F interrupt request, the counter specified in the RAM is incremented, and then a transition to watch mode occurs.
5. Figure 1 shows a mode transition in this sample task.

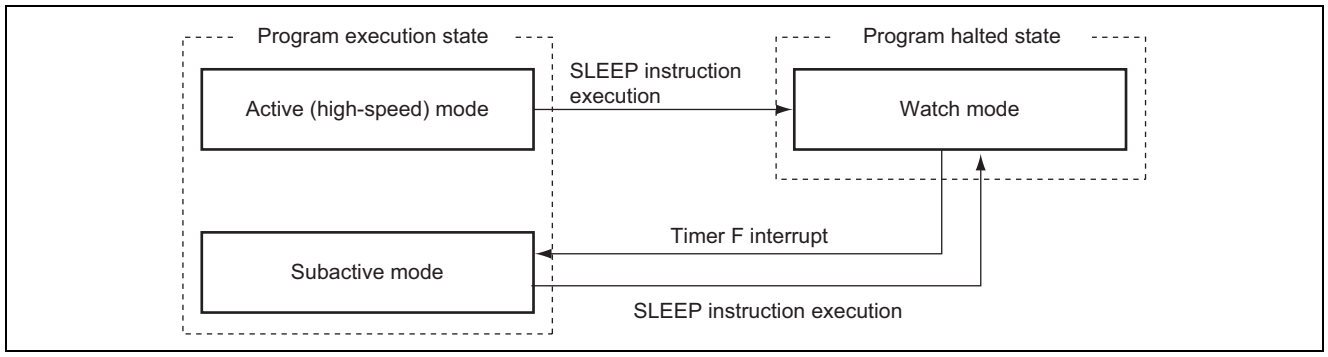


Figure 1 Mode Transition in this Sample Task

2. Description of Functions Used

1. In this sample task, timer F is used to increment the counter specified in the RAM every second. The following describes the timer F characteristics.
   - — One of four clocks (ϕ/32, ϕ/16, ϕ/4, ϕw/4) and an external clock can be selected. (An external event can be counted.)
   - — A toggle signal is output from the TMOFH pin by a compare match signal. (Initial value of the toggle output can be specified.)
   - — Counter reset is enabled by the compare match signal.
   - — Two interrupt sources: one compare match and one overflow are provided.
   - — Timer F can also operate as two 8-bit timers (timers FH and FL)
   - — When ϕw/4 is selected as an internal clock, timer F can operate in watch mode, sub-active mode, or sleep mode.
   - — Timer F can be placed in standby mode by module standby mode while timer F is not used.
2. Figure 2 shows the block diagram of 16-bit compare match function of timer F used in this sample task.

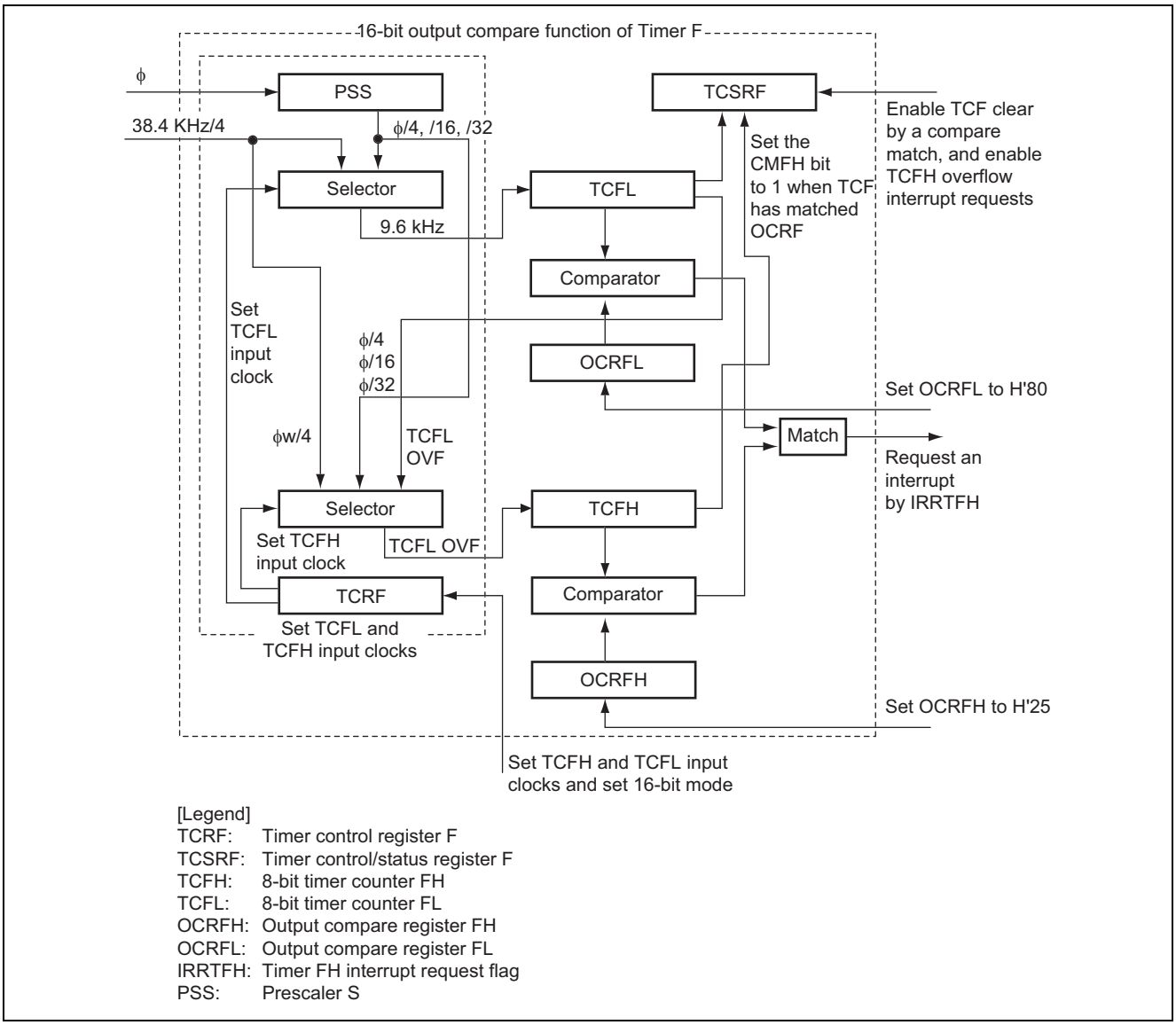


Figure 2 Block Diagram of Timer F Compare Match Function

3. Table 1 describes the timer F functions.

Table 1 Timer F Functions

Register	Function
Timer control register F (TCRF)	TCRF is an 8-bit write-only register that switches 16-bit mode to 8-bit mode, selects one of four internal clocks and an external event, and set the TMOFH and TMOFL pin output levels. TCRF is initialized to H'00 after a reset.
Timer control status register F (TCSRF)	TCSRF is an 8-bit readable/writable register that selects counter clear, sets overflow flag and compare match flag, and enables an overflow interrupt request.
16-bit timer counter F (TCF)	TCF is a 16-bit readable/writable up-counter that is comprised of two 8-bit timer counters (TCFH and TCFL) which are cascade connected. TCF can be used as a 16-bit counter comprised of TCFH of the upper 8 bits and TCFL of the lower 8 bits. TCF also can be used as two independent 8-bit counters TCFH and TCFL. TCFH and TCFL can be read or written by the CPU. In 16-bit mode, data transfer between the CPU and TCFH or TCFL is performed via a temporary register (TEMP). TCFH and TCFL are initialized to H'00 after a reset. When the CKSH2 bit of TCRF is cleared to 0, the TCF functions as a 16-bit counter. The clock to be input to the TCF is selected by the CKSL2 to CKSL0 bits of TCRF. TCF can be cleared by a compare match by the CCLRH bit of TCSRF. When TCF overflows, the OVFH bit of TCSRF is set to 1 and an interrupt is requested when the IENTFH of IENR2 is set to 1.
8-bit timer counter FH (TCFH)	TCFH can operate independently as an 8-bit counter by setting the CKSH2 bit of TCRF to 1. A clock to be input to the TCFH is selected by the CKSH2 to CKSH0 bits of TCRF. TCFH can be cleared by a compare match by setting the CCLRH bit of TCSRF. When TCFH overflows, the OVFH bit of TCSRF is set to 1. In this case, when the OVIEH bit of TCSRF is set to 1, the IRRTFH bit of IRR2 is set to 1, and an interrupt is requested to the CPU when the IENTFH bit of IENR2 is set to 1.
8-bit timer counter FL (TCFL)	TCFL can operate independently as an 8-bit counter by setting the CKSH2 bit of TCRF to 1. A clock to be input to the TCFL is selected by the CKSL2 to CKSL0 bits of TCRF. TCFL can be cleared by a compare match by setting the CCLRL bit of TCSRF. When TCFL overflows, the OVFL bit of TCSRF is set to 1. In this case, when the OVIEL bit of TCSRF is set to 1, the IRRTFL bit of IRR2 is set to 1, and an interrupt is requested to the CPU when the IENTFL bit of IENR2 is set to 1.

Register	Function
16-bit output compare register F (OCRF)	OCRF is a 16-bit readable/writable register comprised of two 8-bit registers OCRFH and OCRFL. OCRF can be used either as a 16-bit register comprised of upper 8 bits of OCRFH and lower 8 bits of OCRFL or as two independent 8-bit registers OCRFH and OCRFL. OCRFH and OCRFL can be read or written by the CPU. In 16-bit mode, data transfer between the CPU and OCRFH or OCRFL is performed via the TEMP register. OCRFH and OCRFL are initialized to H'FF after a reset. When the CKSH2 bit of TCRF is cleared to 0, the OCRF functions as a 16-bit register. The contents of the OCRF are constantly compared with those of TCF. When OCRF matches the TCF, the CMFH bit of TCSRF is set to 1 and the IRRTFH of IRR2 is set to 1 simultaneously. In this case, when the IENTFH bit of IENR2 is set to 1, an interrupt request is given to the CPU. A toggle signal by a compare match can be output from the TMOFH pin. The output level (high or low) can be set by the TOLH bit of TCRF.
8-bit output compare register FH (OCRFH)	When the CKSH2 bit of TCRF is set to 1, the OCRF functions as two 8-bit registers; OCRFH and OCRFL. The contents of OCRFH and OCRFL are compared with the contents of TCFH and TCFL, respectively. When OCRFH matches TCFH, the CMFH bit of TCSRF is set to 1 and simultaneously the IRRTFH bit of IRR2 is set to 1. In this case, when the IENTFH bit of IENR2 is set to 1, an interrupt request is given to the CPU. In addition, a toggle signal by a compare match can be output from the TMOFH pin. The output level (high or low) can be set by the TOLH bit of TCRF.
8-bit output compare register FL (OCRFL)	When the CKSH2 bit of TCRF is set to 1, the OCRF functions as two 8-bit registers; OCRFH and OCRFL. The contents of OCRFH and OCRFL are compared with the contents of TCFH and TCFL, respectively. When OCRFL matches TCFL, the CMFL bit of TCSRF is set to 1 and simultaneously the IRRTFL bit of IRR2 is set to 1. In this case, when the IENTFL bit of IENR2 is set to 1, an interrupt request is given to the CPU. In addition, a toggle signal by a compare match can be output from the TMOFL pin. The output level (high or low) can be set by the TOLL bit of TCRF.
Timer FH interrupt request flag (IRRTFH)	When TCF matches OCRF in 16-bit mode, when TCFH matches OCRFH in 8-bit mode, or when TCF and TCFH overflow while IENTFH is set to 1, IRRTFH is set to 1. IRRTFH is cleared to 0 when IRRTFH is set to 1 while it is 1.
Timer FL interrupt request flag (IRRTFL)	When TCFL matches OCRFL in 8-bit mode, or when TCFL overflows while IENTFL is set to 1, IRRTFL is set to 1. IRRTFL is cleared to 0 when IRRTFL is set to 1 while it is 1.
Timer FH interrupt enable flag (IENTFH)	IENTFH enables or disables a timer FH compare match or overflow interrupt.
Timer FL interrupt enable flag (IENTFL)	IENTFL enables or disables a timer FL compare match or overflow interrupt.
Timer F event input (TMIF)	An event input to be input to the TCFL
Timer FH output (TMOFH)	A timer FH toggle output pin
Timer FL output (TMOFL)	A timer FL toggle output pin

4. The following describes the timer FH interrupt period specification method.
   In this sample task, 38.4 kHz is used as a sub clock to operate timer F as a base clock.
   By setting the CKSL2 to CKLS0 bits of TCRF to 1, the TCF input clock is set as ϕw/4.
   ϕw/4 corresponds to the following:

   ϕw/4 = 38.4 kHz/4 = 9.6 kHz

   Accordingly, TCF input clock frequency can be calculated as follows:

   1/9.6 kHz ≅ 104.167 µs

   When OCRF is set to H'2580, the time necessary to match TCF with OCRF is calculated as follows:

   H'2580 × (1/9.6 kHz) = 9600 × 104.167 µs = 1 s

   Accordingly, OCRF to set timer FH interrupt cycle T_{FH} can be calculated as follows:

   OCRF setting value = T_{FH}/(1/9.6 kHz) = T_{FH} × 9.6 kHz

   Table 2 shows an example of timer FH interrupt periods and OCRA setting values.

Table 2 Timer FH Interrupt Periods and OCRA Setting Values

T_{FH} (s)	Calculation Method	OCRA Setting Value
0.125	0.125 s × 9.6 kHz = 1200	H'04B0
0.25	0.25 s × 9.6 kHz = 2400	H'0960
0.5	0.5 s × 9.6 kHz = 4800	H'12C0
1	1 s × 9.6 kHz = 9600	H'2580
2	2 s × 9.6 kHz = 19200	H'4B00

5. The following describes the timer F to CPU interface.
   TCF and OCRF are 16-bit readable/writable registers; while the data bus between the CPU and on-chip peripheral modules is 8-bit width. Accordingly, the CPU accesses TCF or OCRF via the 8-bit temporary register TEMP.
   In 16-bit mode, TCF should be read or written or OCRF should be written in 16-bit units (executing two byte-size MOV instructions sequentially). In this case, the access should be performed in the upper bytes and then lower bytes. Note that data cannot be transferred correctly by accessing only the upper or lower byte.
   In 8-bit mode, there are no restrictions on TCF and OCRF access.
   a. Write operation
      By writing to the upper byte, the upper byte data is transferred to the TEMP register. Next, by writing to the lower byte, data in the TEMP register is written to the upper byte register and the lower byte data is directly written to the lower byte register.
      Figure 3 shows the TCF write operation when H'AA55 is written to the TCF.

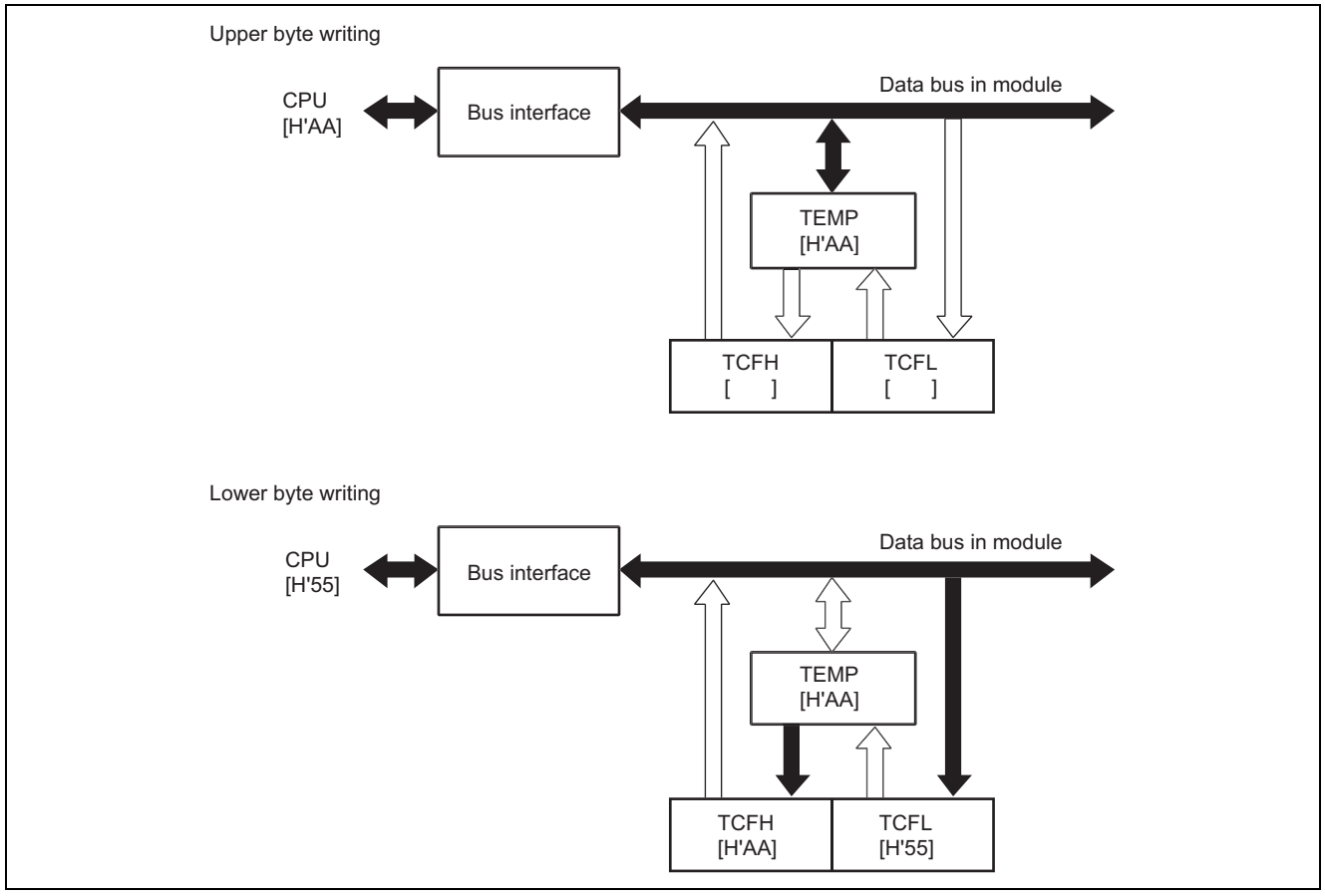


Figure 3 TCF Write Operation

b. Read operation

When the TCF is read, by reading the upper byte, upper byte data is transferred to the CPU directly, and the lower byte is transferred to the TEMP register. By reading the lower byte, lower byte data in the TEMP register is transferred to the CPU.

Once the OCRF is read, by reading the upper byte, the upper byte data is transferred to the CPU directly and by reading the lower byte, lower byte data is transferred to the CPU directly.

Figure 4 shows the case where H'AAFF is read from the TCF.

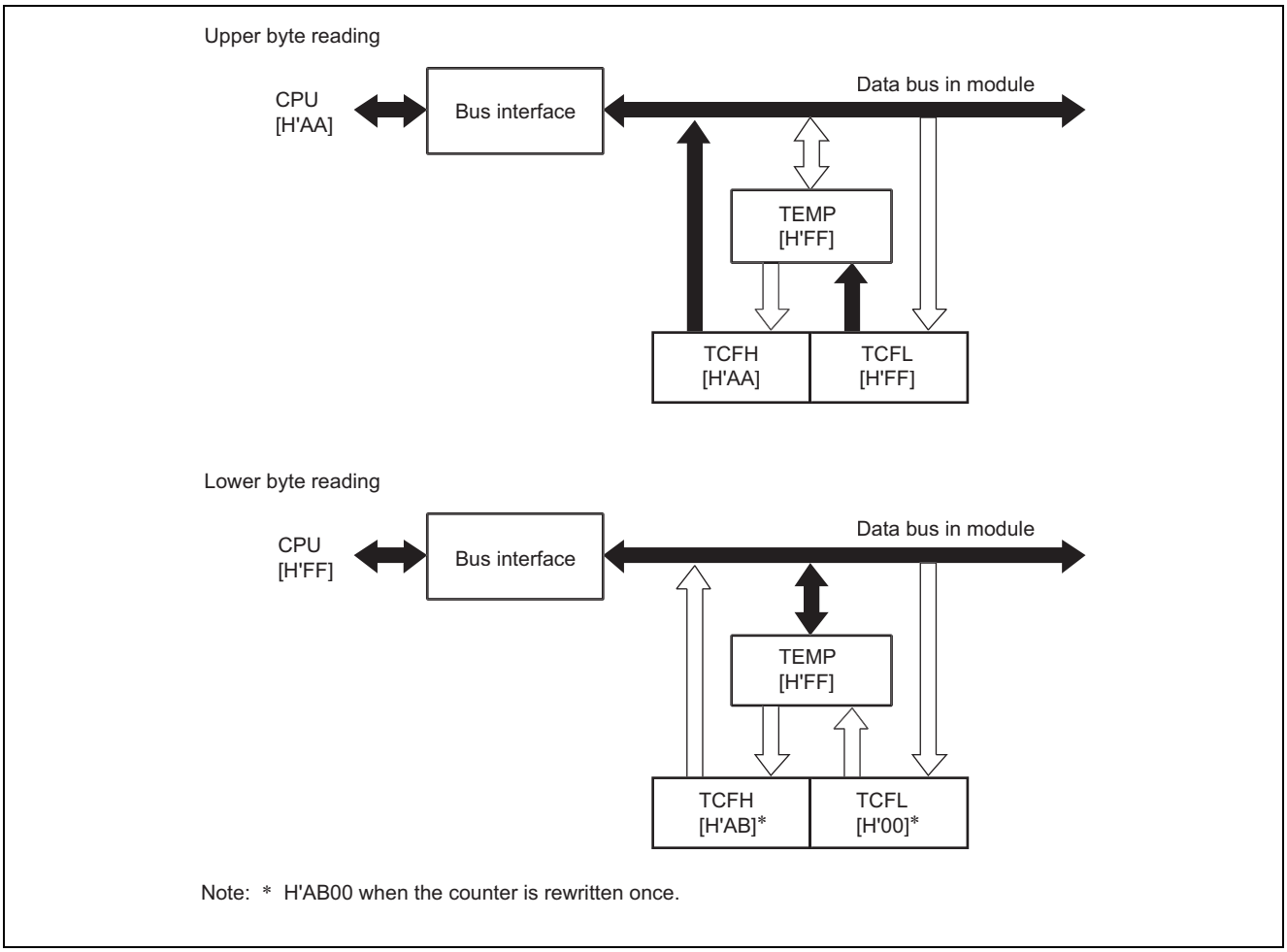


Figure 4 TCF Read Operation

6. Precautions on Timer F Usage

   Note the following conflicts or illegal operations may occur while timer F is used as the 16-bit timer mode.

   a. A toggle signal is output from the TMOFH when a compare match signal is generated when 16 bits of OCRF completely match the 16 bits of TCF. When a write to the TCRF by a MOV instruction occurs simultaneously with the compare match signal generation, TOLH data written by the TCRF write is output from the TMOFH pin. In 16-bit timer mode, TMOFL pin output is undefined. Accordingly, the TMOFL pin should be used as a port in 16-bit timer mode.
   b. When a write to the OCRFL occurs simultaneously with a compare match signal generation, the compare match signal is invalidated. Note, however, that when the OCRFL write value matches the counter value, the compare match signal is generated at this time. The compare match signal is output synchronously with the TCFL clock. Accordingly, while the TCFL clock stops, no compare match signal is generated even when a compare match occurs.
   c. The compare match flag is set to the CMFH bit when a compare match signal is generated when the 16 bits of OCRF completely match the 16 bits of TCF. The CMFL bit is set to 1 when the set conditions for the lower 8 bits are satisfied.
   d. When the TCF overflows, the OVFH bit is set to 1. The OVFL bit is set to 1 when the set conditions for the lower 8 bits are satisfied when the lower 8 bits of TCF overflows. When a write to the TCFL occurs simultaneously with an overflow signal output, the overflow signal is not output.
   e. When $\phi w/4$ is selected as TCF internal clock in active mode or sleep mode, the system clock is asynchronous with the internal clock. Accordingly, the system clock is synchronized with the internal clock by the synchronization circuit. This causes a maximum $1/\phi$ (s) of deviation in the count period. To prevent such a deviation from occurring, the timer should be operated in sub-active mode, sub-sleep mode, or watch mode.

7. Table 3 indicates the allocation of functions in this sample task.

Table 3 Function Allocation

Function	Function Allocation
TCRF	Sets 16-bit mode and selects a clock to be input to the TCFL
TCSRF	Selects the counter clear, sets the overflow flag and compare match flag, and enables or disables an overflow interrupt
TCF	Functions as a 16-bit up-counter comprised of TCFH and TCFL. It is incremented by an internal clock ($\phi w/4$) and that sets IRTFH and CMFH to 1 by a compare match
OCRF	16-bit register comprised of OCRFH and OCRFL. When data specified in OCRF matches the TCF, a compare match signal is generated
IRRTFH	Indicates whether a timer FH interrupt occurs or not
IENTFH	Enables or disables a timer FH interrupt
ϕw	Sub-clock frequency of 38.4 kHz

3. Principle of Operations

1. The following describes the 16-bit timer mode operation of timer F.
   Timer F is a 16-bit counter that is incremented by an input clock. The contents of the output compare register F is constantly compared with the contents of the timer counter F. When a compare match occurs, the counter can be cleared, an interrupt can be generated, and a toggle signal can be output from the port. Timer F can also be used as two independent 8-bit timers.
   When the CKSH2 bit of timer control register F (TCRF) is cleared to 0, timer F functions as a 16-bit timer. Immediately after a reset, timer counter F (TCF) is initialized to H'0000, output compare register F (OCRF) to H'FFFF, timer control register (TCRF) and timer control status register (TCSRF) to H'00, respectively. The counter starts incrementing from inputs from an external event (TMIF). An edge of an external event (TMIF) can be set by the IEG3 bit of the IRQ edge select register (IEGR)
   By setting the CKSL2 to CKSL0 bits of TCRF, the timer F operating clock can be selected from three types of internal clocks output from prescaler S, an internal clock generated by dividing the sub-clock by four, or an external clock.
   The contents of TCF and OCRF are constantly compared. When they match, the CMFH bit of TCSRF is set to 1. In this case, when the IENTFH bit of IENR2 is set to 1, an interrupt request is given to the CPU and the TMOFH pin output is toggled simultaneously. In addition, when the CCLRH bit of TCSRF is set to 1, the TCF is cleared. Note that the TMOFH pin output can be set by the TOLH bit of the TCRF.
   When the TCF overflows (H'FFFF → H'0000), the OVFH bit of TCSRF is set to 1. In this case, when both the OVIEH bit of TCSRF and the IENTFH bit of IENR2 are set to 1, an interrupt is requested by the CPU.

2. Table 4 shows the timer F operating mode.

Table 4 Timer F Operating Mode

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module standby
TCF	Reset	Operates	Operates	Operates/ stops*	Operates/ stops*	Operates/ stops*	Stops	Stops
OCRF	Reset	Operates	Held	Held	Operates	Held	Held	Held
TCRF	Reset	Operates	Held	Held	Operates	Held	Held	Held
TCSRF	Reset	Operates	Held	Held	Operates	Held	Held	Held

Note: * When $\phi_w/4$ is selected as the TCF's internal clock in active mode or sleep mode, the system clock and internal clock are mutually asynchronous, and so synchronization is established by a synchronization circuit. This results in a maximum error of 1/ϕ(s) in the count period.
When the counter is operated in subactive mode, watch mode, or subsleep mode, $\phi_w/4$ must always be selected as the internal clock. The counter will not operate when any other internal clock is selected.

3. Figure 5shows the principle applied to this sample task.

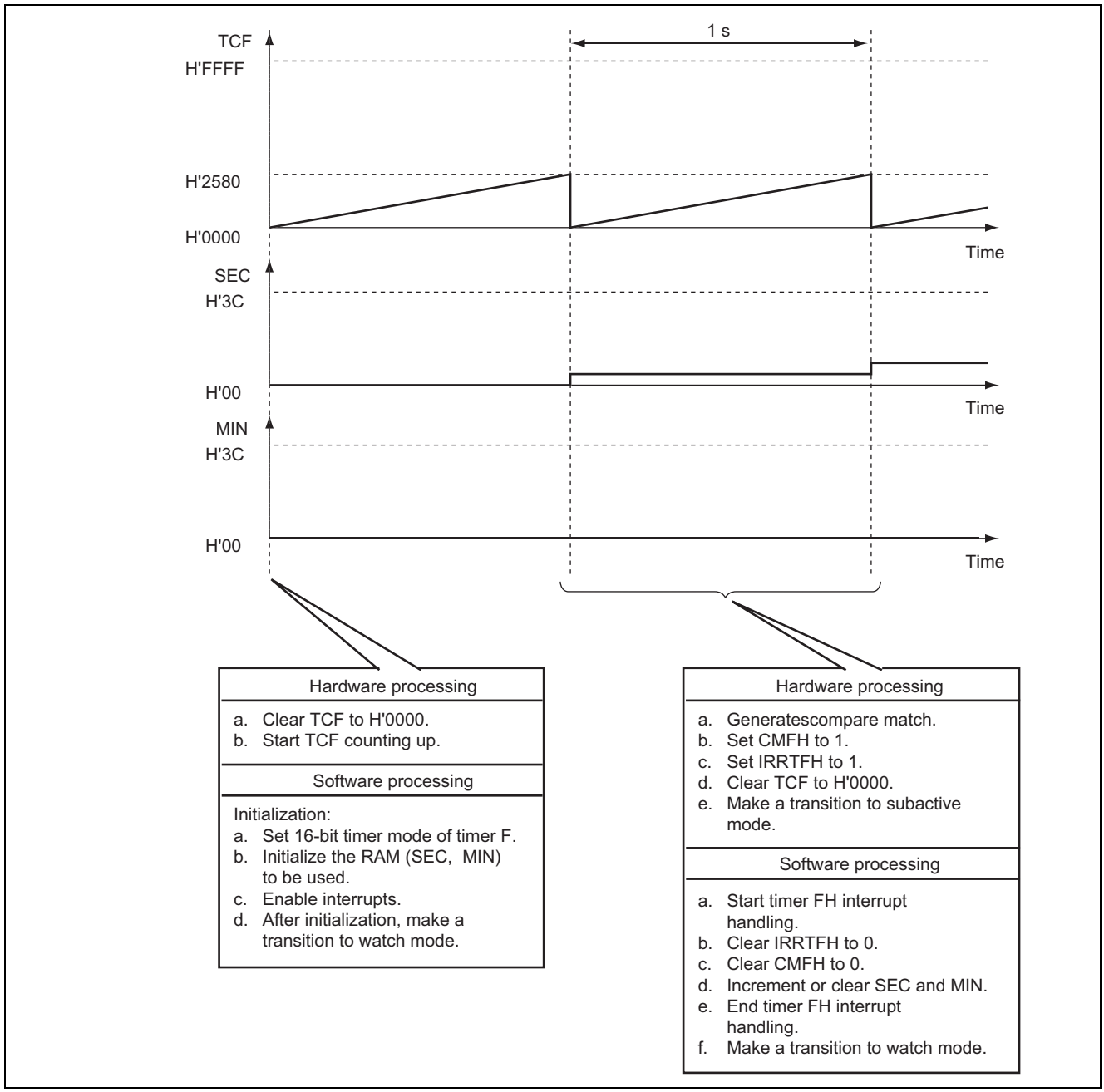


Figure 5 Principle applied to this sample task

4. Description of Software

4.1 Modules

Table 5 describes the modules used in this sample task.

Table 5 Description of Modules

Module	Label	Function
Main Routine	MAIN	Initializes the stack pointer, used RAM, and timer F, enables interrupts, and performs a transition to watch mode.
Timer F interrupt processing routine	TFINT	Clears IRRTFH and CMFT to 0, saves register contents, increments or clears SEC and MIN set to RAM, and restores register contents.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers

The internal registers used in this sample task are described in table 6.

Table 6 Description of Internal Registers

Register		Function	Address	Setting
TCRF	CKSH2 CKSH1 CSKH0	Timer control register F (Clock select H3 to H0) Selects a clock to be input to the TCFH as one of four internal clocks or a TCFL overflow. CKSH2 = 0, CKSH1 = 0, CKSH0 = 0: Select a TCL overflow CKSH2 = 0, CKSH1 = 0, CKSH0 = 1: Select a TCL overflow CKSH2 = 0, CKSH1 = 1, CKSH0 = 0: Select a TCL overflow CKSH2 = 0, CKSH1 = 1, CKSH0 = 1: Setting prohibited CKSH2 = 1, CKSH1 = 0, CKSH0 = 0: Select internal clock ϕ/32 CKSH2 = 1, CKSH1 = 0, CKSH0 = 1: Select internal clock ϕ/16 CKSH2 = 1, CKSH1 = 1, CKSH0 = 0: Select internal clock ϕ/4 CKSH2 = 1, CKSH1 = 1, CKSH0 = 1: Select internal clock ϕw/4	H'FFB6 Bit 6 Bit 5 Bit 4	CKSH2 = 0 CKSH1 = 0 CKSH0 = 0
	CKSL2 CKSL1 CSKL0	Timer control register F (Clock select L2 to L0) Selects a clock to be input to the TCFL as one of four internal clocks or an external event. CKSL2 = 0, CKSL1 = 0, CKSL0 = 0: Select an external event CKSL2 = 0, CKSL1 = 0, CKSL0 = 1: Select an external event CKSL2 = 0, CKSL1 = 1, CKSL0 = 0: Select an external event CKSL2 = 0, CKSL1 = 1, CKSL0 = 1: Setting prohibited CKSL2 = 1, CKSL1 = 0, CKSL0 = 0: Select internal clock ϕ/32 CKSL2 = 1, CKSL1 = 0, CKSL0 = 1: Select internal clock ϕ/16 CKSL2 = 1, CKSL1 = 1, CKSL0 = 0: Select internal clock ϕ/4 CKSL2 = 1, CKSL1 = 1, CKSL0 = 1: Select internal clock ϕw/4	H'FFB6 Bit 2 Bit 1 Bit 0	CKSL2 = 1 CKSL1 = 1 CKSL0 = 1

Register		Function	Address	Setting
TCSRF	OVFH	Timer control status register F (Timer overflow flag H) Indicates whether the TCF has overflowed or not. OVFH = 0: Indicates that the TCF has not overflowed. OVFH = 1: Indicates that the TCF has overflowed	H'FFB7 Bit 7	0
	CMFH	Timer control status register F (Compare match flag H) Indicates whether TCF and OCRF compare match has occurred or not. CMFH = 0: Indicates that the no TCF and OCRF compare match has occurred. CMFH = 1: Indicates that a TCF and OCRF compare match has occurred.	H'FFB7 Bit 6	0
	OVIEH	Timer control status register F (Timer overflow interrupt enable H) Enables or disables an interrupt when a TCF overflow occurs. OVIEH = 0: Disables an interrupt by a TCF overflow. OVIEH = 1: Enables an interrupt by a TCF overflow.	H'FFB7 Bit 5	1
	CCLRH	Timer control status register F (Counter clear H) Enables or disables the TCF clear when a TCF and OCRF compare match occurs. CCLRH = 0: Disables TCF clear by a compare match. CCLRH = 1: Enables TCF clear by a compare match.	H'FFB7 Bit 4	1
TCFH		Timer counter FH Upper 8 bits of the 16-bit timer counter (TCF). It is incremented by inputting TCFL overflow signal.	H'FFB8	H'00
TCFL		Timer counter FL Lower 8 bits of the 16-bit timer counter (TCF). It is incremented by inputting internal clock ϕw/4.	H'FFB9	H'00
OCRFH		Output compare register FH Upper 8 bits of the 16-bit output compare register (OCRF). It generates a compare match signal when the OCRF matches the TCF.	H'FFBA	H'25
OCRFL		Output compare register FL Lower 8 bits of the 16-bit output compare register (OCRF). It generates a compare match signal when the OCRF matches the TCF.	H'FFBB	H'80
IENR2	IENTFH	Interrupt enable register 2 (Timer FH interrupt enable) Enables or disables a timer FH interrupt request. IENTFH = 0: Disables a timer FH interrupt request. IENTFH = 1: Enables a timer FH interrupt request.	H'FFF4 Bit 3	1
IRR2	IRRTFH	Interrupt request register 2 (Timer FH interrupt request flag) Indicates whether a timer FH interrupt has been requested or not. IRRTFH = 0: Indicates that no timer FH interrupt has been requested. IRRTFH = 1: Indicates that a timer FH interrupt has been requested.	H'FFF7 Bit 3	0

Register		Function	Address	Setting
SYSCR1	SSBY	System control register 1 (software standby) Specifies a transition to standby mode or watch mode. SSBY = 0: After executing the SLEEP instruction in active mode, generates a transition to sub-active mode, or after executing the SLEEP instruction in sub-active mode, generates a transition to sub-sleep mode. SSBY = 1: After executing the SLEEP instruction in active mode, generates a transition to standby mode or watch mode, or after executing the SLEEP instruction in sub-active mode, generates a transition to watch mode.	H'FFF0 Bit 7	1
	STS2 STS1 STS0	System control register 1 (Standby timer select 2 to 0) Specifies the CPU and the peripheral function wait time untill the clock is stabilized when a transition from standby mode or watch mode to active mode is caused by a specific interrupt. The wait time should be specified longer than the clock stabilization time according to the operating frequency. STS2 = 0, STS1 = 0, STS0 = 0: Specifies the wait time as 8192 states. STS2 = 0, STS1 = 0, STS0 = 1: Specifies the wait time as 16384 states. STS2 = 0, STS1 = 1, STS0 = 0: Specifies the wait time as 32768 states. STS2 = 0, STS1 = 1, STS0 = 1: Specifies the wait time as 65536 states. STS2 = 1, STS1 = 0, STS0 = 0: Specifies the wait time as 131072 states. STS2 = 1, STS1 = 0, STS0 = 1: Specifies the wait time as 2 states. STS2 = 1, STS1 = 1, STS0 = 0: Specifies the wait time as 8 states. STS2 = 1, STS1 = 1, STS0 = 1: Specifies the wait time as 16 states.	H'FFF0 Bit 6 Bit 5 Bit 4	STS2 = 0 STS1 = 0 STS0 = 0
	LSON	System control register 1 (Low-speed on flag) Selects CPU operating clock as the system clock or sub-clock when watch mode is cancelled. LSON = 0: Selects a system clock as the CPU operating clock. LSON = 1: Selects a sub-clock as the CPU operating clock.	H'FFF0 Bit 3	1

Register		Function	Address	Setting
SYSCR2	DTON	System control register 2 (Direct transfer on flag) Specifies whether or not a mode transition among active (high speed) mode, active (middle speed) mode , and sub-active mode can be performed directly by executing the SLEEP instruction. DTON = 0: When the SLEEP instruction is executed in active mode, generates a transition to standby mode, watch mode, or sleep mode. DTON = 1: When the SLEEP instruction is executed in active (high-speed) mode, generates a direct transition to active (middle speed) mode (when SSBY = 0, MSON = 1, and LSON = 0) or sub-active mode (when SSBY = 1, TMA = 1, and LSON = 1).	H'FFF1 Bit 3	0
	MSON	System control register 2 (Middle speed on flag) Selects whether the MCU operates in active (high speed) mode or in active (middle speed) mode after standby mode, watch mode, or sleep mode is cancelled. MSON = 0: Operates in active (high speed) mode MSON = 1: Operates in active (middle speed) mode	H'FFF1 Bit 2	0
TMA	TMA3	Timer mode register A (Timer mode register A3) Selects a clock source to be input to timer counter A. TMA3 = 0: Selects PSS as a TCA input clock source. TMA3 = 1: Selects PSW as a TCA input clock source.	H'FFB0 Bit 3	1

4.4 RAM

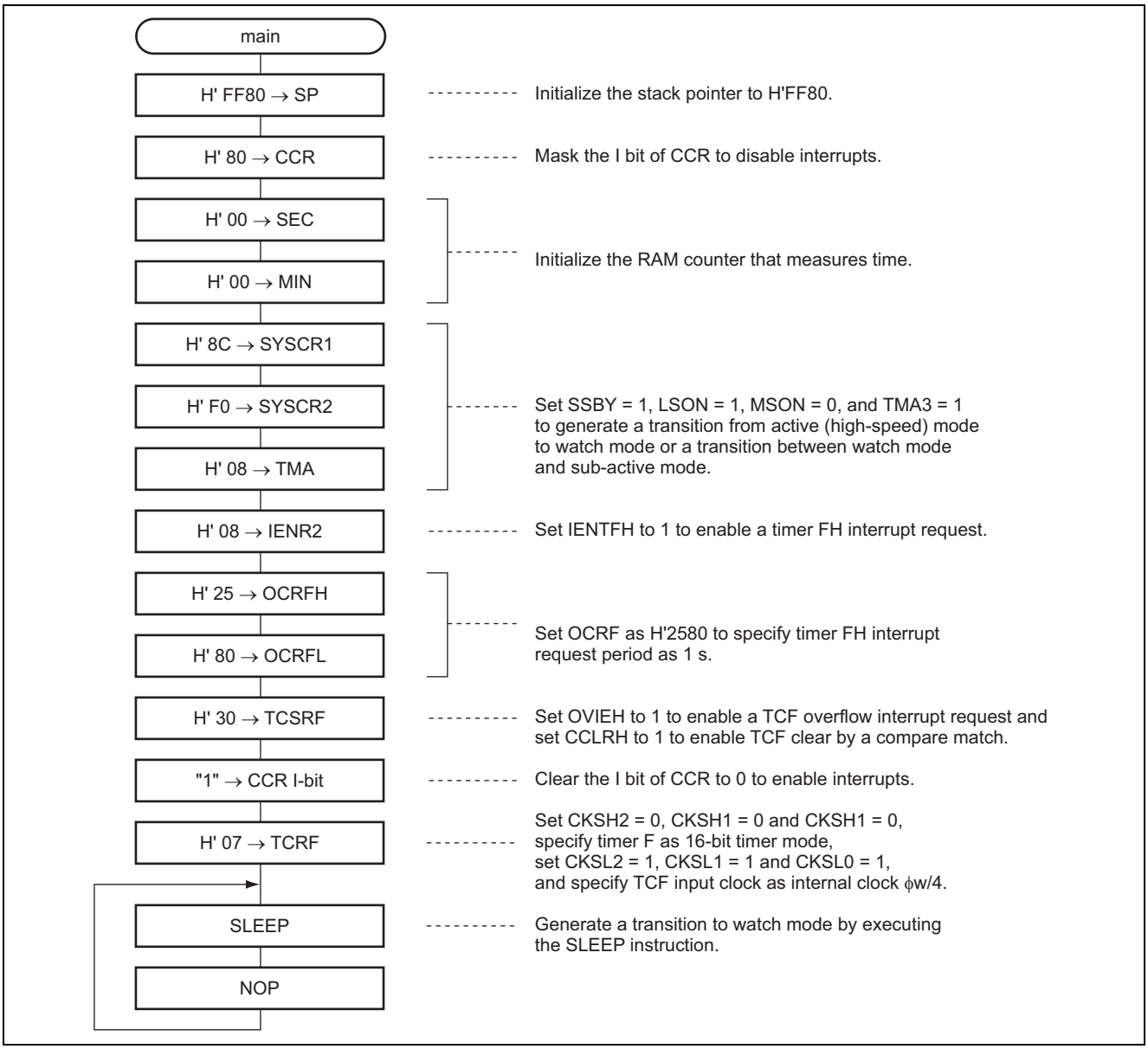
Table 7 describes the RAM used in this sample task.

Table 7 Description of RAM Used

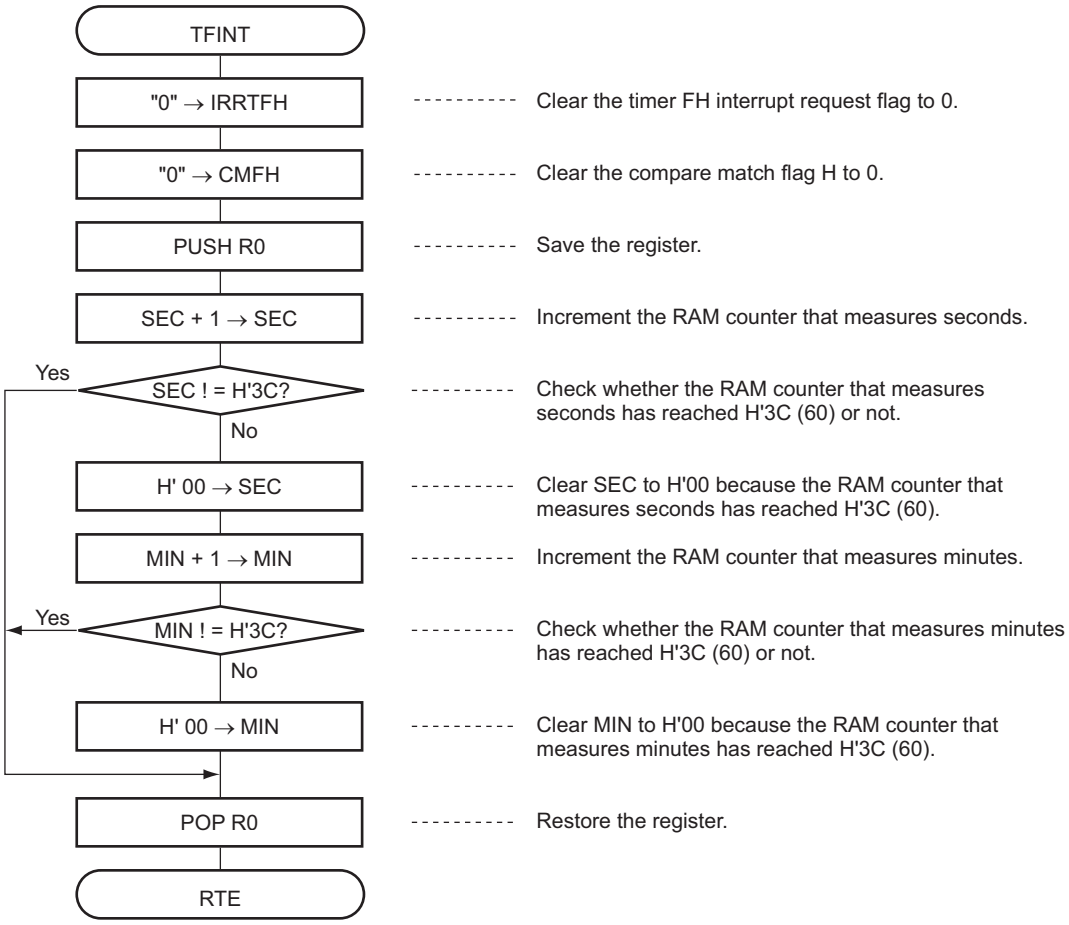
Label	Function	Address	Used in
SEC	A timer counter that counts seconds.	H'F780	MAIN, TFINT
MIN	A timer counter that counts minutes.	H'F781	MAIN, TFINT

5. Flowchart

1. Main routine



2. Timer F interrupt processing routine



6. Program Listing

```
;*********************************************************************************************
;*      H8/3867 Application Note                                                             *
;*                                                                                           *
;*      'Timer F -Clock Time Base-'                                                          *
;*                                                                                           *
;*      Function : Timer F                                                                   *
;*                                                                                           *
;*      External Clock : 6MHz                                                                *
;*      Internal Clock : 3MHz                                                                *
;*      Sub Clock :      38.4kHz                                                             *
;*********************************************************************************************
;
          .cpu          300L
;
;*********************************************************************************************
;*  Symbol Defnition                                                                         *
;*********************************************************************************************
;
TMA       .equ          h'ffb0                    ;Timer Mode Register A
TCRF      .equ          h'ffb6                    ;Timer Control Register F
TCSRF     .equ          h'ffb7                    ;Timer Control/Status Register F
TCFH      .equ          h'ffb8                    ;8-bit Timer Counter FH
TCFL      .equ          h'ffb9                    ;8-bit Timer Counter FL
OCRFH     .equ          h'ffba                    ;Output Compare Register FH
OCRFL     .equ          h'ffbb                    ;Output Compare Register FL
SYSCR1    .equ          h'fff0                    ;System Control Register 1
SYSCR2    .equ          h'fff1                    ;System Control Register 2
IENR2     .equ          h'fff4                    ;Interrupt Enable Register 2
IRR2      .equ          h'fff7                    ;Interrupt Request Register 2
;
;*********************************************************************************************
;*RAM Allocation                                                                             *
;*********************************************************************************************
;
SEC       .equ          h'f780                    ;Second Counter
MIN       .equ          h'f781                    ;Minute Counter
;
;*********************************************************************************************
;*  Vector Address                                                                           *
;*********************************************************************************************
;
          .org          h'0000
          .data.w       MAIN                      ;No.0 Reset Interrupt(H'0000-H'0001)
;
          .org          h'0008
          .data.w       MAIN                      ;No.4 _IRQ0 Interrupt(H'0008-H'0009)
          .data.w       MAIN                      ;No.5 _IRQ1 Interrupt(H'000A-H'000B)
          .data.w       MAIN                      ;No.6 _IRQ2 Interrupt(H'000C-H'000D)
          .data.w       MAIN                      ;No.7 _IRQ3 Interrupt(H'000E-H'000F)
          .data.w       MAIN                      ;No.8 _IRQ4 Interrupt(H'0010-H'0011)
          .data.w       MAIN                      ;No.9 _WKP0-_WKP7 Interrupt(H'0012-H'0013)
;
```

```
          .org          h'0016
          .data.w       MAIN                    ;No.11 Timer A Interrupt(H'0016-H'0017)
          .data.w       MAIN                    ;No.12 AEC Interrupt(H'0018-H'0019)
          .data.w       MAIN                    ;No.13 Timer C Interrupt(H'001A-H'001B)
          .data.w       MAIN                    ;No.14 Timer FL Interrupt(H'001C-H'001D)
          .data.w       TFINT                   ;No.15 Timer FH Interrupt(H'001E-H'001F)
          .data.w       MAIN                    ;No.16 Timer G Interrupt(H'0020-H'0021)
          .data.w       MAIN                    ;No.17 SCI31 Interrupt(H'0022-H'0023)
          .data.w       MAIN                    ;No.18 SCI32 Interrupt(H'0024-H'0025)
          .data.w       MAIN                    ;No.19 A/D Converter Interrupt(H'0026-H'0028)
          .data.w       MAIN                    ;No.20 Direct Transfer Interrupt(H'0028-H'0029)
;
;*********************************************************************************************
;*  MAIN : Main Routine                                                                      *
;*********************************************************************************************
;
          .org          h'1000
;
MAIN:     .equ          $
          mov.w         #H'ff80,sp              ;Initialize Stack Pointer
          orc           #h'80,ccr               ;Interrupt Disable
;
          sub.b         r0l,r0l                 ;Initialize RAM
          mov.b         r0l,@SEC
          mov.b         r0l,@MIN
;
          mov.b         #h'8c,r0l               ;Initialize System Control
          mov.b         r0l,@SYSCR1
          mov.b         #h'f0,r0l
          mov.b         r0l,@SYSCR2
          mov.b         #h'08,r0l
          mov.b         r0l,@TMA
;
          mov.b         #h'08,r0l               ;Timer F Interrupt Enable
          mov.b         r0l,@IENR2
;
          mov.b         #h'25,r0h               ;Initialize Timer F
          mov.b         #h'80,r0l
          mov.b         r0h,@OCRFH
          mov.b         r0l,@OCRFL
          mov.b         #h'30,r0l
          mov.b         r0l,@TCSRF
;
          andc          #h'7f,ccr               ;Interrupt Enable
;
          mov.b         #h'07,r0l               ;Initialize TCFL Input Clock
          mov.b         r0l,@TCRF
;
LOOP:     sleep                                 ;Transfer to Watch Mode
          nop
          bra           LOOP
;
```

```
;*********************************************************************************************
;*  TFINT : Timer F Interrupt Routine                                                        *
;*********************************************************************************************
;
TFINT:    .equ          $
          Bclr          #3,@IRR2              ;Clear Timer F Interrupt Request Flag
          Bclr          #6,@TCSRF             ;Clear Compare Match Flag H
;
          push          r0                    ;Store r0
;
          mov.b         @SEC,r0l              ;Load Second Counter
          mov.b         @MIN,r0h              ;Load Minute Counter
          inc           r0l                   ;Increment Second Counter
          cmp.b         #h'3c,r0l             ;@SEC = d'60 ?
          bne           INTEXT                ;No. Exit
          mov.b         #h'00,r0l             ;Yes. Initialize Second Counter
          inc           r0h                   ;Increment Minute Counter
          cmp.b         #h'3c,r0h             ;@MIN = d'60 ?
          bne           INTEXT                ;No. Exit
          mov.b         #h'00,r0h             ;Yes. Initialize Minute Counter
;
INTEXT:   mov.b         r0h,@MIN              ;Store Minute Counter
          mov.b         r0l,@SEC              ;Store Second Counter
;
          pop           r0                    ;Restore r0
;
          rte
;
          .end
```

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