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Renesas Electronics Corporation

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H8/300H Tiny Series

Using Single Mode A/D Conversion to Measure Voltage

Introduction

The input voltage on one channel is measured by using the A/D converter of the H8/3664.

Target Device

H8/3664

Contents

1. Specifications

1. The input voltage on one channel is measured by using the A/D converter of the H8/3664 as shown in figure 1.1.
2. When the switch (SW) connected to the $\overline{\text{ADTRG}}$ pin is turned on, A/D conversion is performed on the voltage input to AN0.
3. The result of A/D conversion is stored in RAM.

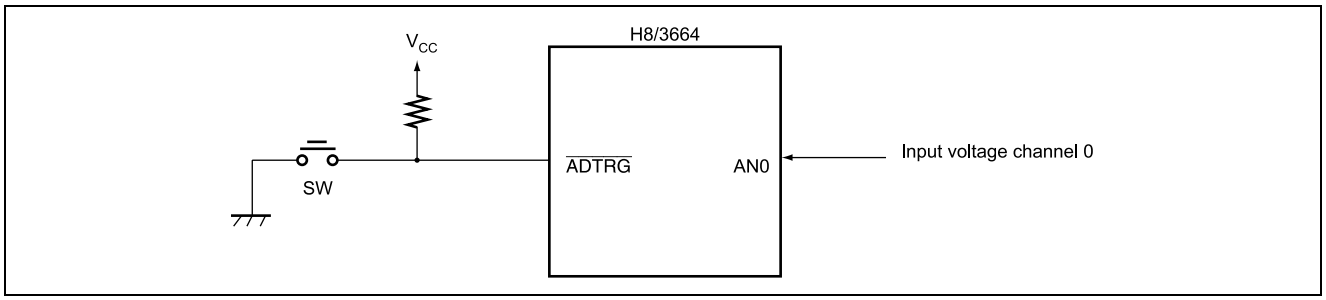


Figure 1.1 Voltage Measurement by Single Mode A/D Conversion

2. Description of Functions

1. In this sample task, the voltage on one channel is measured using the A/D converter. Figure 2.1 is a block diagram of the A/D converter. The elements of the block diagram are described below.

- The A/D data register (ADDRA) is a 16-bit read-only register used to store the result of A/D conversion. The converted 10-bit data is stored in bits 15 to 6 of the ADDRA. The lower 6 bits are always read as 0. The data bus between the CPU and the A/D converter is 8 bits wide. The upper byte can be read directly from the CPU, however the lower byte should be read via a temporary register. The temporary register contents are transferred from the ADDRA when the upper byte of data is read. When reading from ADDRA, read the upper byte only or read in word units. The initial value of ADDRA is 0x0000.
- The A/D control/status register (ADCSR) contains the control bits and conversion end status bits of the A/D converter.
- The A/D control register (ADCR) controls starting of A/D conversion by an external trigger. In this task, the start of A/D conversion by an $\overline{\text{ADTRG}}$ external input trigger is enabled.
- Analog input pin 0 (AN0) is the pin for input voltage channel 0.
- The A/D external trigger input pin ($\overline{\text{ADTRG}}$) is the pin to which triggers for starting A/D conversion are input.

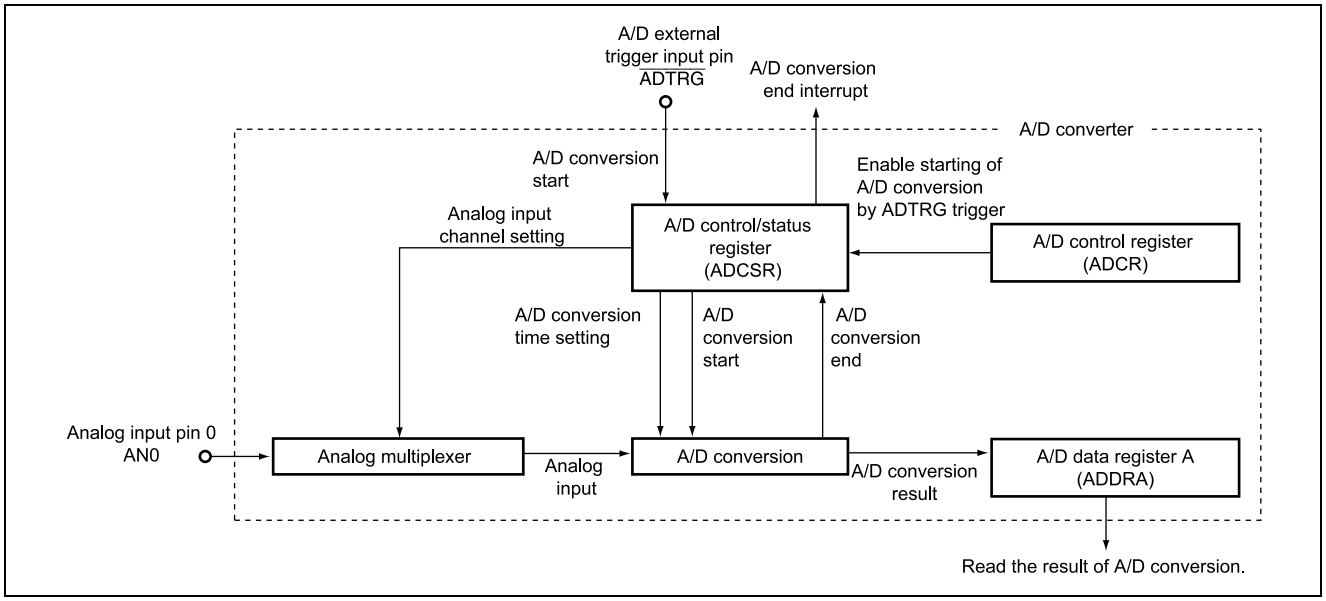


Figure 2.1 Block Diagram of the A/D Converter

2. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so as to measure the voltage on one channel.

Table 2.1 Function Allocation

Function	Description
ADCSR	Starts or stops A/D conversion, indicates the status of A/D conversion, and sets the analog input pin.
ADDRA	Stores the result of A/D conversion.
ADCR	Enables the start of A/D conversion by the external trigger ($\overline{\text{ADTRG}}$ pin).
$\overline{\text{ADTRG}}$ pin	Starts A/D conversion on the falling edge of the $\overline{\text{ADTRG}}$ pin.
AN0	Input pin for input voltage channel 0
AV_{CC}	Power supply and reference voltage pin for the analog block
AV_{SS}	Ground and reference voltage pin for the analog block

3. Description of Operation

Operation of this sample task is described in figure 3.1. Hardware and software processing are applied in the way shown in figure 3.1 to measure the voltage on one channel by single-mode A/D conversion.

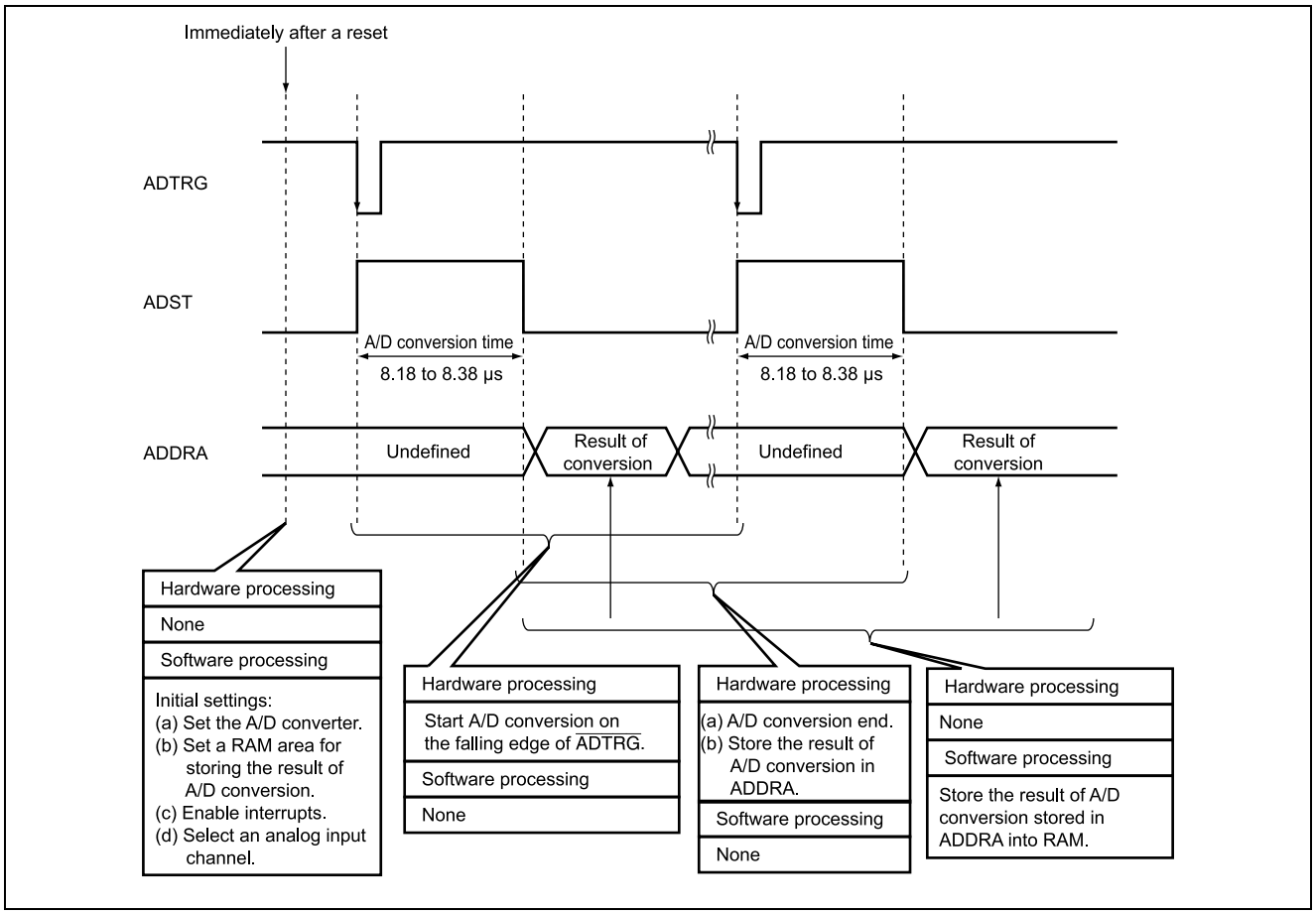


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 describes the software modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets the A/D converter, enables interrupts, selects an analog input channel, and enables starting of A/D conversion by the $\overline{\text{ADTRG}}$ pin.
A/D conversion end	adcinit	Transfers the result of A/D conversion that is stored in ADDRA to RAM after A/D conversion has ended.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- ADDRA A/D data register Address: 0xFFB0
  Function: Stores the 16-bit data which is the result of A/D conversion.
  Setting: —

- ADCSR A/D control/status register Address: 0xFFB8

Bit	Bit Name	Setting	Function
7	ADF	0	A/D end flag ADF = 0: A/D conversion is being performed in single mode. ADF = 1: A/D conversion has ended in single mode.
6	ADIE	1	A/D interrupt enable ADIE = 0: Disables A/D conversion end interrupt requests by ADF (ADI). ADIE = 1: Enables A/D conversion end interrupt requests by ADF (ADI).
5	ADST	0	A/D start ADST = 0: A/D conversion is stopped in single mode. ADST = 1: A/D conversion starts.
4	SCAN	0	Scan mode SCAN = 0: Single mode is selected. SCAN = 1: Scan mode is selected.
3	CKS	0	Clock select CKS = 0: A/D conversion time is set to 134 clock cycles (max.). CKS = 1: A/D conversion time is set to 70 clock cycles (max.).
2	CH2	CH2 = 0	Channel select 2 to 0
1	CH1	CH1 = 0	CH2 = 0, CH1 = 0, CH0 = 0: AN0 is selected as an analog input channel.
0	CH0	CH0 = 0	

- ADCR A/D control register Address: 0xFFB9

Bit	Bit Name	Setting	Function
7	TRGE	1	Trigger enable TRGE = 0: $\overline{\text{ADTRG}}$ input is invalid. TRGE = 1: A/D conversion starts on the falling edge of $\overline{\text{ADTRG}}$.

- PMR5 Port mode register 5 Address: 0xFFDB

Bit	Bit Name	Setting	Function
5	WKP5	1	P55/$\overline{\text{WKP5}}$ pin function switch WKP5 = 0: P55 input/output pin WKP5 = 1: $\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ input pin.

- IEGR2 Interrupt edge select register 2 Address: 0xFFF3

Bit	Bit Name	Setting	Function
5	WPEG5	1	WKP5 edge select WPEG5 = 0: The falling edge of $\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ pin input is detected. WPEG5 = 1: The rising edge of $\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ pin input is detected.

4.4 Description of RAM

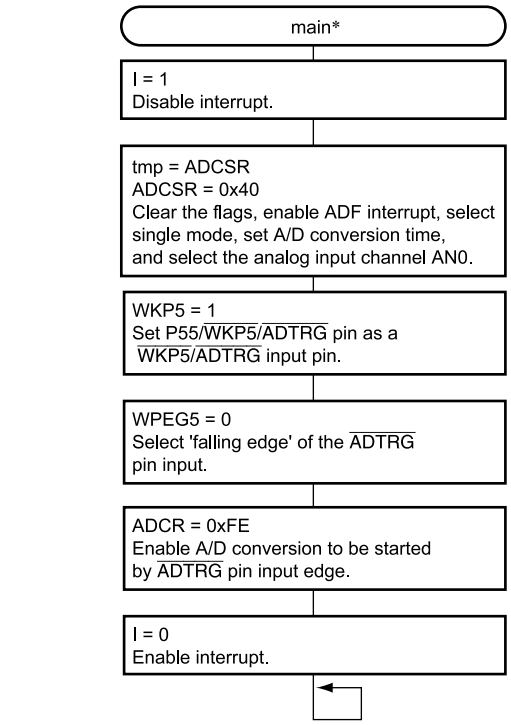
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
addata	Stores the result of A/D conversion on AN0.	2 bytes	A/D conversion end

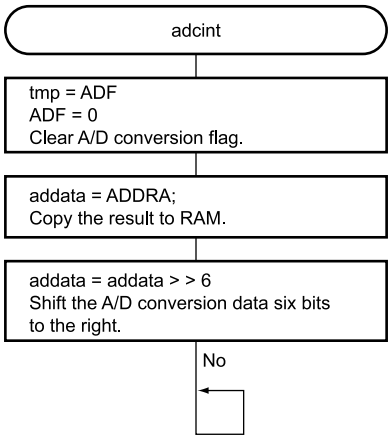
5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

2. A/D Conversion End



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3664-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Voltage Measurement by 1-Channel A/D Converter'                                                                   */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : A/D Converter                                                                                                    */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :         32.768kHz                                                                                      */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        ADDRA          *(volatile unsigned short *)0xFFB0              /* A/D Data Register A                  */
#define        ADCSR          *(volatile unsigned char *)0xFFB8               /* A/D Control/Status Register          */
#define        ADCSR_BIT      (*(struct BIT *)0xFFB8)                         /* A/D Control/Status Register          */
#define        ADF            ADCSR_BIT.b7                                    /* A/D END Flag                         */
#define        ADIE           ADCSR_BIT.b6                                    /* A/D Interrupt Enable                 */
#define        ADST           ADCSR_BIT.b5                                    /* A/D Start                            */
#define        SCAN           ADCSR_BIT.b4                                    /* A/D Scan Mode                        */
#define        CKS            ADCSR_BIT.b3                                    /* A/D Clock Select                     */
#define        CH2            ADCSR_BIT.b2                                    /* Channel Select 2                     */
#define        CH1            ADCSR_BIT.b1                                    /* Channel Select 1                     */
#define        CH0            ADCSR_BIT.b0                                    /* Channel Select 0                     */
#define        ADCR           *(volatile unsigned char *)0xFFB9               /* A/D Control/Status Register          */
#define        PMR5           *(volatile unsigned char *)0xFFE1               /* Port Mode Register 5                 */
#define        PMR5_BIT       (*(struct BIT *)0xFFE1)                         /* Port Mode Register 5                 */
#define        WKP5           PMR5_BIT.b5                                     /* function of pin Wakeup5 bit5         */
#define        IEGR2_BIT      (*(struct BIT *)0xFFF3)                         /* Interrupt Edge Select Register 2     */
#define        WPEG5          IEGR2_BIT.b5                                    /* WKP5 Edge Select                     */

#pragma interrupt   (adcint)
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                    /* SP Set                               */
void main ( void );
void adcint ( void );
```

```
/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned short addata;

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                  /* VECTOR SECTOIN SET                    */
void (*const VEC_TBL1[])(void) = {                                      /* 0x00 - 0x0f                           */
     INIT                                                               /* 00 Reset                              */
};
#pragma section     V2                                                  /* VECTOR SECTOIN SET                    */
void (*const VEC_TBL2[])(void) = {
     adcint                                                             /* 32 A/D Converter Interrupt            */
};

#pragma section                                                         /* P                                     */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                                  /* Interrupt Disable                     */

     tmp = ADCSR;                                                       /* Clear Flag , Select Single mode       */
     ADCSR = 0x40;                                                      /* A/D convertion Time , AN0             */
     WKP5 = 1;                                                          /* ~WKP5/~ADTRG input pin                */
     WPEG5 = 0;                                                         /* ADTRG pin is Falling edge             */
     ADCR = 0xFE;                                                       /* A/D conversion is started             */
                                                                        /* at the edge of ~ADTRG                 */
     set_imask_ccr(0);                                                  /* Interrupt Enable                      */
     while(1);
}

/************************************************************************************************************************/
/*   A/D Converter Interrupt                                                                                            */
/************************************************************************************************************************/
void adcint ( void )
{
     unsigned char tmp;

     tmp = ADF;
     ADF = 0;
     addata = ADDRA;                                                    /* Save A/D Convert Data                 */
     addata = addata>>6;
}
```

Link Address Setting:

Section Name	Address
CV1	0x0000
CV2	0x0032
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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