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RENESAS

H8/300L SLP Series

Using External Expansion of Segment Data in Driving an LCD (H8/3867)

Introduction

The LCD display is performed by using the H8/3867-series segment-type LCD control circuit, LCD driver, and power supply circuit. The timer B1 interval function is used to increment an 8-bit counter specified in RAM.

Target Device

H8/3867

Contents

1. Specifications

1. The LCD display is performed by using the H8/3867-series segment-type LCD control circuit, LCD driver, and power supply circuit.
2. The HD66100 is connected to the H8/3867 to perform segment extension and to perform the LCD display.
3. An 8-digit 16 segment LCD display is performed with duty cycle of 1/4.
4. Vcc is used as the LCD drive power supply.
5. Figure 1.1 shows an example of liquid crystal display module and HD66100 connection, and an example of LCD display in this sample task.

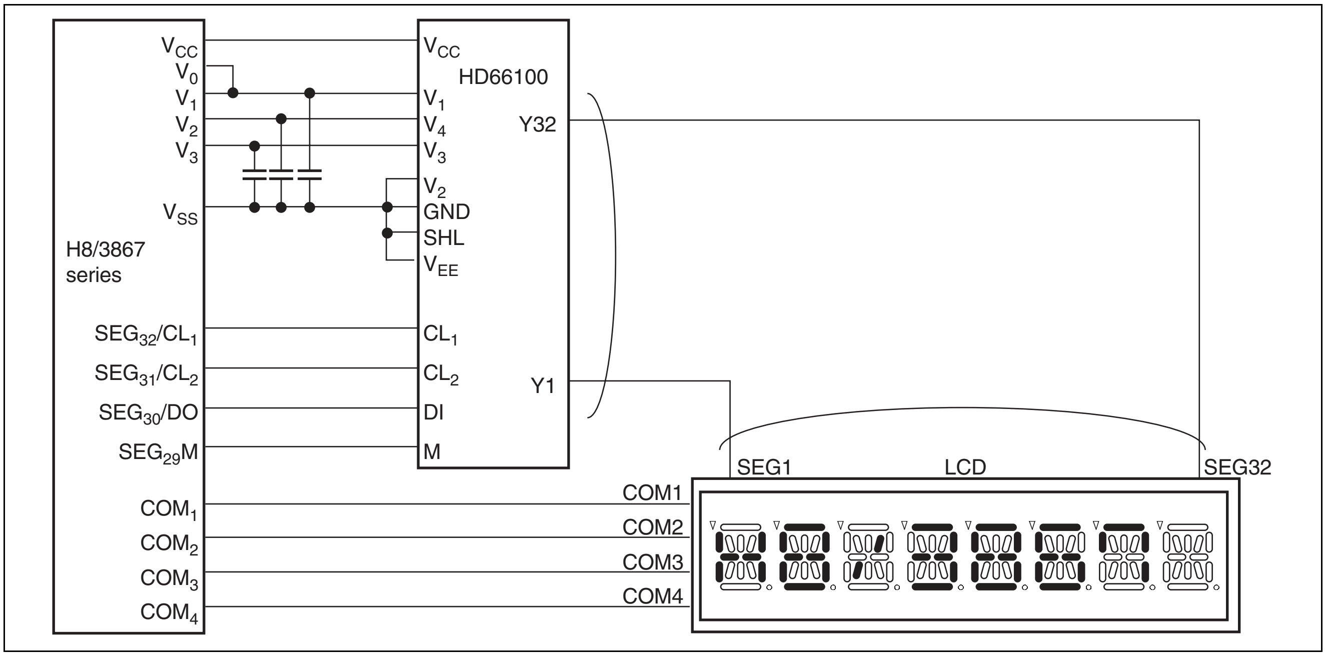


Figure 1.1 Examples of HD66100 and LCD Module Connection by Segment Extension, and LCD Display

2. Description of Functions

1. In this sample task, the LCD display is performed by using the LCD controller/driver. The characteristics of the LCD controller/driver are shown below.
   - Display size
     - A. Duty cycle: 1 (static)
       To internal driver: 32 SEG   Segment external extension driver: 256 SEG
     - B. Duty cycle: 1/2 static drive
       To internal driver: 32 SEG   Segment external extension driver: 128 SEG
     - C. Duty cycle: 1/3 static drive
       To internal driver: 32 SEG   Segment external extension driver: 64 SEG
     - D. Duty cycle: 1/4 static drive
       To internal driver: 32 SEG   Segment external extension driver: 64 SEG
   - LCD RAM size: 8 bits x 32 bytes (256 bits)
   - The LCD RAM can be accessed in word units.
   - The segment output pins can be used as ports in 8-pin units.
   - The segment output pins can be used as ports in 8-pin units.
   - Common output pins not used according to the duty cycle can be used as common double buffer pins (for parallel connection).
   - The LCD display can be performed in the operating modes other than standby mode.
   - The frame frequency can be specified as one of 11 frequencies.
   - The power supply dividing resistor is incorporated in the MCU to supply LCD drive power.
   - This module can be specified in standby mode while it is not used by module standby mode.
   - The step-up constant-voltage (5 V) power supply is incorporated to enable LCD display even when power supply is stopped.
   - Either A or B waveform can be selected by software.

2. Figure 2.1 shows the block diagram of the LCD controller/driver during segment external extension used in this sample task.

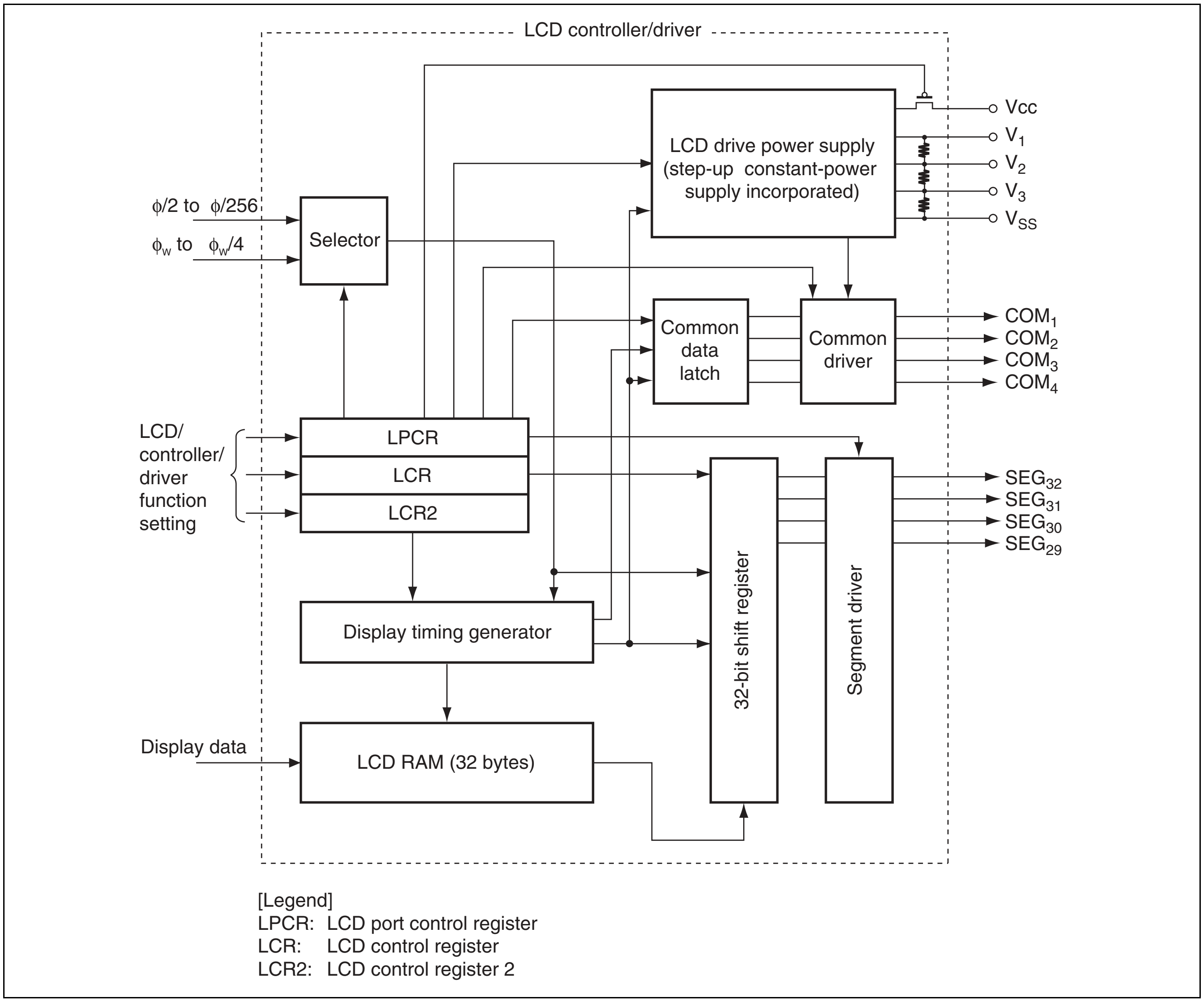


Figure 2.1 Block Diagram of LCD Controller/Driver in Segment External Extension

3. Table 2.1 describes the functions of LCD controller/driver.

Table 2.1 LCD Controller/drier Functions

Register	Function
LCD port control register (LPCR)	The CPCR is an 8-bit readable/writable register that selects duty cycle, LCD driver, and pin functions. It is initialized to H'00 at reset.
LCD control register (LCR)	The LCR is an 8-bit readable/writable register that controls the LCD drive power supply ON/OFF and display data, and selects a frame frequency. It is initialized to H'80 at reset.
LCD control register 2 (LCR2)	The LCR2 is an 8-bit readable/writable register that controls switching between the A waveform and B waveform, selects the drive power supply, controls the step-up constant-voltage (5 V) power supply, and selects the duty cycle of the charge/discharge pulses that control disconnection of the power supply split-resistor from the power supply circuit. It is initialized to H'60 at reset.
Common output pin (COM_4 to COM_1)	COM_4 to COM_1 are liquid crystal common drive pins that can be used in parallel for double buffering in static or 1/2 duty cycle.
Segment external extension signal pin (CL_1)	CL_1 is a display data latch clock. It is multiplexed with SEG_{32}.
Segment external extension signal pin (CL_2)	CL_2 is a display data latch clock. It is multiplexed with SEG_{31}.
Segment external extension signal pin (M)	M is an LCD current-alternating signal. It is multiplexed with SEG_{29}.
Segment external extension signal pin (D0)	D0 is a serial display data. It is multiplexed with SEG_{30}.
LCD power supply pins (V_0, V_1, V_2, V_3)	V_0, V_1, V_2, and V_3 are used when an external power supply circuit is used, or when an external bypass capacitor is connected.
LCD RAM	The LCD RAM specifies the display data. The relationship between the LCD RAM and display segments differs depending on the duty cycle. After specifying the registers necessary for LCD display, data is written to the LCD RAM corresponding to the selected duty cycle by an instruction in the same way as data is written to normal RAM, and turn on the display to start LCD display automatically. Word or byte access instructions can be used for RAM settings.

4. In this sample task, the 8-digit 16-segment LCD display is performed with 1/4 duty cycle by segment external extension. Figure 2.2 shows the connection between the segment signals and common signals of 8-digit 16-segment LCD used in this sample task.

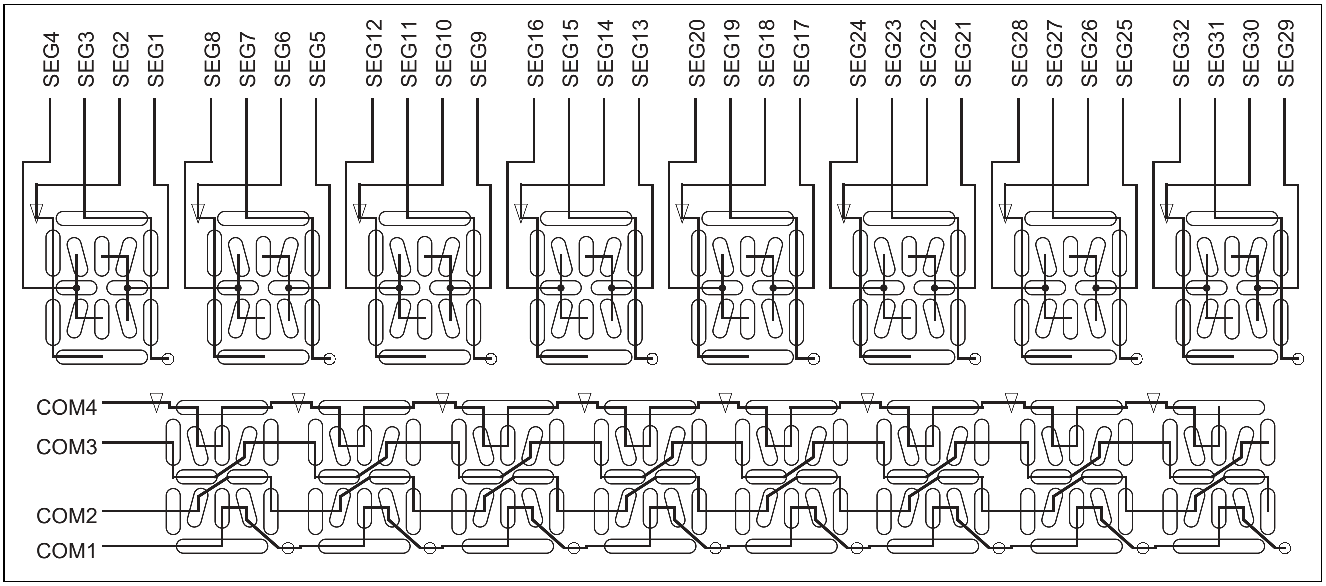


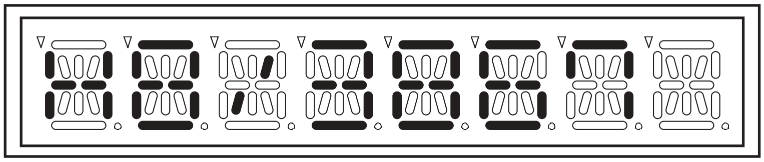
Figure 2.2 Connection between Segment Signals and Common Signals of 8-Digit 16-Segment LCD Used in this Sample Task.

5. Figure 2.3 shows the LCD RAM map at 1/4 duty cycle with segment external extension.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H'F740	SEG_2	SEG_2	SEG_2	SEG_2	SEG_1	SEG_1	SEG_1	SEG_1
H'F741	SEG_4	SEG_4	SEG_4	SEG_4	SEG_3	SEG_3	SEG_3	SEG_3
H'F742	SEG_6	SEG_6	SEG_6	SEG_6	SEG_5	SEG_5	SEG_5	SEG_5
H'F743	SEG_8	SEG_8	SEG_8	SEG_8	SEG_7	SEG_7	SEG_7	SEG_7
H'F744	SEG_{10}	SEG_{10}	SEG_{10}	SEG_{10}	SEG_9	SEG_9	SEG_9	SEG_9
H'F745	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{12}	SEG_{11}	SEG_{11}	SEG_{11}	SEG_{11}
H'F746	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{14}	SEG_{13}	SEG_{13}	SEG_{13}	SEG_{13}
H'F747	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{16}	SEG_{15}	SEG_{15}	SEG_{15}	SEG_{15}
H'F748	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{18}	SEG_{17}	SEG_{17}	SEG_{17}	SEG_{17}
H'F749	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{20}	SEG_{19}	SEG_{19}	SEG_{19}	SEG_{19}
H'F74A	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{22}	SEG_{21}	SEG_{21}	SEG_{21}	SEG_{21}
H'F74B	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{24}	SEG_{23}	SEG_{23}	SEG_{23}	SEG_{23}
H'F74C	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{26}	SEG_{25}	SEG_{25}	SEG_{25}	SEG_{25}
H'F74D	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{28}	SEG_{27}	SEG_{27}	SEG_{27}	SEG_{27}
H'F74E	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{30}	SEG_{29}	SEG_{29}	SEG_{29}	SEG_{29}
H'F74F	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{32}	SEG_{31}	SEG_{31}	SEG_{31}	SEG_{31}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H'F75F	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}	SEG_{64}
	↓ COM_4	↓ COM_3	↓ COM_2	↓ COM_1	↓ COM_4	↓ COM_3	↓ COM_2	↓ COM_1

Figure 2.3 LCD RAM Map at 1/4 Duty Cycle with Segment External Extension

6. Figure 2.4 shows the relationship between the 8-digit 16-segment LCD display and LCD RAM setting values used in this sample task. "H8/3867" is displayed on the LCD by setting the LCD RAM.



	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'F740	0	1	1	0	0	0	1	0	"H" display data
H'F741	0	1	0	0	0	1	1	0	
H'F742	0	1	1	1	0	0	1	0	"8" display data
H'F743	0	1	0	0	1	1	1	0	
H'F744	0	0	0	0	0	1	0	0	"/" display data
H'F745	0	0	1	0	0	0	0	0	
H'F746	0	0	0	1	0	0	1	0	"3" display data
H'F747	0	1	0	0	1	1	1	0	
H'F748	0	1	1	1	0	0	1	0	"8" display data
H'F749	0	1	0	0	1	1	1	0	
H'F74A	0	1	1	1	0	0	1	0	"6" display data
H'F74B	0	1	0	0	1	0	1	0	
H'F74C	0	1	0	0	0	0	0	0	"7" display data
H'F74D	0	0	0	0	1	1	1	0	
H'F74E	0	0	0	0	0	0	0	0	" " display data*
H'F74F	0	0	0	0	0	0	0	0	

Note: * " " indicates a blank.

Figure2.4 Relationship between the LCD Display and the LCD RAM Settings

7. Figure 2.5 shows the relationship between the leftmost digit of the 8-digit 16-segment LCD and LCD RAM setting values corresponding to SEG_1 to SEG_4. As shown in figure 6, when the bits in LCD RAM corresponding to 0 to f are set to 1, the corresponding LCDs light up; while bits in LCD RAM corresponding to 0 to f are cleared to 0, the corresponding LCDs do not light up.

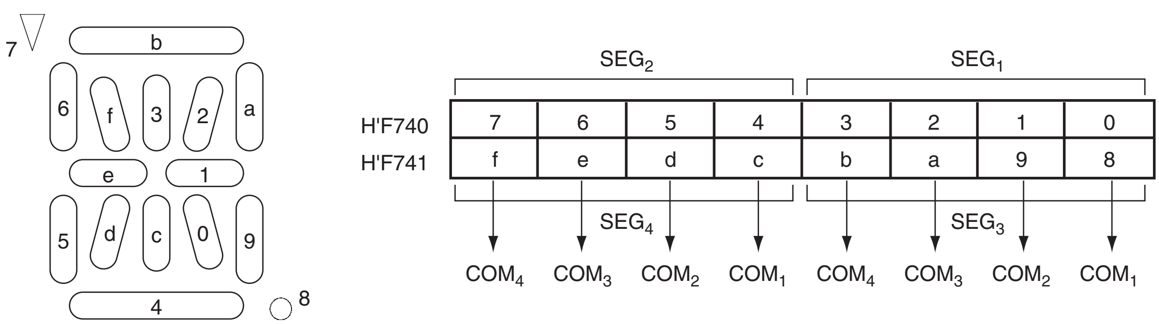


Figure 2.5 Relationship between LCD Light On/Off and Corresponding LCD RAM Setting Values

8. Table 2.2 shows an example of SEG1 to SEG4 display of 8-digit 16-segment LCD and display data.

Table 2.2 Example of SEG1 to SEG4 Display and Display Data

Symbol	Display	Address	Display Data							
		H'F740	0	0	0	0	0	0	0	0
		H'F741	0	0	0	0	0	0	0	0
*		H'F740	0	0	0	0	1	1	1	1
		H'F741	1	1	1	1	0	0	0	0
–		H'F740	0	0	0	0	0	0	1	0
		H'F741	0	1	0	0	0	0	0	0
/		H'F740	0	0	0	0	0	1	0	0
		H'F741	0	0	1	0	0	0	0	0
0		H'F740	0	1	1	1	0	1	0	0
		H'F741	0	0	1	0	1	1	1	0
1		H'F740	0	0	0	0	0	0	0	0
		H'F741	0	0	0	0	0	1	1	0
2		H'F740	0	0	1	1	0	0	1	0
		H'F741	0	1	0	0	1	1	0	0
3		H'F740	0	0	0	1	0	0	1	0
		H'F741	0	1	0	0	1	1	0	0
4		H'F740	0	1	0	0	0	0	1	0
		H'F741	0	1	0	0	0	1	1	0
5		H'F740	0	1	0	1	0	0	1	0
		H'F741	0	1	0	0	1	0	1	0
6		H'F740	0	1	1	1	0	0	1	0
		H'F741	0	1	0	0	0	0	1	0
7		H'F740	0	1	0	0	0	0	0	0
		H'F741	0	0	0	0	1	1	1	0
8		H'F740	0	1	1	1	0	0	1	0
		H'F741	0	1	0	0	1	1	1	0
9		H'F740	0	1	0	0	0	0	1	0
		H'F741	0	1	0	0	1	1	1	0
A		H'F740	0	1	1	0	0	0	1	0
		H'F741	0	1	0	0	1	1	1	0
B		H'F740	0	0	0	1	1	1	0	0
		H'F741	0	0	0	1	1	1	1	0
C		H'F740	0	1	1	1	0	0	0	0
		H'F741	0	0	0	0	1	0	0	0
D		H'F740	0	0	0	1	1	0	0	0
		H'F741	0	0	0	1	1	1	1	0
E		H'F740	0	1	1	1	0	0	1	0
		H'F741	0	1	0	0	1	0	0	0
F		H'F740	0	1	1	0	0	0	1	0
		H'F741	0	1	0	0	1	0	0	0
G		H'F740	0	1	1	1	0	0	1	0
		H'F741	0	0	0	0	1	0	1	0
H		H'F740	0	1	1	0	0	0	1	0
		H'F741	0	1	0	0	0	1	1	0
I		H'F740	0	0	0	1	1	0	0	0
		H'F741	0	0	0	1	1	0	0	0
J		H'F740	0	0	1	1	1	0	0	0
		H'F741	0	0	0	1	1	0	0	0
K		H'F740	0	1	1	0	0	1	0	1
		H'F741	0	1	0	0	0	0	0	0
L		H'F740	0	1	1	1	0	0	0	0
		H'F741	0	0	0	0	0	0	0	0
M		H'F740	0	1	1	0	0	1	0	0
		H'F741	1	0	0	0	0	1	1	0
N		H'F740	0	1	1	0	0	0	0	1
		H'F741	1	0	0	0	0	1	1	0
O		H'F740	0	1	1	1	0	0	0	0
		H'F741	0	0	0	0	1	1	1	0
P		H'F740	0	1	1	0	0	0	1	0
		H'F741	0	1	0	0	1	1	0	0
Q		H'F740	0	1	1	1	0	0	0	1
		H'F741	0	0	0	0	1	1	1	0
R		H'F740	0	1	1	0	0	0	1	1
		H'F741	0	1	0	0	1	1	0	0
S		H'F740	0	0	0	1	0	0	0	1
		H'F741	1	0	0	0	1	0	0	0
T		H'F740	0	0	0	0	1	0	0	0
		H'F741	0	0	0	1	1	0	0	0
U		H'F740	0	1	1	1	0	0	0	0
		H'F741	0	0	0	0	0	1	1	0
V		H'F740	0	1	1	0	0	1	0	0
		H'F741	0	0	1	0	0	0	0	0
W		H'F740	0	1	1	0	0	0	0	1
		H'F741	0	0	1	0	0	1	1	0
X		H'F740	0	0	0	0	0	1	0	1
		H'F741	1	0	1	0	0	0	0	0
Y		H'F740	0	0	0	0	0	1	0	0
		H'F741	1	0	0	1	0	0	0	0
Z		H'F740	0	0	0	1	0	1	0	0
		H'F741	0	0	1	0	1	0	0	0

9. Table 2.3 indicates the allocation of functions in this sample task.

Table 2.3 Function Allocation

Function	Function Allocation
LPCR	Selects duty cycle, LCD driver, and pin functions
LCR	Controls the LCD drive power supply on/off and display data, and selects a frame frequency
LCR2	Controls A/B waveform switching and step-up constant voltage (5 V) power supply, and selects drive power supply and duty cycle of charge/discharge pulse to control the disconnection of the power supply split resistor from the power supply circuit
COM_4 to COM_1	Used as common drivers
V_0 to V_3	LCD power supply pins connected to the HD66100
CL1	Display latch clock output connected to the HD66100
CL2	Display shift clock output connected to the HD66100
M	LCD current-alternating signal connected to the HD66100
D0	LCD current-alternating signal connected to the HD66100
LCD RAM	Specifies LCD display data

3. Principle of Operation

1. The following describes the hardware settings to perform LCD display.
   A. LCD drive power supply settings
   The H8/3867 series can use either on-chip power supply circuit or external power supply circuit as the LCD power supply. In addition, either power supply voltage (Vcc) or step-up constant voltage (5 V) can be selected as on-chip power supply circuit.
   To use the on-chip power supply circuit as the LCD drive power supply, the V_0 pin should be externally connected to the V_1 pin. Figure 3.1 shows an example of the V_0 pin to V_1 pin connection.
   In this sample task, the step-up constant-voltage power supply is used as the LCD drive power supply.

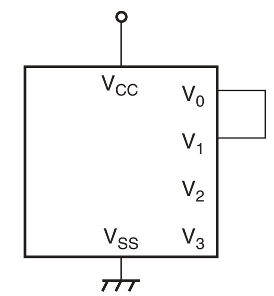


Figure 3.1 LCD Power Supply Pin Connection When the On-Chip Power Supply Circuit is Used

   B. Luminance control function
   Figure 3.2 shows the block diagram of the LCD drive power supply unit. Either Vcc or a 5-V output from the step-up constant-voltage power supply current is output to the V_0 pin. If these voltages are used directly as the LCD drive voltage, the V_0 and V_1 pins should be shorted. In addition, the voltage to be applied to the V1 pin can be adjusted by connecting the variable resistor R between the V_0 and V_1 pins, thus enabling the LCD panel luminance control.

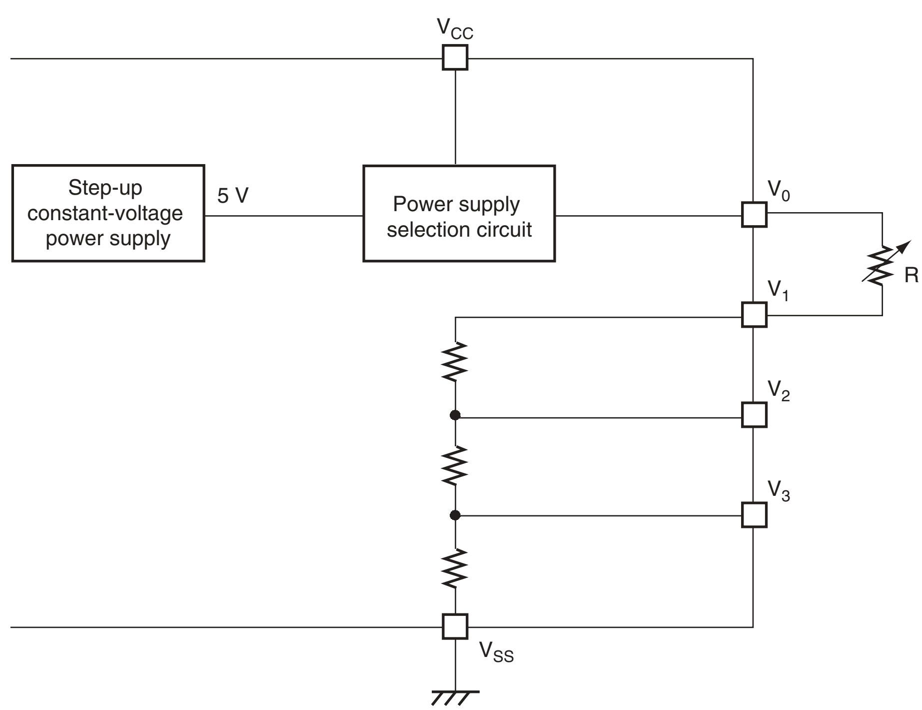


Figure 3.2 Block Diagram of LCD Drive Power Supply Unit

2. The following describes the software settings for the LCD display.
   A. Duty cycle selection
      Duty cycle can be specified as static, 1/2 duty cycle, 1/3 duty cycle, or 1/4 duty cycle via the DST1 and DST0 bits.
   B. Segment driver selection
      A segment driver to be used can be selected via the SGS3 to SGS0 bits.
   C. Frame frequency selection
      A frame frequency can be selected by setting the CKS3 to CKS0 bits. Note that a frame frequency should be specified according to the LCD panel specifications.
   D. A or B waveform selection
      An LCD waveform to be used can be specified as either an A or B waveform by the LCDAB bit.
   E. LCD drive power supply selection
      When the on-chip power supply circuit is used, power supply to be used can be selected via SUPS. When an external power supply circuit is used, the Vcc should be selected via SUPS and the LCD drive power supply should be turned off via the PSW bit.

3. Figure 3.3 shows this sample task's principle of operation.

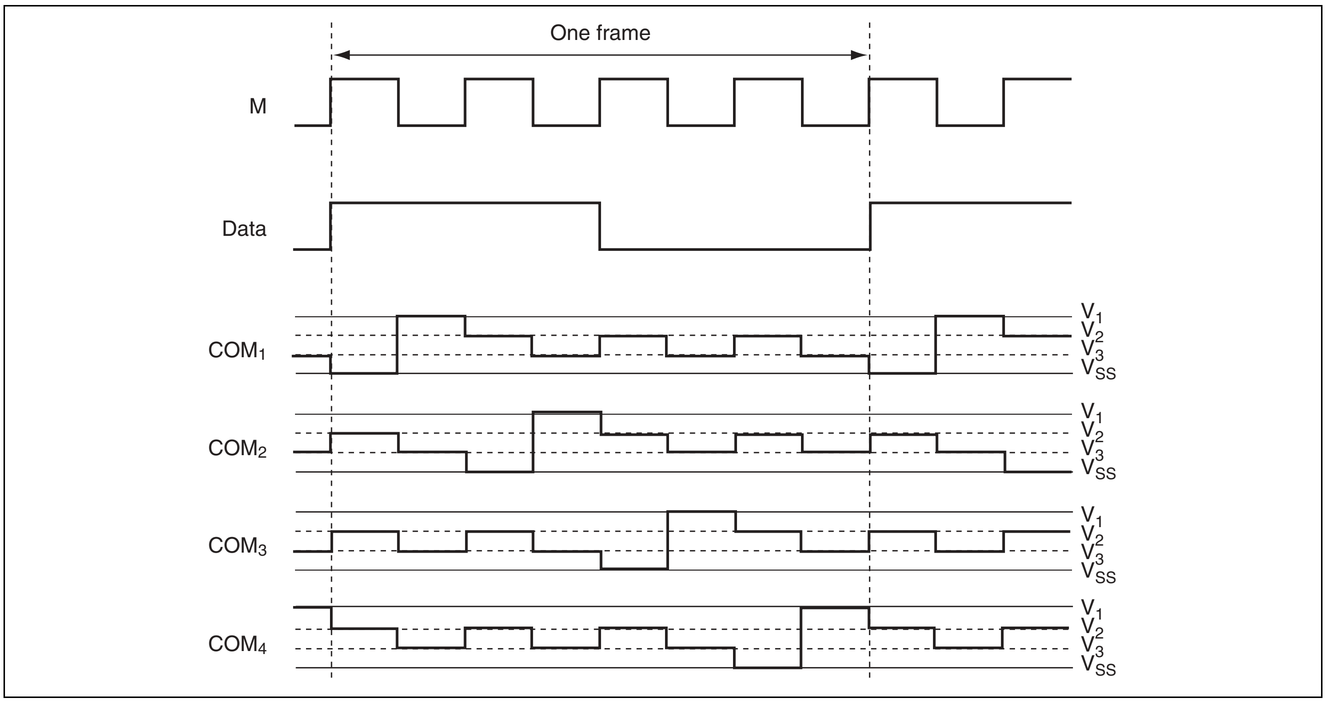


Figure 3.3 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module	Label	Function
Main routine	MAIN	Initializes the stack pointer, LCD RAM, and LCD controller/driver, and enables interrupts.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers

The internal registers used in this sample task are described in table 4.2.

Table 4.2 Description of Internal Registers

Register		Function	Address	Setting
LPCR	DTS1 DST0	LCD port control register (duty cycle selection 1, 0) Select one of static, 1/2, 1/3, or 1/4 duty cycle via the combination of DTS1 and DTS0. DTS1 = 0, DTS0 = 0: Selects static DTS1 = 0, DTS0 = 1: Selects 1/2 duty cycle DTS1 = 1, DTS0 = 0: Selects 1/3 duty cycle DTS1 = 1, DTS0 = 1: Selects 1/4 duty cycle	H'FFC0 Bit 7 Bit 6	DST1 = 1 DST0 = 1
	CMX	(Common function selection) Selects whether or not the same waveform is output from multiple common pins that are not used according to the duty cycle to increase the common drive capability. CMX = 0: Same waveform is not output from multiple common pins which are not used according to the duty cycle. CMX = 1: Same waveform is output from multiple common pins which are not used according to the duty cycle.	H'FFC0 Bit 5	0
	SGX	(Extension signal selection) Selects whether the SEG32/CL1, SEG31/CL2, SEG30/DO, and SEG29/M pins are used as segment pins (SEG32 to SEG29) or as segment external expansion pins (CL1, CL2, DO, M). SGX = 0: These pins are used as segment pins (SEG32 to SEG29). CMX = 1: These pins are used as segment external expansion pins (CL1, CL2, DO, M).	H'FFC0 Bit 4	1

Register		Function	Address	Setting
LPCR	SGS3 SGS2 SGS1 SGS0	(Segment driver selection) Select the segment driver to be used. SGX = 0, SGS3 = 0, SGS2S = 0, SGS1 = 0, SGS0 = 0: The SEG32 to SEG1 pins function as ports SGX = 0, SGS3 = 0, SGS2S = 0, SGS1 = 0, SGS0 = 1: The SEG32 to SEG1 pins function as ports SGX = 0, SGS3 = 0, SGS2S = 0, SGS1 = 1, SGS0 = *: The SEG32 to SEG25 pins function as segment drivers and the SEG24 to SEG1 pins function as ports SGX = 0, SGS3 = 0, SGS2S = 1, SGS1 = 0, SGS0 = *: The SEG32 to SEG17 pins function as segment drivers and the SEG16 to SEG1 pins function as ports SGX = 0, SGS3 = 0, SGS2S = 1, SGS1 = 1, SGS0 = *: The SEG32 to SEG9 pins function as segment drivers and the SEG8 to SEG1 pins function as ports SGX = 0, SGS3 = 1, SGS2S = *, SGS1 = *, SGS0 = *: The SEG32 to SEG1 pins function as segment drivers SGX = 1, SGS3 = 0, SGS2S = 0, SGS1 = 0, SGS0 = 0: The SEG32 to SEG29 pins function as external extension pins and the SEG28 to SEG1 pins function as ports SGX = 1, SGS3 = *, SGS2S = *, SGS1 = *, SGS0 = *: Setting prohibited Note: * Don't care	H'FFC0 Bit 3 Bit 2 Bit 1 Bit 0	SGS3 = 0 SGS2 = 0 SGS1 = 0 SGS0 = 0
LCR	PSW	LCD control register (LCD drive power supply on/off control) If the LCD display is not performed in power-down mode, or if an external power supply is used, the LCD drive power supply can be turned off. If the ACT bit is cleared to 0 or in standby mode, the LCD drive power supply is turned off regardless of this bit setting. PSW = 0: Turns off the LCD drive power supply PSW = 1: Turns on the LCD drive power supply	H'FFC1 Bit 6	1
	ACT	(Display function start) Selects whether the LCD controller/driver is used or not. If this bit is cleared to 0, the LCD controller/driver stops operating and the LCD driver power supply is turned off regardless of the PSW bit setting. In this case, the register value is held. ACT = 0: Stops the LCD controller/driver operation ACT = 1: Operates the LCD controller/driver	H'FFC1 Bit 5	1
	DISP	(Display data control) Selects whether the LCD RAM contents are displayed or blank data is displayed regardless of the LCD RAM contents. DISP = 0: Displays blank data DISP = 1: Displays LCD RAM data	H'FFC1 Bit 4	1

Register		Function	Address	Setting
LCR	CKS3 CKS2 CKS1 CKS0	(Frame frequency selection 3 to 0) Select the clock to be used and the frame frequency. CKS3 = 0, CKS2 = *, CKS1 = 0, CKS0 = 0: Select ϕw as a clock. CKS3 = 0, CKS2 = *, CKS1 = 0, CKS0 = 1: Select ϕw/2 as a clock. CKS3 = 0, CKS2 = *, CKS1 = 1, CKS0 = *: Select ϕw/4 as a clock. CKS3 = 1, CKS2 = 0, CKS1 = 0, CKS0 = 0: Select ϕ/2 as a clock. CKS3 = 1, CKS2 = 0, CKS1 = 0, CKS0 = 1: Select ϕ/4as a clock. CKS3 = 1, CKS2 = 0, CKS1 = 1, CKS0 = 0: Select ϕ/8 as a clock. CKS3 = 1, CKS2 = 0, CKS1 = 1, CKS0 = 1: Select ϕ/16 as a clock. CKS3 = 1, CKS2 = 1, CKS1 = 0, CKS0 = 0: Select ϕ/32 as a clock. CKS3 = 1, CKS2 = 1, CKS1 = 0, CKS0 = 1: Select ϕ/64 as a clock. CKS3 = 1, CKS2 = 1, CKS1 = 1, CKS0 = 0: Select ϕ/128 as a clock. CKS3 = 1, CKS2 = 1, CKS1 = 1, CKS0 = 1: Select ϕ/256 as a clock. Note: * Don't care	H'FFC1 Bit 3 Bit 2 Bit 1 Bit 0	CKS3 = 1 CKS2 = 1 CKS1 = 1 CKS0 = 0
LCR2	LCDAB	LCD control register 2 (A/B waveform switching control) Selects the LCD drive waveform as A or B waveform. LCDAB = 0: Drives the LCD as A waveform LCDAB = 1: Drives the LCD as B waveform	H'FFC2 Bit 7	0
	SUPS	(Drive power supply selection and step-up constant-voltage (5 V) power supply control) If Vcc is selected as drive power supply, the step-up constant-voltage (5 V) power supply immediately stops operating; while if 5 V is selected as drive power supply, the step-up constant-voltage (5 V) power supply immediately starts operating. SUPS = 0: Selects Vcc as drive power supply and stops the step-up constant-voltage (5 V) power supply SUPS = 1: Selects 5 V as drive power supply and operates the step-up constant-voltage (5 V) power supply	H'FFC2 Bit 4	0

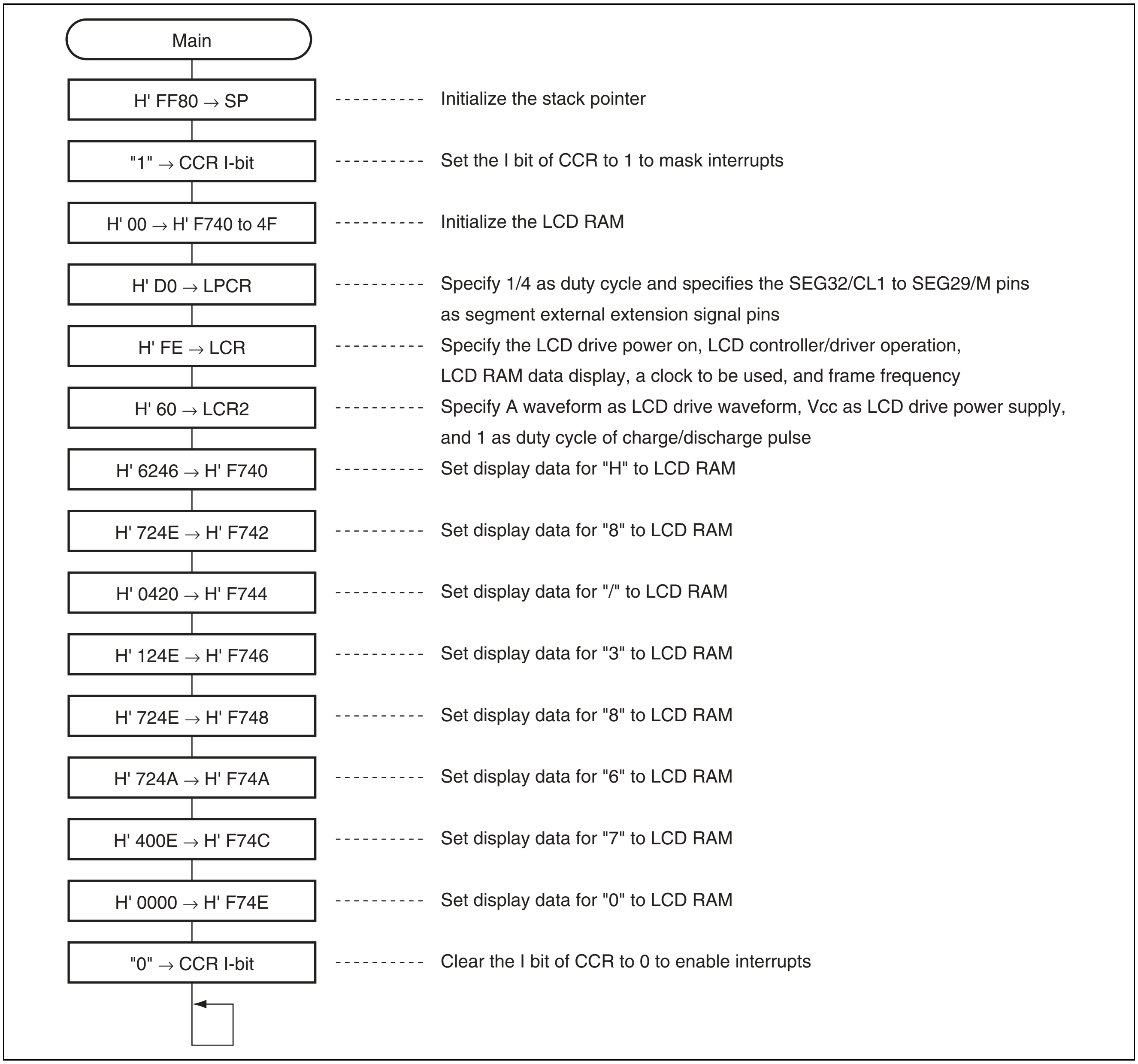
Register		Function	Address	Setting
LCR2	CDS3 CDS2 CDS1 CDS0	(Charge/discharge pulse duty cycle selection 3 to 0) Select the duty cycle while the power supply split resistor is connected to the power supply circuit. CDS3 = 0, CDS2 = 0, CDS1 = 0, CDS0 = 0: Selects 1 as duty cycle. CDS3 = 0, CDS2 = 0, CDS1 = 0, CDS0 = 1: Selects 1/8 as duty cycle. CDS3 = 0, CDS2 = 0, CDS1 = 1, CDS0 = 0: Selects 2/8 as duty cycle. CDS3 = 0, CDS2 = 0, CDS1 = 1, CDS0 = 1: Selects 3/8 as duty cycle. CDS3 = 0, CDS2 = 1, CDS1 = 0, CDS0 = 0: Selects 4/8 as duty cycle. CDS3 = 0, CDS2 = 1, CDS1 = 0, CDS0 = 1: Selects 5/8 as duty cycle. CDS3 = 0, CDS2 = 1, CDS1 = 1, CDS0 = 0: Selects 6/8 as duty cycle. CDS3 = 0, CDS2 = 1, CDS1 = 1, CDS0 = 1: Selects 0 as duty cycle. CDS3 = 1, CDS2 = 0, CDS1 = *, CDS0 = *: Selects 1/16 as duty cycle. CDS3 = 1, CDS2 = 1, CDS1 = *, CDS0 = *: Selects 1/32 as duty cycle. Note: * Don't care	H'FFC2 Bit 3 Bit 2 Bit 1 Bit 0	CDS3 = 0 CDS2 = 0 CDS1 = 0 CDS0 = 0

4.4 Description of RAM

No RAM is used in this sample task.

5. Flowchart

1. Main routine



6. Program Listing

```
;***************************************************************************
;                                                                          *
;  H8/3867 Application Note                                                *
;                                                                          *
;  'Liquid Crystal Display                                                 *
;  -Using Segment External Expansion,                                      *
;  Using HD66100, 1/4 Duty Drive'                                          *
;                                                                          *
;  Function : LCD Controller / Driver                                      *
;                                                                          *
;  External Clock : 6MHz                                                   *
;  Internal Clock : 3MHz                                                   *
;  Sub Clock      : 32.768kHz                                              *
;                                                                          *
;***************************************************************************
;
         .cpu          300L
;
;***************************************************************************
;*  Symbol Defnition                                                       *
;***************************************************************************
;
LPCR      .equ         h'ffc0        ;LCD Port Control Register
LCR       .equ         h'ffc1        ;LCD Control Register
LCR2      .equ         h'ffc2        ;LCD Control Register 2
;
;***************************************************************************
;*  Vector Address                                                         *
;***************************************************************************
;
          .org         h'0000
          .data.w      MAIN          ;No.0 Reset Interrupt(H'0000-H'0001)
;
          .org         h'0008
          .data.w      MAIN          ;No.4 _IRQ0 Interrupt(H'0008-H'0009)
          .data.w      MAIN          ;No.5 _IRQ1 Interrupt(H'000A-H'000B)
          .data.w      MAIN          ;No.6 _IRQ2 Interrupt(H'000C-H'000D)
          .data.w      MAIN          ;No.7 _IRQ3 Interrupt(H'000E-H'000F)
          .data.w      MAIN          ;No.8 _IRQ4 Interrupt(H'0010-H'0011)
          .data.w      MAIN          ;No.9 _WKP0-_WKP7 Interrupt(H'0012-H'0013)
;
          .org         h'0016
          .data.w      MAIN          ;No.11 Timer A Interrupt(H'0016-H'0017)
          .data.w      MAIN          ;No.12 AEC Interrupt(H'0018-H'0019)
          .data.w      MAIN          ;No.13 Timer C Interrupt(H'001A-H'001B)
          .data.w      MAIN          ;No.14 Timer FL Interrupt(H'001C-H'001D)
          .data.w      MAIN          ;No.15 Timer FH Interrupt(H'001E-H'001F)
          .data.w      MAIN          ;No.16 Timer G Interrupt(H'0020-H'0021)
          .data.w      MAIN          ;No.17 SCI31 Interrupt(H'0022-H'0023)
          .data.w      MAIN          ;No.18 SCI32 Interrupt(H'0024-H'0025)
          .data.w      MAIN          ;No.19 A/D Converter Interrupt(H'0026-H'0028)
          .data.w      MAIN          ;No.20 Direct Transfer Interrupt(H'0028-H'0029)
;
```

```
;*****************************************************************************************
;*  MAIN : Main Routine                                                                  *
;*****************************************************************************************
          .org         h'1000
;
MAIN:     equ          $
          mov.w        #h'ff80,sp    ;Initialize Stack Pointer
          orc          #h'80,ccr     ;Interrupt Disable
;
          sub.b        r0l,r0l       ;Initialize LCD RAM

          mov.w        #h'f740,r1
          mov.w        #h'f750,r2
INIT:     mov.b        r0l,@r1
          adds         #1,r1
          cmp.w        r2,r1
          bne          INIT
;
          mov.b        #h'd0,r0l     ;Initialize LCD Port Control

          mov.b        r0l,@LPCR
          mov.b        #h'fe,r0l     ;Initialize LCD Control

          mov.b        r0l,@LCR
          mov.b        #h'60,r0l     ;Initialize LCD Control 2
          mov.b        r0l,@LCR2
;
          mov.w        #h'f740,r1    ;Set LCD RAM Start Address
          mov.w        #h'f750,r2    ;Set LCD RAM End Address
          mov.w        #h'1500,r3    ;Set LCD Data Address
DISP:     mov.w        @r3,r0        ;Load LCD Data
          mov.w        r0,@r1        ;Store LCD Data to LCD RAM
          adds         #2,r3         ;Increment LCD Data Address
          adds         #2,r1         ;Increment LCD RAM Address
          cmp.w        r2,r1         ;LCD RAM Address = LCD RAM End Address ?
          bne          DISP          ;No.
;
EXIT:     bra          EXIT;         ;Yes.
;
;*****************************************************************************************
;*  LCD Data Table                                                                       *
;*****************************************************************************************
          .org         h'1500
;
          .data.w      h'6246        ;"H"
          .data.w      h'724e        ;"8"
          .data.w      h'0420        ;"/"
          .data.w      h'124e        ;"3"
          .data.w      h'724e        ;"8"
          .data.w      h'724a        ;"6"
          .data.w      h'400e        ;"7"
          .data.w      h'0000        ;" "
;
          .end
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued