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H8SX Family

Using the DMAC with Address Updating by Offset Addition

Introduction

Image data is rotated left by 90° through data transfer by the DMAC using a mode where the transfer address is updated by adding a specified offset.

Target Device

H8SX/1653

Contents

1. Specifications

- Image data is rotated left by 90° as shown in figure 1 through data transfer by the DMAC using a mode where the transfer address is updated by adding a specified offset.
- The source image data is stored in on-chip ROM, and the rotated data is stored in on-chip RAM (array ramarea).
- The source image data is a 256-gray-scale image (eight bits per dot) having a height of 32 dots and a width of 48 dots.
- Figure 2 shows the source and destination memory allocation.
- Table 1 shows the necessary DMA transfer settings.

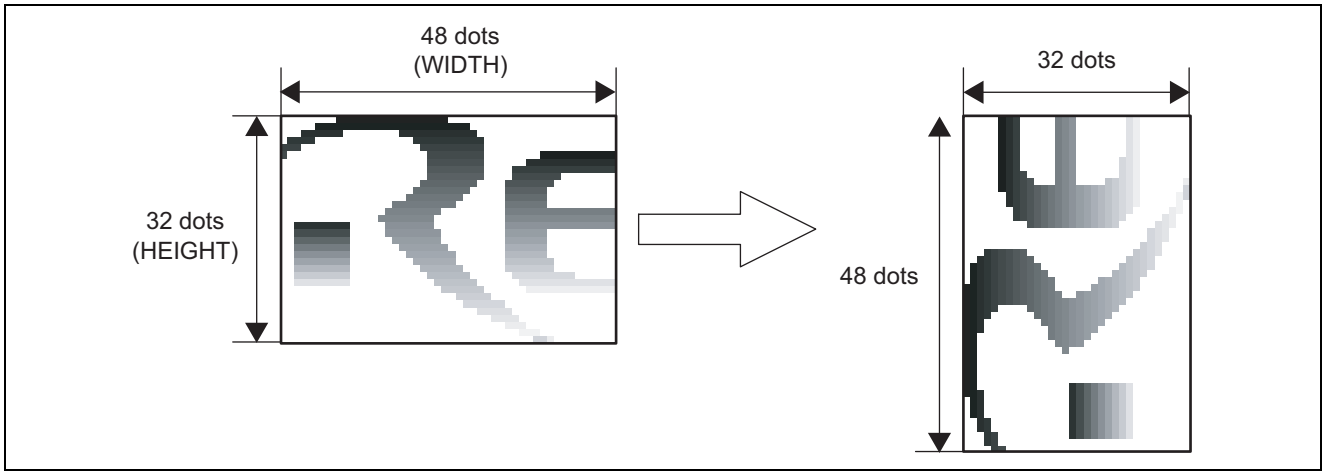


Figure 1 Rotating Image Data Left by 90°

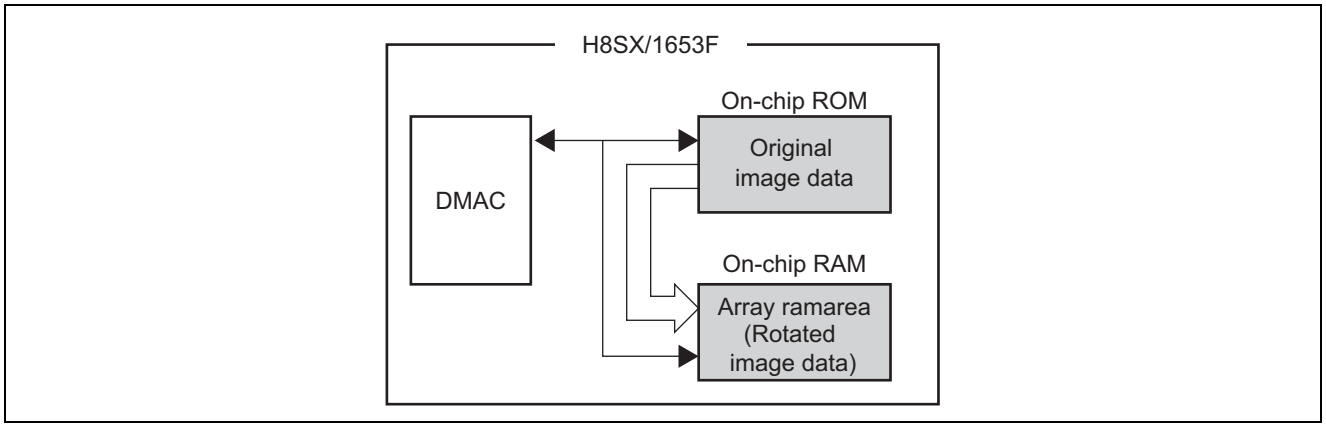


Figure 2 Memory Allocation for This Sample Task

Table 1 DMA Transfer Settings

Item	Contents
DMA transfer request	Auto request mode
Bus mode	Cycle stealing mode
Transfer mode	Repeat transfer mode
Address mode	Dual address mode
Unit of transfer	Byte

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.01 (from Renesas Technology Corp.)
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'003000	PIC	Source image data
H'FF2000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 3 shows a block diagram of the DMAC. The block diagram of the DMAC is described below.

- DMA source address register_0 (DSAR_0)
  A 32-bit readable/writable register that specifies the source address of DMA transfer. This register has an address updating function so the value of this register is changed to the next source address after each transfer processing.
- DMA destination address register_0 (DDAR_0)
  A 32-bit readable/writable register that specifies the destination address of DMA transfer. This register has an address updating function so the value of this register is changed to the next destination address after each transfer processing.
- DMA offset register_0 (DOFR_0)
  A 32-bit readable/writable register that specifies the offset used in updating the source or destination address when offset addition is specified.
- DMA transfer count register_0 (DTCR_0)
  A 32-bit readable/writable register that specifies the size of the data to be transferred (total transfer size). The value of this register will be decremented by a value corresponding to the access size of the transferred data after each data transfer. In this sample task, the size of the data for transfer is set as 1536 bytes (H'00000600) and the unit of data access is a byte. Accordingly, the value of this register is decremented by one during DMA transfer, indicating the size of the remaining data.
- DMA block size register_0 (DBSR_0)
  DBSR is enabled in repeat transfer mode or block transfer mode and specifies the repeat size or block size. It is disabled in normal transfer mode. In this sample task, the DMAC operates in repeat transfer mode with the repeat size specified as 32 bytes.
- DMA mode control register_0 (DMDR_0)
  Controls operation of the DMAC.
- DMA address control register_0 (DACR_0)
  Sets the operating mode and transfer mode.

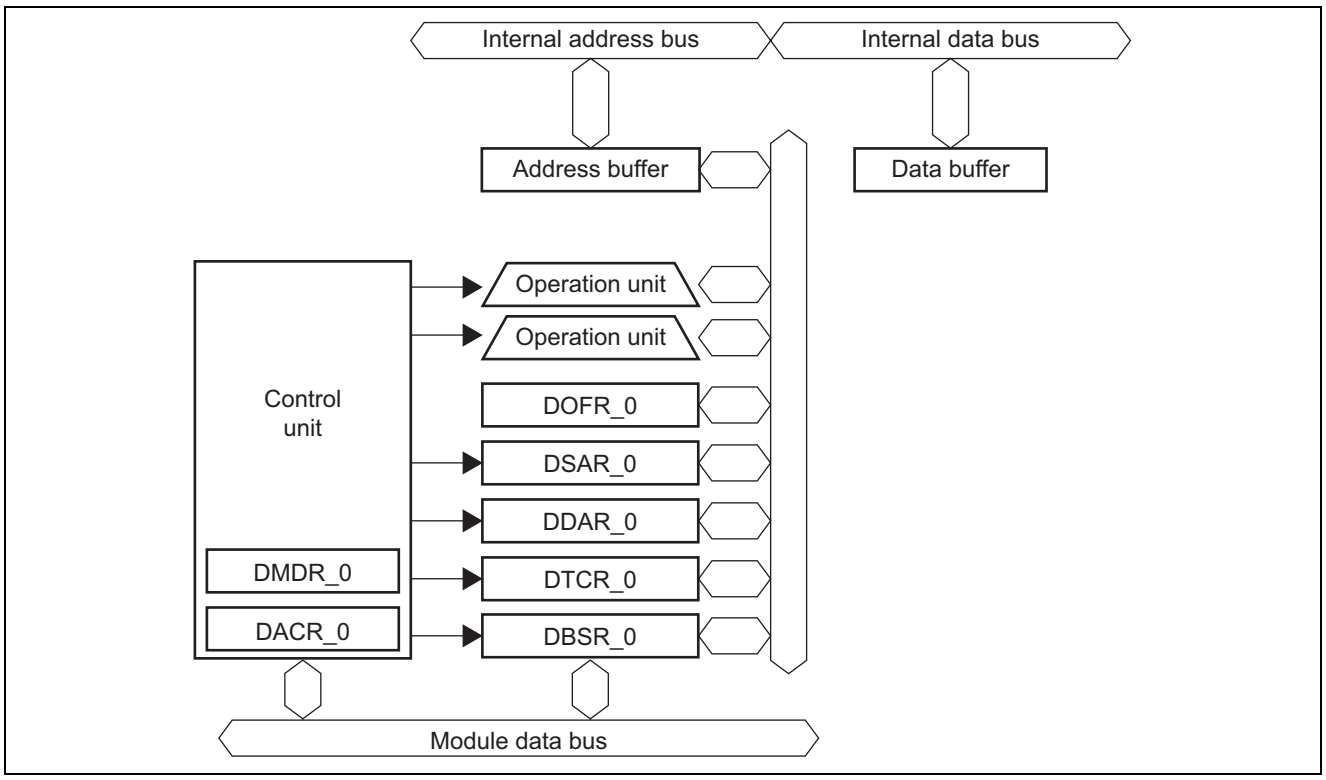


Figure 3 Block Diagram of DMAC

4. Description of Operation

Figure 4 shows an example of image data rotation to the left by 90° using the DMAC in a mode where address updating is by offset addition. Table 4 shows the DMAC settings for transfer with address updating by offset addition. The following gives an overview of the operation shown in figure 4.

- First cycle
  (1) Initiate the transfer.
  (2) The DMAC transfers the data at the source address to which an offset is added.
  (3) The transferred data is stored to the location at the start address of the destination area + H'5E0 and to the subsequent addresses in the order of transfer.
  (4) After up to data H'01F has been transferred, that is, the data transfer has been completed for the repeat size, the DMAC initializes the source address to the transfer start address (the address where transfer data H'001 is stored). At the same time, the DMAC generates a repeat size end interrupt.
  (5) This interrupt request suspends the data transfer. By the CPU, change the DSAR value to the address where data H'020 is stored (in byte-size transfer, change this to the address of data H'001 + 1).
- Second and subsequent cycles
  (6) Set the DTE bit in DMDR to 1: Transfer is resumed from the suspended state.

After that, repeat steps (2) to (6), and the source image data is transferred to the destination area in the arrangement such that it is rotated left by 90°.

Table 4 DMAC Settings for Transfer with Address Updating by Offset Addition

Item	Setting
Repeat area	Source address side
Source address update mode	Offset addition
Destination address update mode	Incrementation by 1, 2, or 4
Offset value	48 bytes (WIDTH)
Repeat size	32 bytes (HEIGHT)
RPTIE bit set to 1 in DACR	A repeat size end interrupt request is generated when data of the repeat size has been transferred

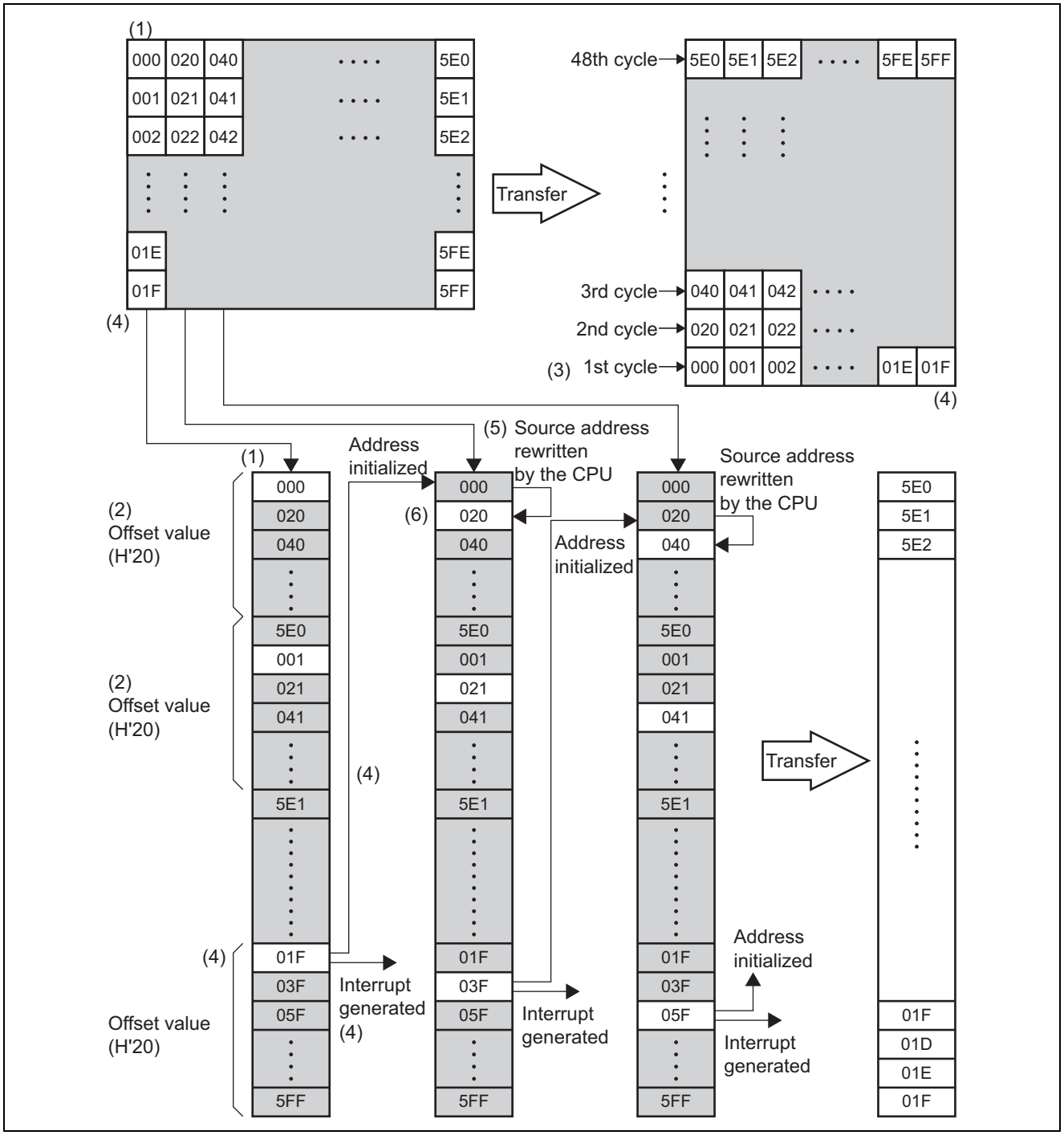


Figure 4 Example of 90° Left Rotation

5. Description of Software

5.1 List of Functions

Table 5 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR, configures the clocks, cancels the module stop mode, and calls the main function.
main	Main routine Makes the settings for DMAC repeat transfer mode and offset addition.
dmeend0_int	DMAC0 transfer escape end interrupt handling routine Changes the source and destination addresses.

5.2 RAM Usage

Table 6 RAM Usage

Type	Variable Name	Description	Used In
unsigned char	ramarea[128]	Destination RAM area	main

5.3 Constants

Table 7 List of Constants

Constant Name	Description	Used In
HEIGHT	Height of the original image for transfer Setting: 32 dots	main
WIDTH	Width of the original image for transfer Setting: 48 dots	main

5.4 Description of Functions

5.4.1 init Function

(1) Functional overview

Initialization routine which cancels the module stop mode, sets up the clocks, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock, which is
8	ICK0	0	R/W	supplied to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit in these registers to 1 places the corresponding module in module stop mode, while clearing the bit to 0 cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

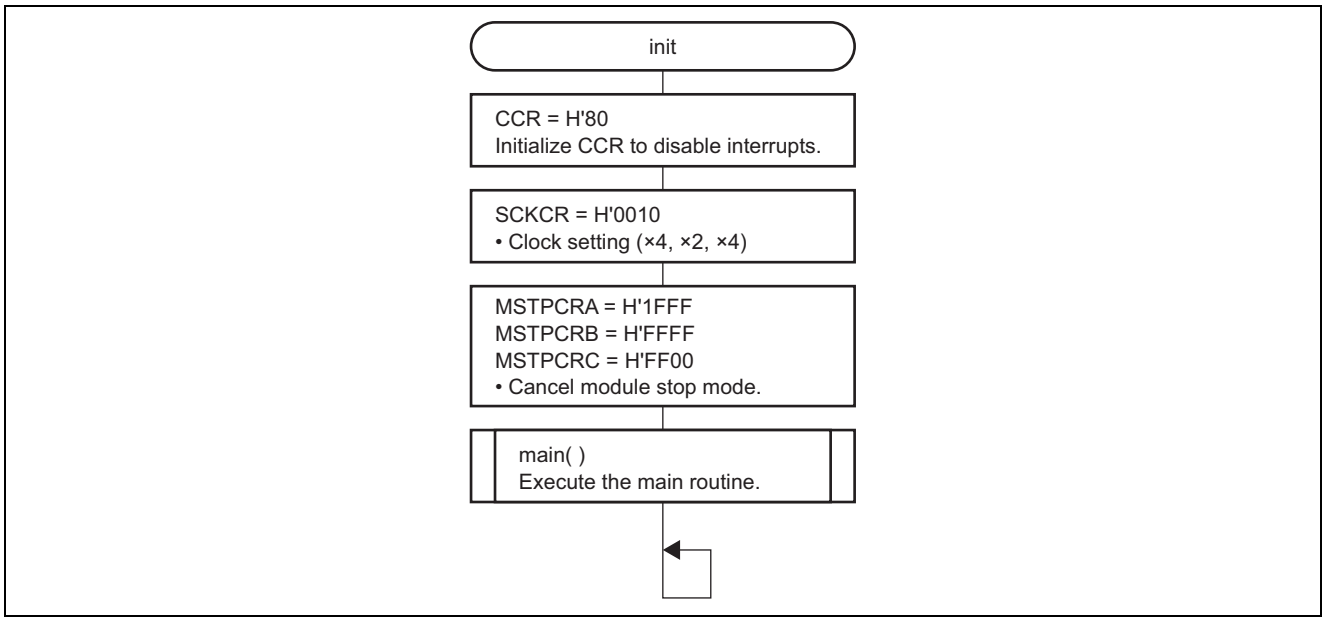
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

(5) Flowchart


init
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0010
• Clock setting (×4, ×2, ×4)
MSTPCRA = H'1FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Cancel module stop mode.
main( )
Execute the main routine.

5.4.2 main Function

(1) Functional overview

Makes settings for transfer by the DMAC and starts transfer.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DMA source address register_0 (DSAR_0) Address: H'FFFC00
  Function: Specifies the source address for data transfer.
  Setting: H'003000
- DMA destination address register_0 (DDAR_0) Address: H'FFFC04
  Function: Specifies the destination address for data transfer.
  Setting: &ramarea[(WIDTH – 1) * HEIGHT]
- DMA offset register_0 (DOFR_0) Address: H'FFFC08
  Function: Specifies the offset value.
  Setting: WIDTH
- DMA transfer count register_0 (DTCR_0) Address: H'FFFC0C
  Function: Specifies the size of the data to be transferred.
  Setting: HEIGHT * WIDTH
- DMA block size register_0 (DBSR_0) Address: H'FFFC10
  Function: Specifies the repeat size in repeat transfer mode. When DBSR_0 = H'00200020, the repeat size is 32 bytes.
  Setting: HEIGHT * H'10000 + HEIGHT

- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

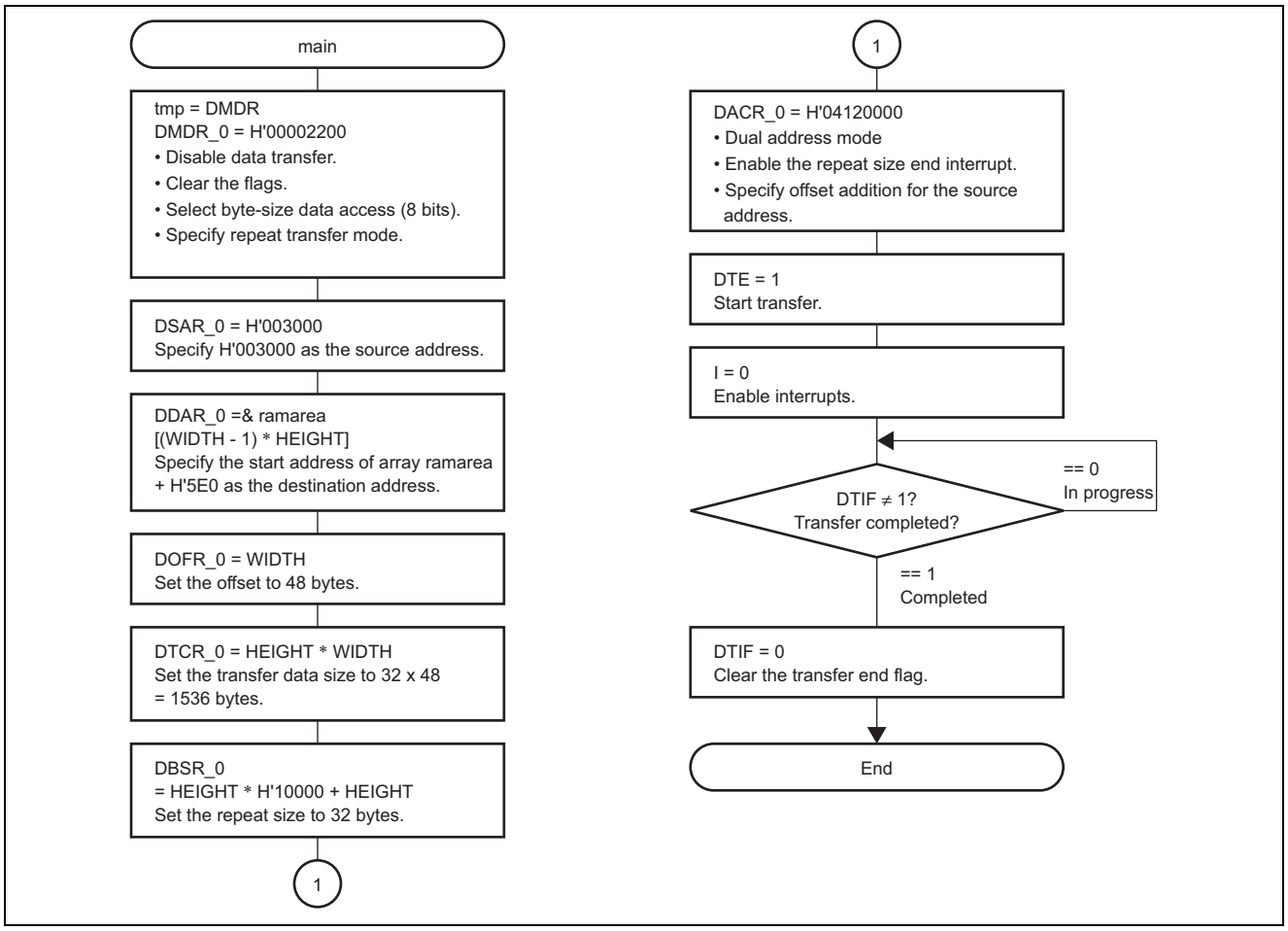
Bit	Bit Name	Setting	Function	
31	DTE	0/1	R/W	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled
26	NRD	0	R/W	Next Request Delay 0: Starts accepting the next transfer request after completion of the current transfer 1: Starts accepting the next transfer request one cycle after completion of the current transfer
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: Transfer end interrupt by the transfer counter has not been requested 1: Transfer end interrupt by the transfer counter has been requested
15	DTSZ1	0	R/W	Data Access Size 1, 0
14	DTSZ0	0	R/W	00: Byte size (8 bits)
13	MDS1	1	R/W	Transfer Mode Select 1, 0
12	MDS0	0	R/W	00: Repeat transfer mode
9	ESIE	1	R/W	Transfer Escape Interrupt Enable 0: Disables transfer escape end interrupts 1: Enables transfer escape end interrupts
7	DTF1	0	R/W	Data Transfer Factor 1, 0
6	DTF0	0	R/W	00: DMAC is activated by an auto request (cycle stealing)

Note: * Only 0 can be written to clear the flag after reading the flag as 1.

- DMA address control register_0 (DACR_0) Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Function
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
26	RPTIE	1	R/W	Repeat Size End Interrupt Enable 0: Disables repeat size end interrupts 1: Enables repeat size end interrupts
25	ARS1	0	R/W	Area Select 1, 0
24	ARS0	0	R/W	00: Select the source address side as the repeat area in repeat transfer mode
21	SAT1	0	R/W	Source Address Update Mode 1, 0
20	SAT0	1	R/W	01: Source address is updated by adding the offset
17	DAT1	1	R/W	Destination Address Update Mode 1, 0
16	DAT0	0	R/W	10: Destination address is incremented (When data access is in byte units, incremented by 1)

(5) Flowchart


main
tmp = DMDR
DMDR_0 = H'00002200
• Disable data transfer.
• Clear the flags.
• Select byte-size data access (8 bits).
• Specify repeat transfer mode.
DSAR_0 = H'003000
Specify H'003000 as the source address.
DDAR_0 =& ramarea
[(WIDTH - 1) * HEIGHT]
Specify the start address of array ramarea
+ H'5E0 as the destination address.
DOFR_0 = WIDTH
Set the offset to 48 bytes.
DTCR_0 = HEIGHT * WIDTH
Set the transfer data size to 32 x 48
= 1536 bytes.
DBSR_0
= HEIGHT * H'10000 + HEIGHT
Set the repeat size to 32 bytes.
1
1
DACR_0 = H'04120000
• Dual address mode
• Enable the repeat size end interrupt.
• Specify offset addition for the source
address.
DTE = 1
Start transfer.
I = 0
Enable interrupts.
DTIF ≠ 1?
Transfer completed?
== 0
In progress
== 1
Completed
DTIF = 0
Clear the transfer end flag.
End

5.4.3 dmeend0_int Function

(1) Functional overview

DMAC0 transfer escape end interrupt handling routine

(2) Argument

None

(3) Return value

None

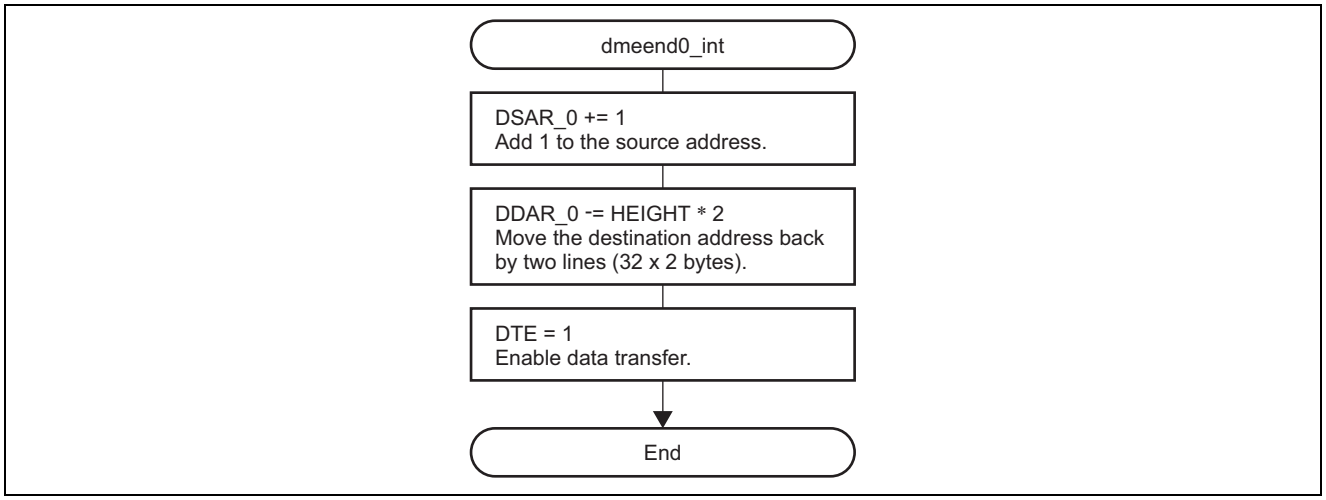
(4) Description of internal registers

The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DMA source address register_0 (DSAR_0) Address: H'FFFC00
  Function: Specifies the source address for data transfer.
  Setting: DSAR_0 + 1
- DMA destination address register_0 (DDAR_0) Address: H'FFFC04
  Function: Specifies the destination address for data transfer.
  Setting: DDAR_0 – HEIGHT * 2
- DMA mode control register_0 (DMDR_0) Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Function
31	DTE	1	R/W	Data Transfer Enable 0: Data transfer is disabled 1: Data transfer is enabled

(5) Flowchart



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