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April 1st, 2010
Renesas Electronics Corporation

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H8/300L SLP Series

Using the Clock Output Function for Clock-Signal Output

Introduction

A clock is output from the TMOW output pin using the timer A clock output function.

Target Device

H8/3867

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1. Specifications

1. A clock is output from the TMOW output pin using the timer A clock output function.
2. A clock to be output is selectable from eight clocks including four clocks which divide the system clock and four clocks which divide 32.768 kHz.
3. In this sample task, a 2.048-kHz clock which divides the system clock by 16 is output from the TMOW pin.

2. Description of Functions

1. In this sample task, clock output is performed from the TMOW output pin using the timer A clock output function. Figure 2.1 shows a block diagram of the timer A clock output function. The block diagram of the timer A clock output function is described below.
   - The system clock (ϕ) is a 5-MHz clock which divides the 10-MHz OSC clock by 2, and is a reference clock for activating the CPU and the peripheral functions.
   - ϕw is an output clock (32.768 kHz) of the sub clock oscillator.
   - The prescaler S (PSS) is a 13-bit counter to which ϕ is input, and is incremented for each cycle.
   - The prescaler W (PSW) is a 5-bit counter to which a clock (ϕw/4) that divides 32.768 kHz by 4 is input.
   - The timer mode register A (TMA) is an 8-bit readable/writable register, which selects a clock to be output from the TMOW pin. In this sample task, a 2.048-Hz clock which divides the sub system clock by 16 is selected as the clock to be output from the TMOW output pin by setting the TMA to H'B0.
   - The clock output pin (TMOW) is an output pin of the timer output clock, which can select the clock to be output from the clocks that divide 32.768 kHz by 32, 16, 8, or 4, and the clocks that divide the system clock by 32, 16, 8, or 4.
   - Table 2.1 shows the types of clocks to be output from the TMOW pin and the settings.

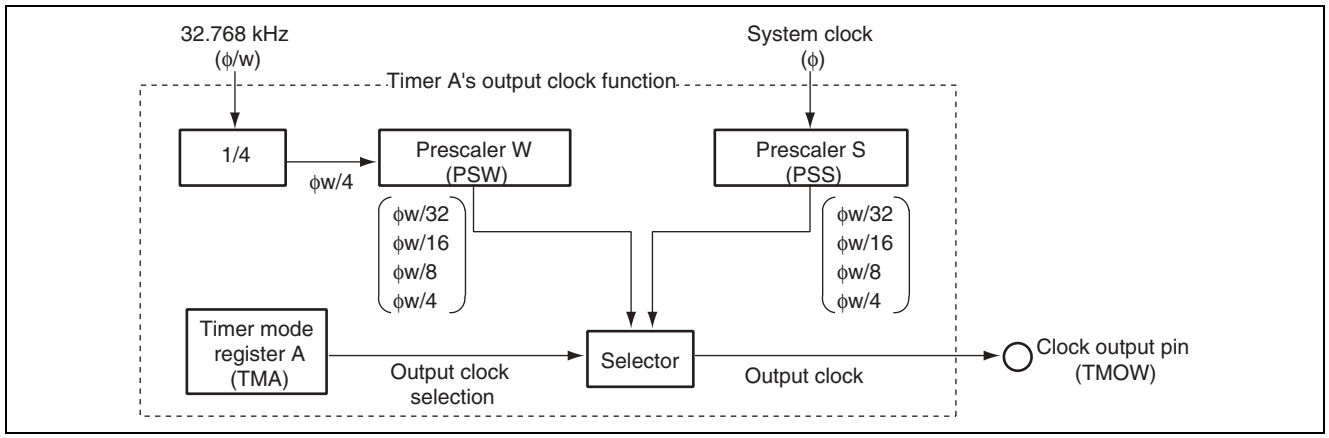


Figure 2.1 Block Diagram of Timer A Clock Output Function

Table 2.1 Clock to be Output from TMOW Pin and Setting

TMA					
TMA 7	**TMA 6**	**TMA 5**	**Clock to be output**	**Output clock frequency**	**TMA setting**
0	0	0	ϕ/32	5 MHz / 32 = 156.25 kHz	H'10
0	0	1	ϕ/16	5 MHz / 16 = 312.5 kHz	H'30
0	1	0	ϕ/8	5 MHz / 8 = 625 kHz	H'50
0	1	1	ϕ/4	5 MHz / 4 = 1.25 kHz	H'70
1	0	0	ϕ_W/32	32.768 kHz / 32 = 1.024 kHz	H'90
1	0	1	ϕ_W/16	32.768 kHz / 16 = 2.048 kHz	H'B0
1	1	0	ϕ_W/8	32.768 kHz / 8 = 4.096 kHz	H'D0
1	1	1	ϕ_W/4	32.768 kHz / 4 = 8.192 kHz	H'F0

2. Table 2.2 shows function allocations. Clock output is performed using the timer A clock output function through function allocations as shown in table 2.2.

Table 2.2 Function Allocation

Function	Function Allocation
PSS	13-bit counter to which the system clock is input.
PSW	5-bit counter to which a clock that divides 32.768 kHz by 4 is input.
TMA	Selects output clock.
TMOW	Clock output pin
PMR1	Sets TMOW output pin functions.

3. Principles of Operation

1. Figure 3.1 shows the principle of operation. As shown in figure 3.1, clock output is performed using the timer A clock output functions by hardware and software processing.

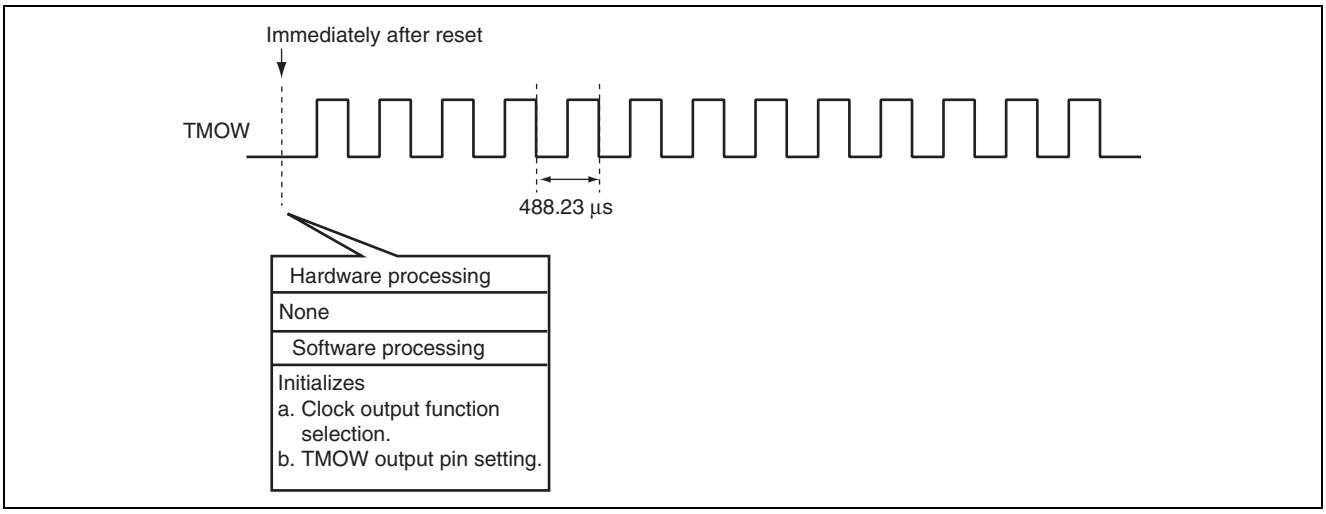


Figure 3.1 Principle of Operation of Clock Output by Timer A Clock Output Function

4. Description of Software

4.1 Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module	Label	Function
Main routine	MAIN	Initializes stack pointer, sets clock output function, sets the TMOW output pin, and enables interrupts

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 4.2.

Table 4.2 Description of Internal Registers

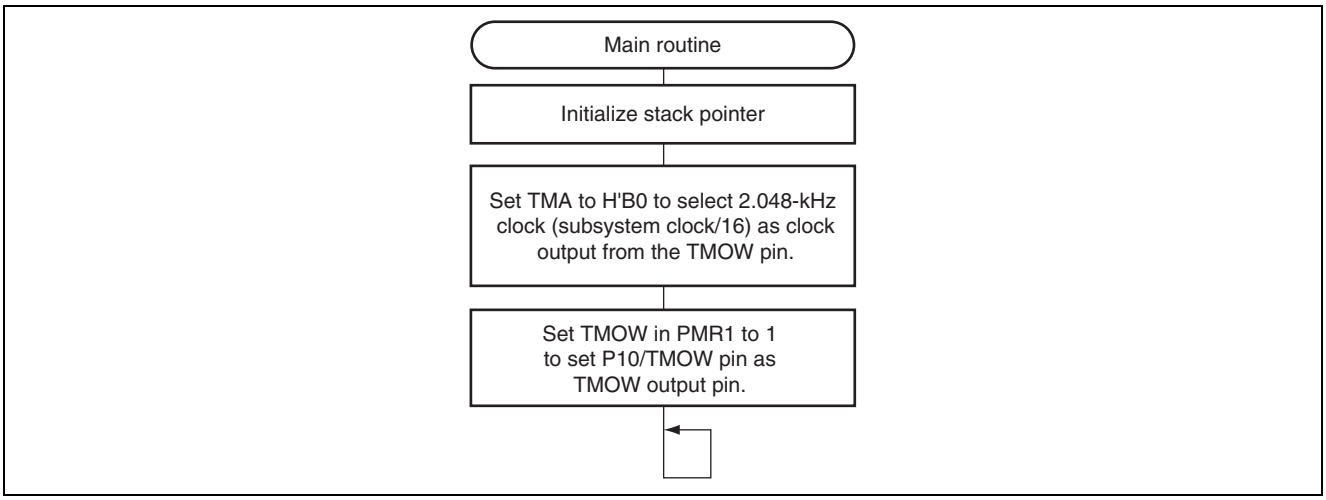
Register		Function	Address	Setting
TMA		Timer mode register A: when TMA = H'B0, selects the 2.048 kHz clock which divides the sub system clock by 16 as a clock to be output from the TMOW output pin	H'FFB0	H'B0
PMR1	TMOW	Port mode register 1 ($P1_0$/TMOW pin function switch): when TMOW = 1, sets the $P1_0$/TMOW pin as the TMOW output pin function	H'FFFC Bit 0	1

4.4 Description of RAM

This sample task does not use RAM.

5. Flowchart

1. Main routine



6. Program Listing

```
;*************************************************************************************
;*                                                                                   *
;*     H8/300L Series -H8/3644,H8/3657-                                              *
;*     Application Note                                                              *
;*                                                                                   *
;*     'Clock Output by Clock Output Function'                                       *
;*                                                                                   *
;*     Function       : Timer A Clock Output                                         *
;*                                                                                   *
;*     External Clock : 10MHz                                                        *
;*     Internal Clock :  5MHz                                                        *
;*     Sub Clock      : 32.768kHz                                                    *
;*                                                                                   *
;*************************************************************************************
;
          .cpu         300L
;
;*************************************************************************************
;*  Symbol Defnition                                                                 *
;*************************************************************************************
;
TMA       .equ         H'FFB0        ;Timer Mode Register A
PDR7      .equ         H'FFDA        ;Port Data Register 7
PMR1      .equ         H'FFFC        ;Port Mode Register 1
TMOW      .bequ        0,PMR1        ;P10/TMOW Terminal Function Change
;
;*************************************************************************************
;*  Ram Allocation                                                                   *
;*************************************************************************************
;
STACK     .equ         H'FF80        ;Stack Pointer
;
;*************************************************************************************
;*  Vector Address                                                                   *
;*************************************************************************************
;
          .org         H'0000
          .data.w      MAIN          ;Reset Interrupt
;
          .org         H'0008
          .data.w      MAIN          ;IRQ0 Interrupt
          .data.w      MAIN          ;IRQ1 Interrupt
          .data.w      MAIN          ;IRQ2 Interrupt
          .data.w      MAIN          ;IRQ3 Interrupt
          .data.w      MAIN          ;INT0 - INT7 Interrupt
;
          .org         H'0014
          .data.w      MAIN          ;Timer A Interrupt
          .data.w      MAIN          ;Timer B1 Interrupt
;
          .org         H'0020
          .data.w      MAIN          ;Timer X Interrupt
          .data.w      MAIN          ;Timer V Interrupt
;
```

```
          .org         H'0026
          .data.w      MAIN          ;Sci1 Interrupt
;
          .org         H'002A
          .data.w      MAIN          ;Sci3 Interrupt
          .data.w      MAIN          ;A/D Converter Interrupt
          .data.w      MAIN          ;Sleep Interrupt
;
;*************************************************************************************
;*  Main Program                                                                     *
;*************************************************************************************
;
          .org         H'1000
;
MAIN      .equ         $
          MOV.W        #STACK,SP     ;Initialize Stack Pointer
;
          MOV.B        #H'B0,R0L
          MOV.B        R0L,@TMA      ;Initialize Output Clock Function
;
          BSET         TMOW          ;Initialize TMOW Output Terminal Function
;
MAIN9     .equ         $
          BRA          MAIN9
;
          .end
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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