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SH7280 Group

Transmission and Reception of Serial Data by the SCIF in Asynchronous Mode

Introduction

This application note describes transmission and reception of serial data by using the asynchronous transfer function of the serial communications interface with FIFO (SCIF). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

This sample application employs the asynchronous serial transfer function of the serial communications interface with FIFO (SCIF) to perform data transmission and reception. Figure 1 shows an example of connection for transmission and reception by the SCIF in asynchronous mode.

- SCIF3 is used.
- The communications format has a fixed 8-bit data length, 1 stop bit, and no parity bit.
- Interrupts for transmission and reception are used to conduct bidirectional communications via SCIF3. That is, the data-transfer controller (DTC) is activated by the transmit-FIFO-data-empty interrupt on the transmitting side and the receive-FIFO-data-full interrupt on the receiving side.
- Once 32 bytes of data have been transmitted and received, each operation is halted.

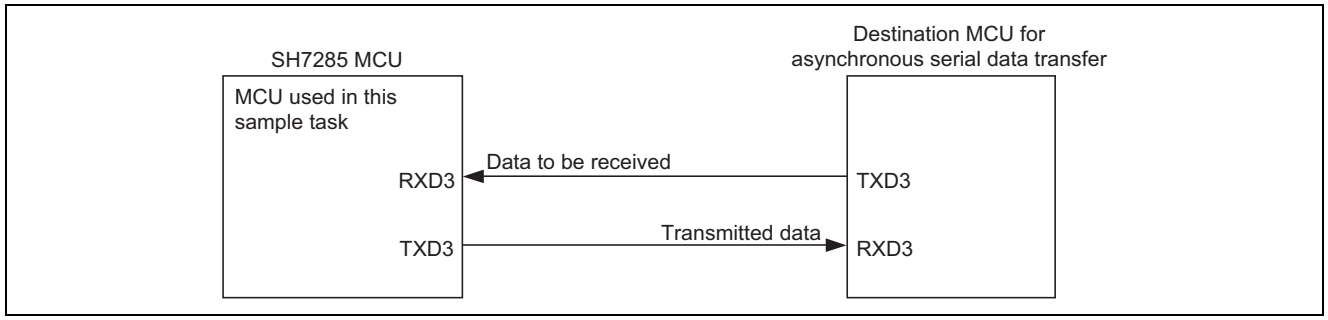

Figure 1 Connection Example for Transmission and Reception by the SCIF in Asynchronous Mode

1.2 Module Used

Serial communications interface with FIFO (SCIF3)

1.3 Applicable Conditions

MCU	SH7285	
Operating frequency	Internal clock:	100 MHz
	Bus clock:	50 MHz
	Peripheral clock:	50 MHz
C compiler	SuperH RISC engine Family C/C++ Compiler Package Ver.9.11	
	(from Renesas Technology Corp.)	

2. Description of the Sample Application

This sample application employs interrupt source of the serial communications interface with FIFO (SCIF), a transmit-FIFO-data-empty interrupt (TXI) and a receive-FIFO-data-full interrupt (RXI) to transmit and receive serial data in asynchronous mode.

2.1 Summary of MCU Module Used

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized in character units. The transmitting and receiving sections of the SCIF are independent, so full-duplex communications is possible while sharing the same clock. Both the transmitter and receiver have a 16-stage FIFO buffered structure so that data can be read or written during transmission and reception, which enables high-speed continuous data transfer.

In asynchronous serial communications, the communication line is normally held in the mark (high) state. The SCIF monitors the line and starts serial communications when the line goes to the space (low) state, indicating a start bit.

One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in this order.

For details on the SCIF, please refer to the section on serial communications interface with FIFO in the *SH7280 Group Hardware Manual (REJ09B0393).*

Table 1 gives an overview of serial communications in asynchronous mode. Figure 2 shows a block diagram of the SCIF.

Table 1 Overview of Serial Data Communications in Asynchronous Mode

Item	Description
Number of interfaces	1 (SCIF3)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on the SCK3 pin
Data format	Transfer data length: Selectable from 7 or 8 bits Order: LSB first and MSB first are selectable
Baud rate	For internal clock: from 110 bps (Pϕ = 50 MHz) For external clock: up to 781,250 bps (Pϕ = 50 MHz, external input clock of 12.5000 MHz)
Error detection	Framing, parity and overrun errors Breaks can also be detected.
Interrupt requests	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Break interrupt (BRI) Receive-error interrupt (ERI)
Clock sources	Internal and external clocks are selectable • Internal clock When the internal clock has been selected, the SCIF operates using the clock from the baud-rate generator and a clock signal at 16 times the frequency of the bit rate can be output. • External clock When the external clock has been selected, input of a clock signal at 16 times the frequency of the bit rate is required, not using the on-chip baud rate generator.
Loop-back test function	• Internal connection of the transmit output pin (TXD) and receive input pin (RXD) enables loop-back testing.

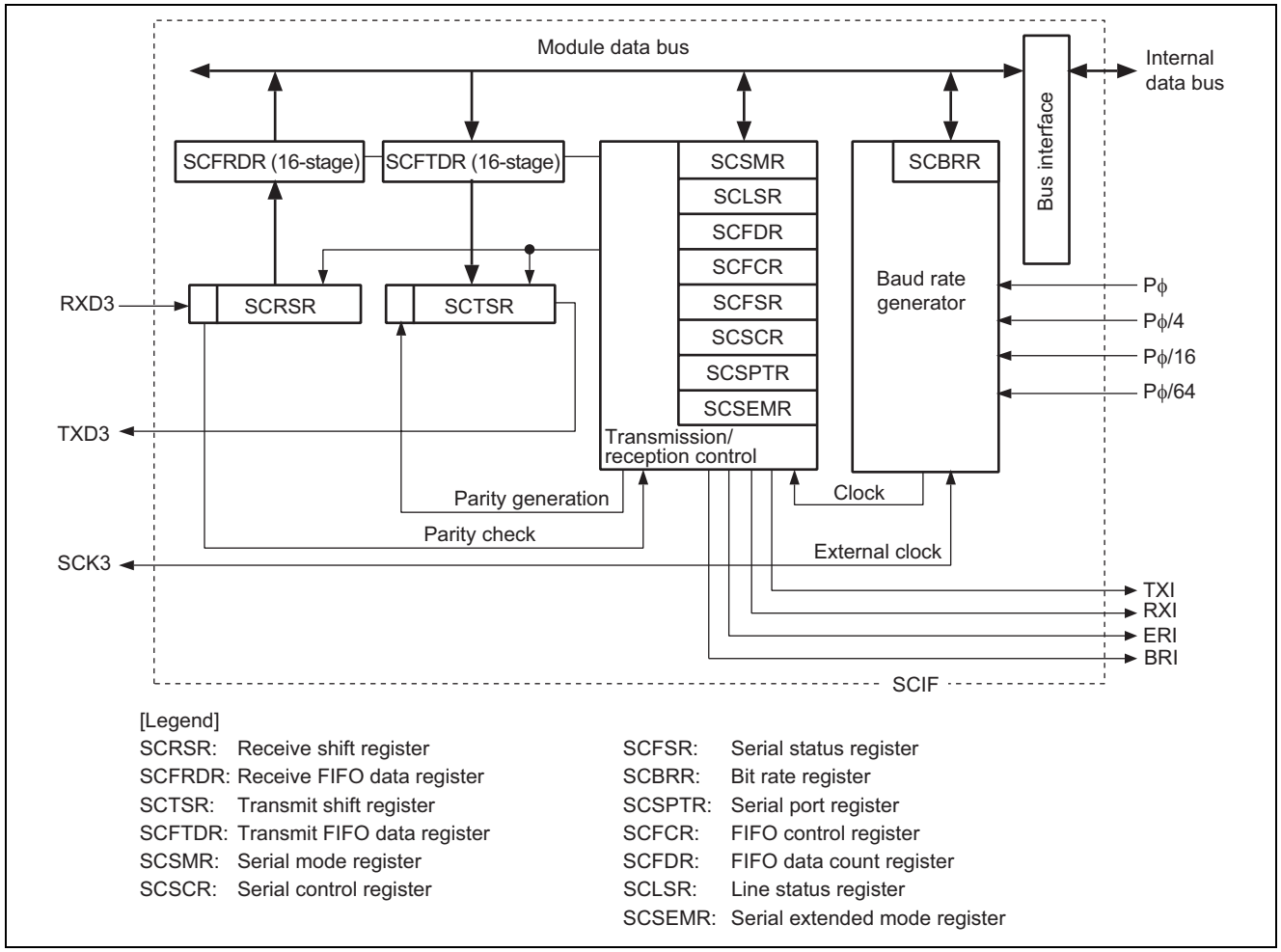

Figure 2 Block Diagram of the SCIF

2.2 Description of the Sample Program

Table 2 gives the settings for SCIF communications function of this sample program, and figure 3 shows the operations in data transmission and reception.

Table 2 Settings for Communications Function of the Sample Program

Item	Description
Module	SCIF3
Communications mode	Asynchronous mode
Interrupts	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Break interrupt (BRI)
Transfer rate	38,400 bps
Number of data to be transmitted and received	32 bytes
Data length	8-bit data
Stop bit	1 stop bit
Parity	None
Bit order	LSB-first
FIFO data trigger number	Receive FIFO data trigger: 8 Transmit FIFO data trigger: 8

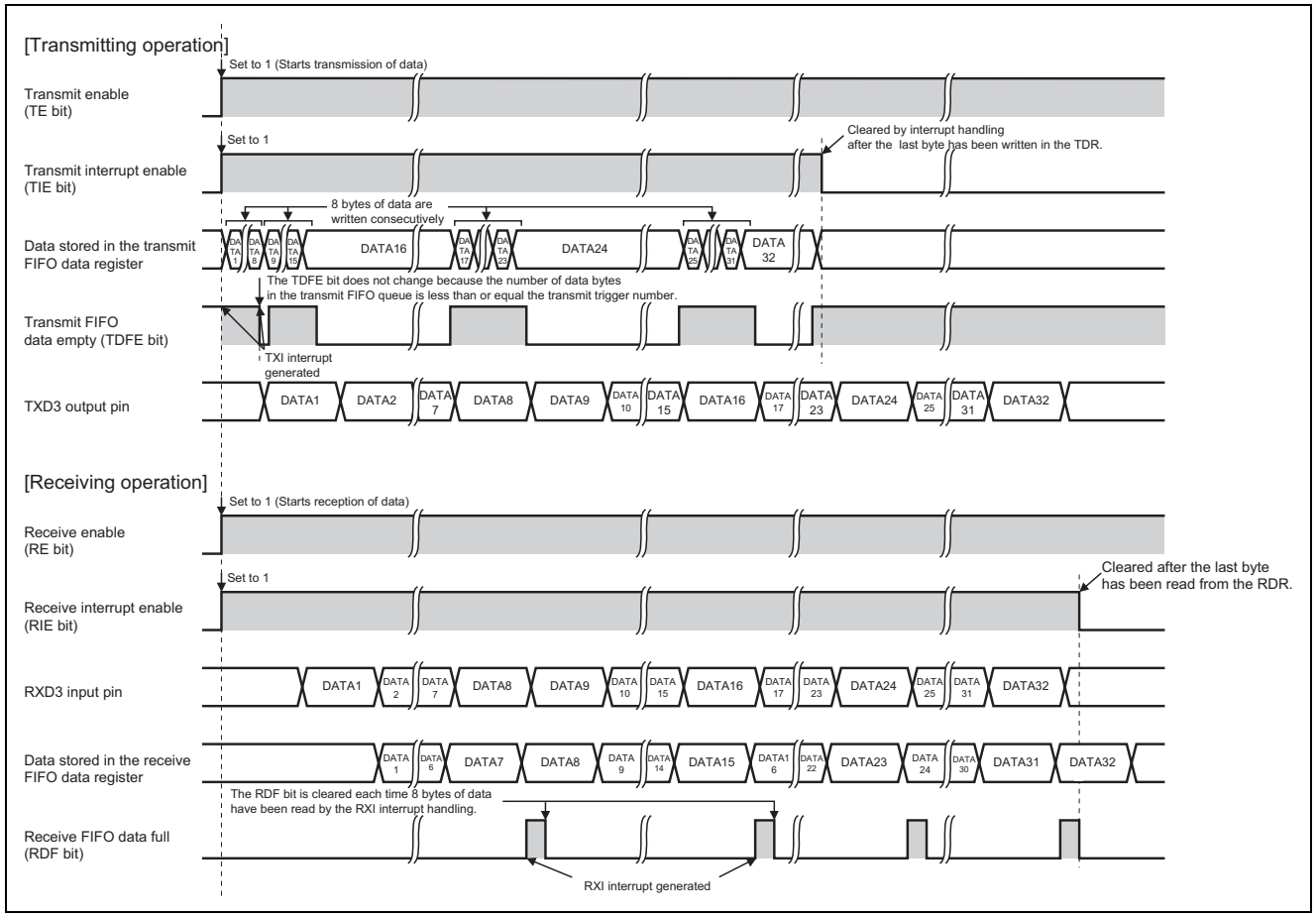

Figure 3 Operations for Data Transmission and Reception

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCIF3 for asynchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for initialization of data transmission and reception in asynchronous mode, and figure 7 shows the flow for setting up the pin function controller. Furthermore, figure 8 shows the flow for handling transmit interrupts in asynchronous mode, figure 9 shows the flow for handling receive interrupts in asynchronous mode, and figure 10 shows the flow for handling receive error interrupts. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual (REJ09B0393).*

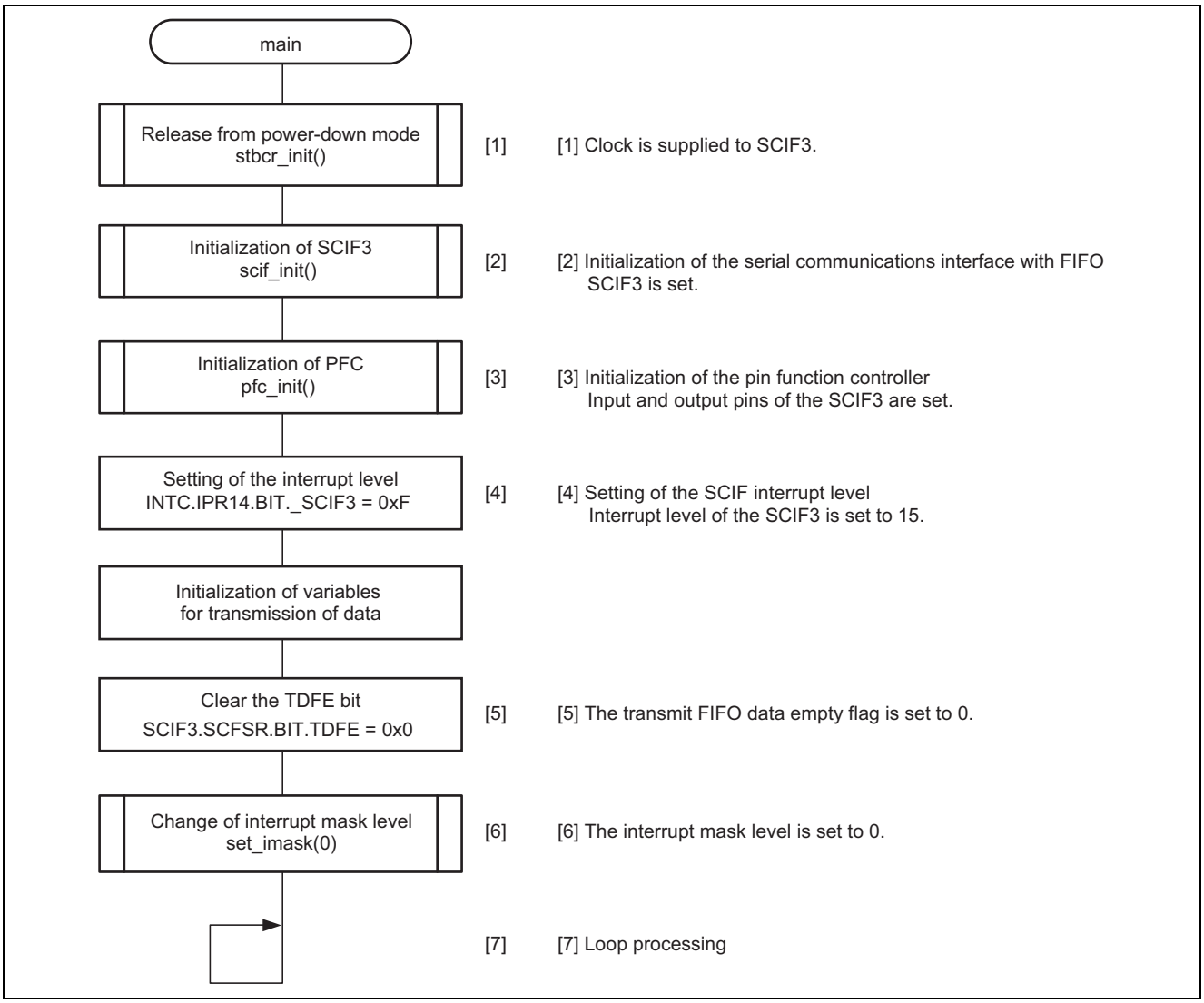

Figure 4 Flow of Processing by the Sample Program

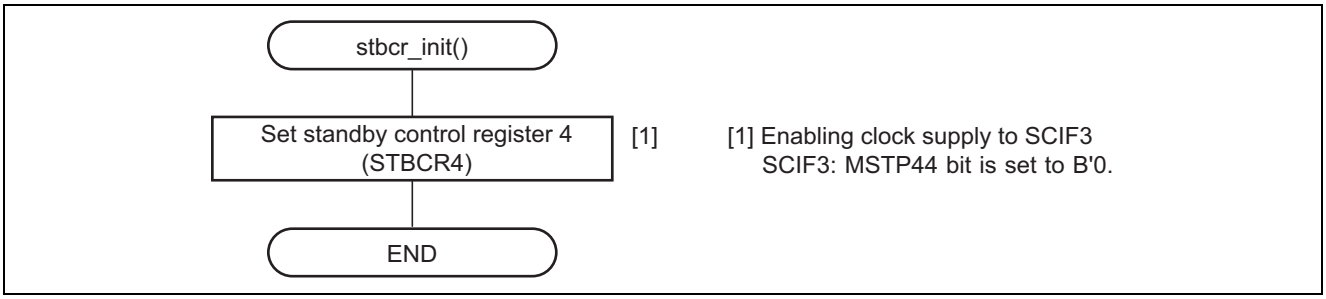

Figure 5 Flow of Settings for Release from Module-Standby Mode

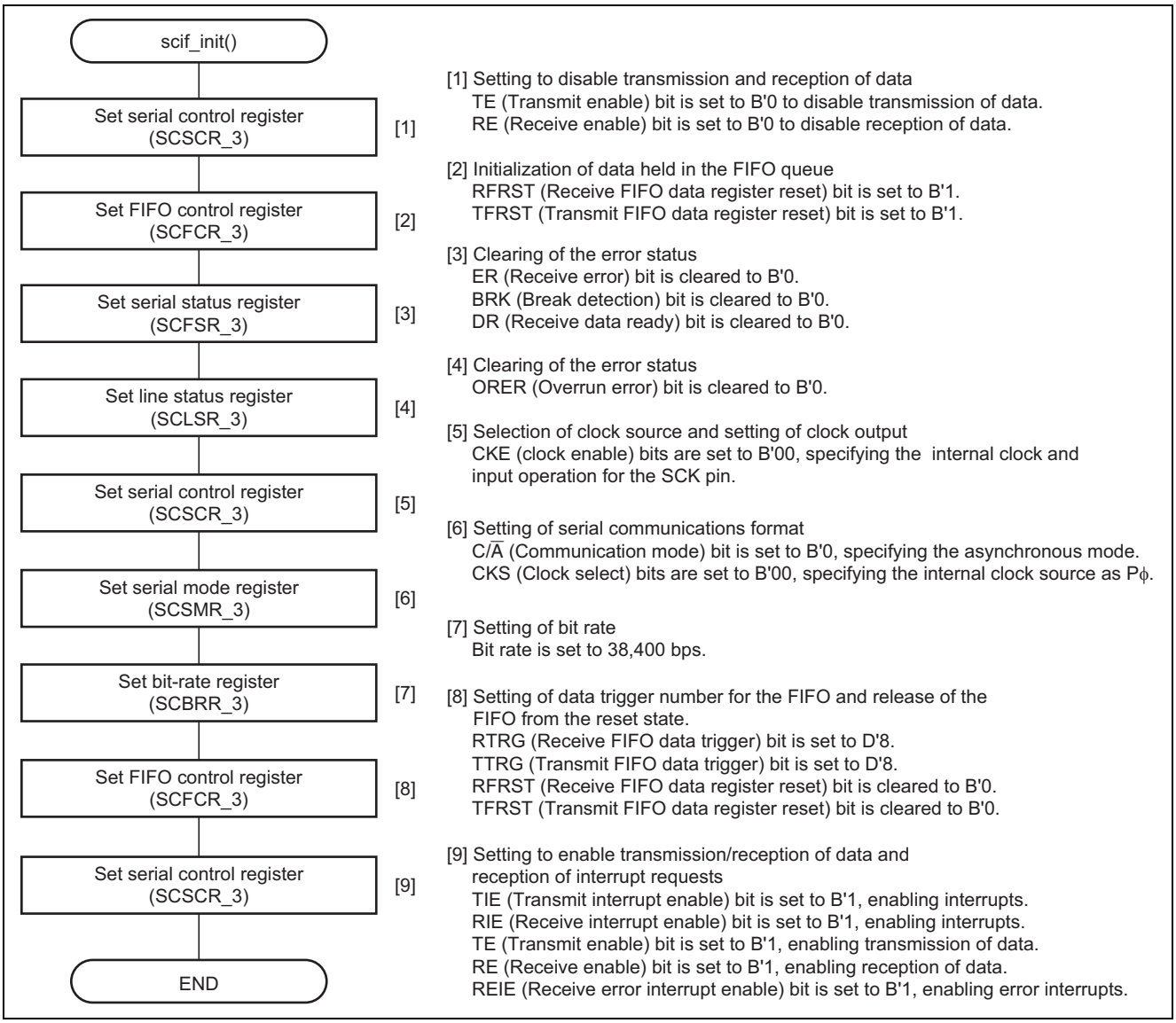

Figure 6 Flow for Initialization of Data Transmission and Reception in Asynchronous Mode

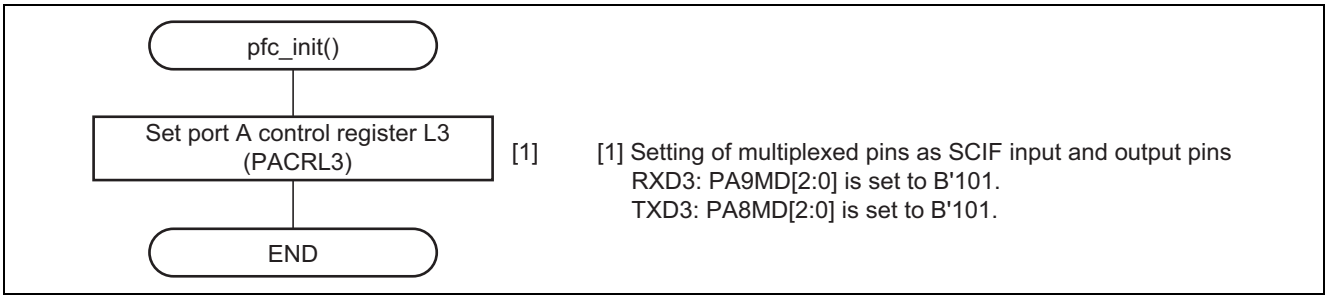

Figure 7 Flow for Setting up the Pin Function Controller

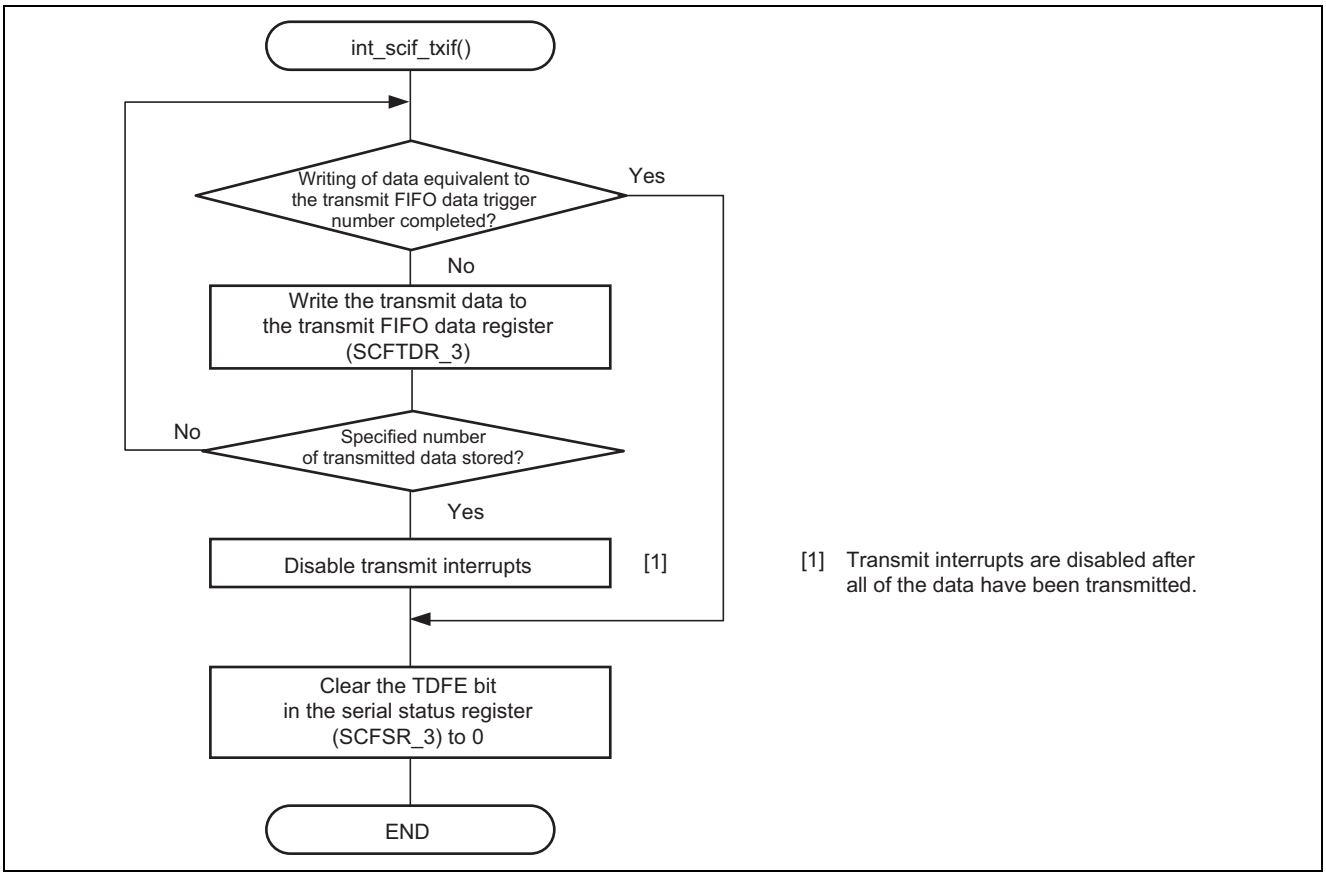

Figure 8 Flow for Handling Transmit Interrupts in Asynchronous Mode

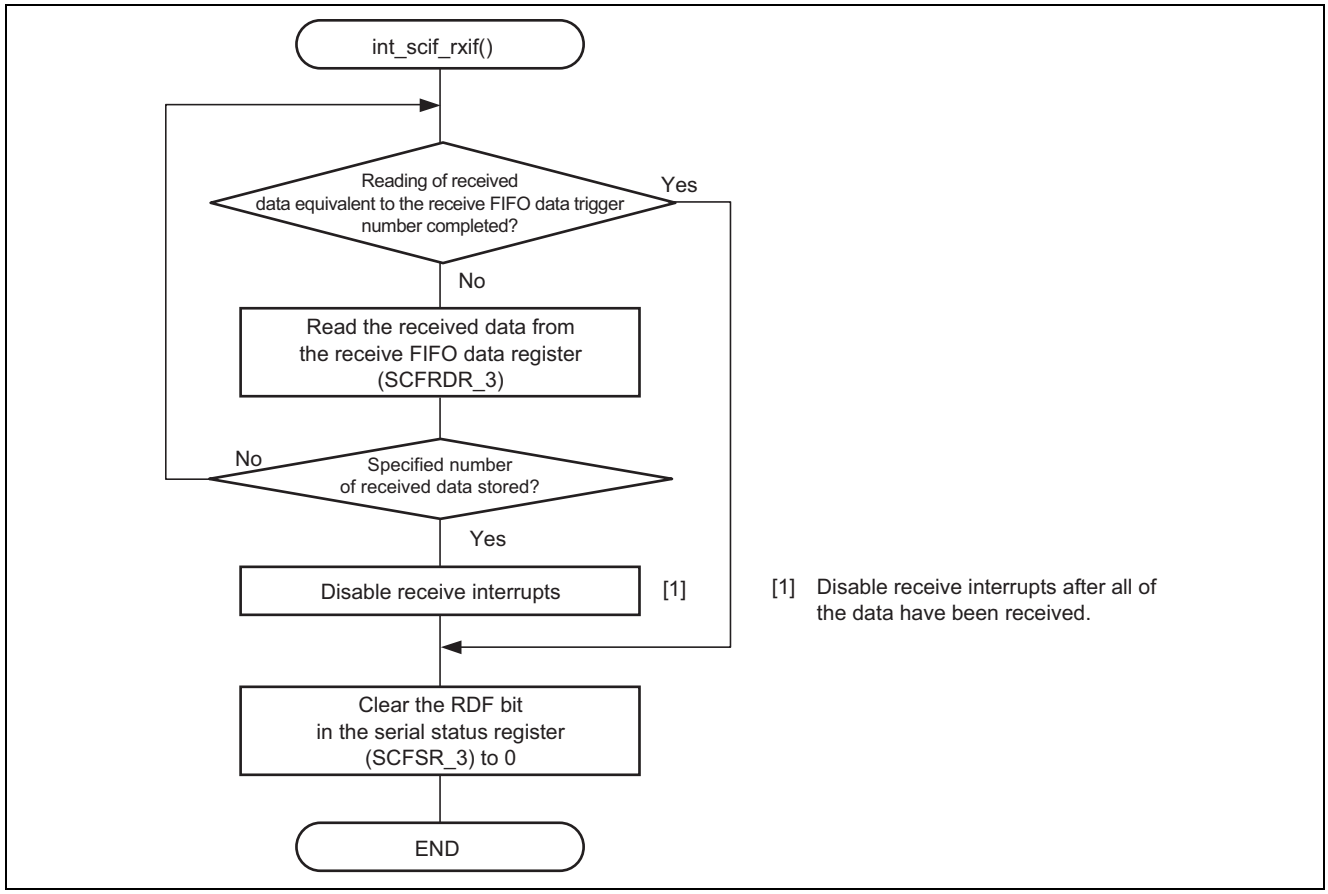

Figure 9 Flow for Handling Receive Interrupts in Asynchronous Mode

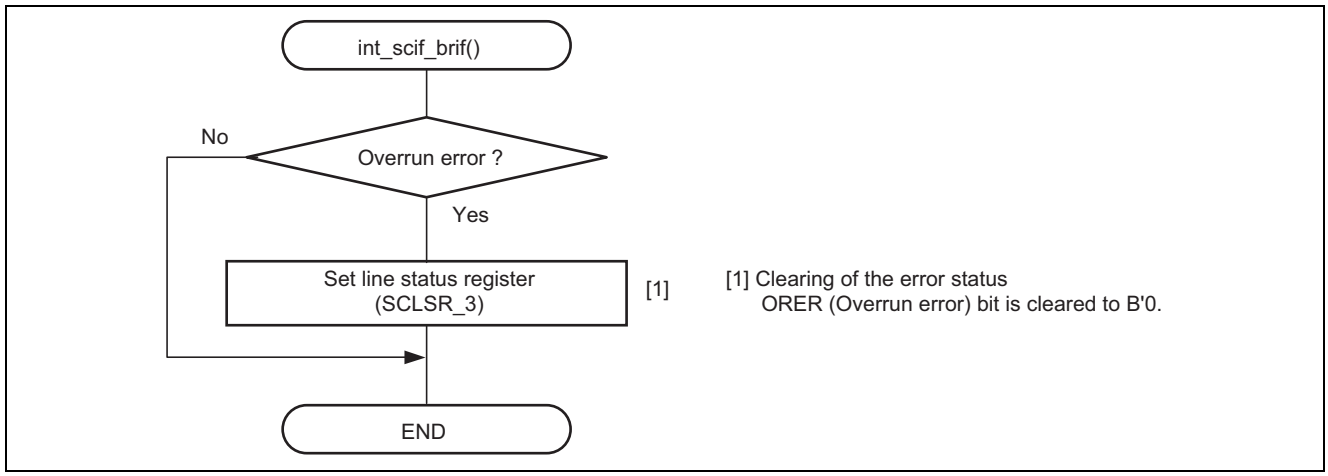

Figure 10 Flow for Handling Receive Error Interrupts in Asynchronous Mode

2.4 Procedure for Processing by the Sample Program

In this sample program, character strings are transmitted and received after initialization of SCIF3 in asynchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

Table 3 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	STC [2:0] = B'001: × 1/2 (Bϕ) IFC [2:0] = B'000: × 1 (Iϕ) PFC [2:0] = B'001: × 1/2 (Pϕ)
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	MSSCS [1:0] = B'01: PLL output clock MSDIVS [1:0] = B'01: × 1/2 (Mϕ)
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	ASSCS [1:0] = B'01: PLL output clock ASDIVS [1:0] = B'01: × 1/2 (Aϕ)

2.4.2 Low Power Consumption Mode

Table 4 gives settings for the standby control register in the sample program.

Table 4 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE 040C	H'E4	MSTP44 = B'0: SCIF3 operates

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample program.

Table 5 Settings for Register of Interrupt Controller

Register Name	Address	Setting	Description
Interrupt priority register 14 (IPR14)	H'FFFE 0C10	H'000F	IPR14 [3:0] = H'F: SCIF3 is at a level 15

Note: The interrupt priority levels of RXI3 and TXI3 are in accord with the order of the corresponding address offsets in the interrupt vector table. For details on interrupt priority levels, see Interrupt Exception Handling Vector Table and Priority in the section on interrupt controller in the *SH7280 Group Hardware Manual (REJ09B0393)*.

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

Table 6 Settings for Register of Pin Function Controller

Register Name	Address	Setting	Description
Port A control register L3 (PACRL3)	H'FFFE 3812	H'0055	PA8MD [2:0] = B'101: TXD3 output PA9MD [2:0] = B'101: RXD3 input

2.4.5 Serial Communications Interface with FIFO

Table 7 gives settings for the registers of the SCIF in the sample program.

Table 7 Settings for SCIF Register

Register Name	Address	Setting	Description
Serial mode register_3 (SCSMR_3)	H'FFFE 9800	H'0000	C/A = B'0: Asynchronous mode CHR = B'0: 8-bit data PE = B'0: Disables adding and checking of parity bits STOP = B'0: 1 stop bit CKS [1:0] = B'00: Pϕ clock
Bit rate register_3 (SCBRR_3)	H'FFFE 9804	D'124	Asynchronous mode Bit rate: 38,400 (bit/s) *[1]
Serial control register_3 (SCSCR_3)	H'FFFE 9808	H'0000	Initialization TIE = B'0: Disables transmit-FIFO-data-empty interrupt (TXI) requests RIE = B'0: Disables receive-FIFO-data-full interrupt (RXI), receive-error-interrupt (ERI) requests TE = B'0: Disables transmission of data RE = B'0: Disables reception of data
			At the time of setting Asynchronous mode CKE [1:0] = B'00: Internal clock, SCK pin is used as an input pin
		H'00F0	When transmitting and receiving operation is enabled TIE = B'1: Enables transmit-FIFO-data-empty interrupt (TXI) request RIE = B'1: Enables receive-FIFO-data-full interrupt (RXI) request TE = B'1: Enables transmission of data RE = B'1: Enables reception of data
Serial status register_3 (SCFSR_3)	H'FFFE 9810	H'0060	Initialization TDFE = B'1: Enables transmit-FIFO-data-empty flag TEND = B'1: Enables transmit end flag
		H'0000	At the time of setting All the flags are cleared.

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface with FIFO in the *SH7280 Group Hardware Manual (REJ09B0393).*

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7280 Group Hardware Manual (REJ09B0393)
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