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H8SX Family

Transition to and Exit from Exception Handling of Break Interrupts by the UBC

Introduction

The user break controller (hereinafter referred to as UBC) generates a UBC break interrupt request and executes exception handling for the UBC break interrupt each time the state of the program counter matches a specified break condition.

Target Device

H8SX/1668R Group

Preface

Other than the target device indicated above, the program covered in this application note can be run on H8SX devices that have the same I/O registers as those employed by the program. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the actual target device.

Contents

1. Specifications

An overview of operation in this application note is given in figure 1, and the operation in this application note is explained as follows:

- Channel A is used.
- The address (H'1400) where exception handling for the IRQ0 interrupt starts is set as a PC break address.
- When exception handling for the UBC break interrupt is completed, the flow of processing returns to the main loop.
- Output on pins of a test port is used to confirm the individual stages of operation: execution of the instruction at the PC break address, execution of exception handling for the UBC break interrupt, and processing of the main loop (see table 1).

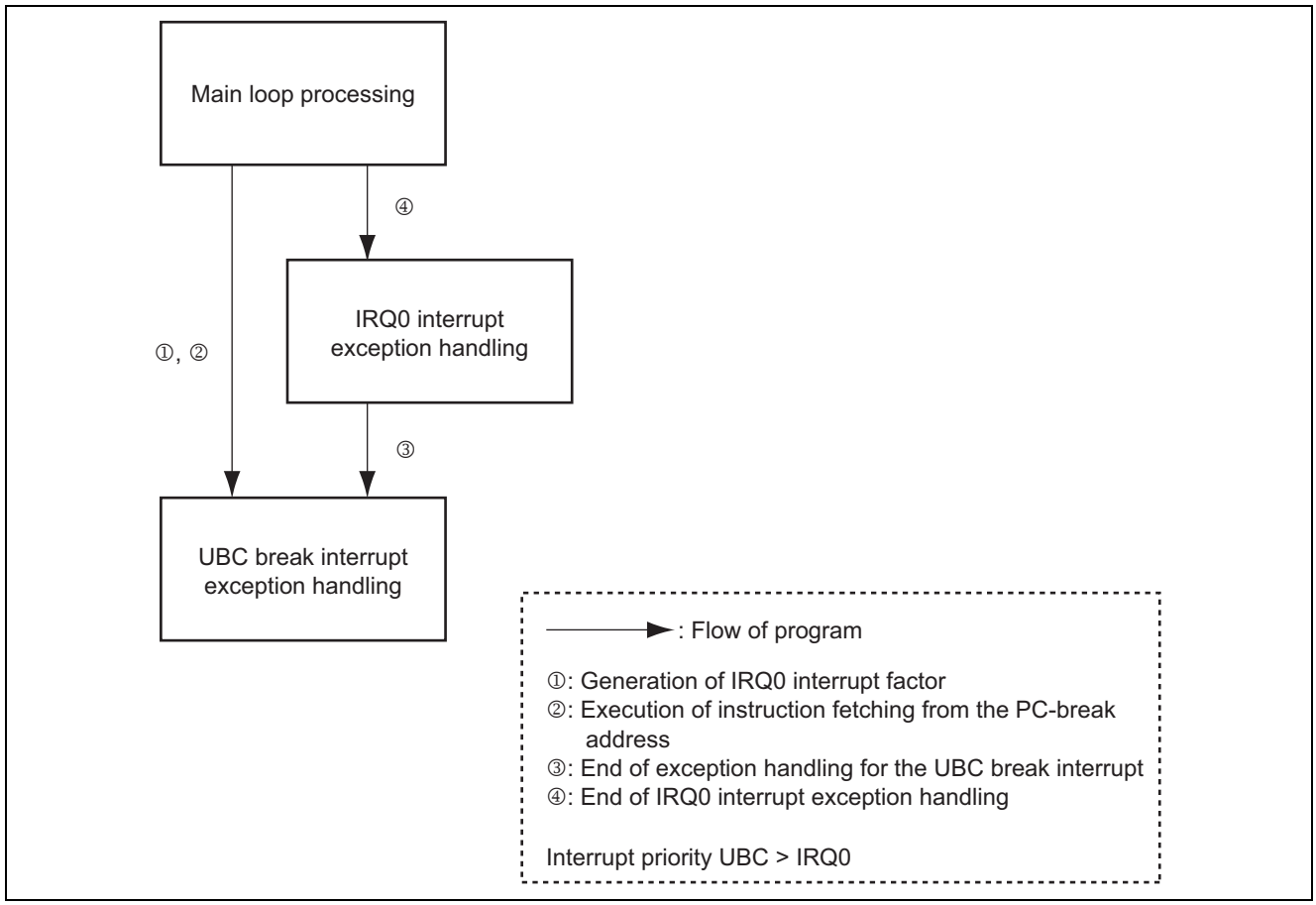

Figure 1 Overview of Operation

Table 1 Output on Test Port to Confirm Operation

Description of Verified Operation	Output Value (Port 3 in Use)
Main loop processing	P30 (inverted output)
Execution of exception handling for the UBC break interrupt	P31 (inverted output)
Execution of the instruction at the PC break address*	P32 (inverted output)

Note*: PC break address is set to the address (H'1400) where IRQ0 interrupt exception handling starts.

2. Applicable Conditions

Table 2 Applicable Conditions

Item	Detail	
Operating frequency	Input clock	: 12.5 MHz
	System clock (Iϕ)	: 50 MHz (12.5 MHz multiplied by 4)
	Peripheral module clock (Pϕ)	: 25 MHz (12.5 MHz multiplied by 2)
	External bus clock (Bϕ)	: 50 MHz (12.5 MHz multiplied by 4)
Operating mode	Mode 7 (MD3 = 0, MD2 = 1, MD1 = 1, MD0 = 1, MD_CLK = 0)	
Development tool	High-performance Embedded Workshop (HEW) Ver.4.04.01	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Ver. 6.02.00 from Renesas Technology	
Compiler option	-cpu = H8SXA:24MD, -optimize = 1, -object, -debug, -nolist, -chgincpath, -nologo	
Linker option	-start = PResetPRG/0400 P,C$DSEC,C$BSEC,D/0800, PIntPRG/01000, PInt_UBC/01200, PInt_IRQ0/01400, B,R/0FF2000, S/0FFBE00	

3. Description of Module Used

3.1 User Break Controller

The user break controller (UBC) generates a UBC break interrupt request each time the state of the program counter matches a specified break condition. The UBC break interrupt is a nonmaskable interrupt and is always accepted, regardless of the interrupt control mode and the state of the interrupt mask bit of the CPU.

Figure 2 show a block diagram of the UBC.

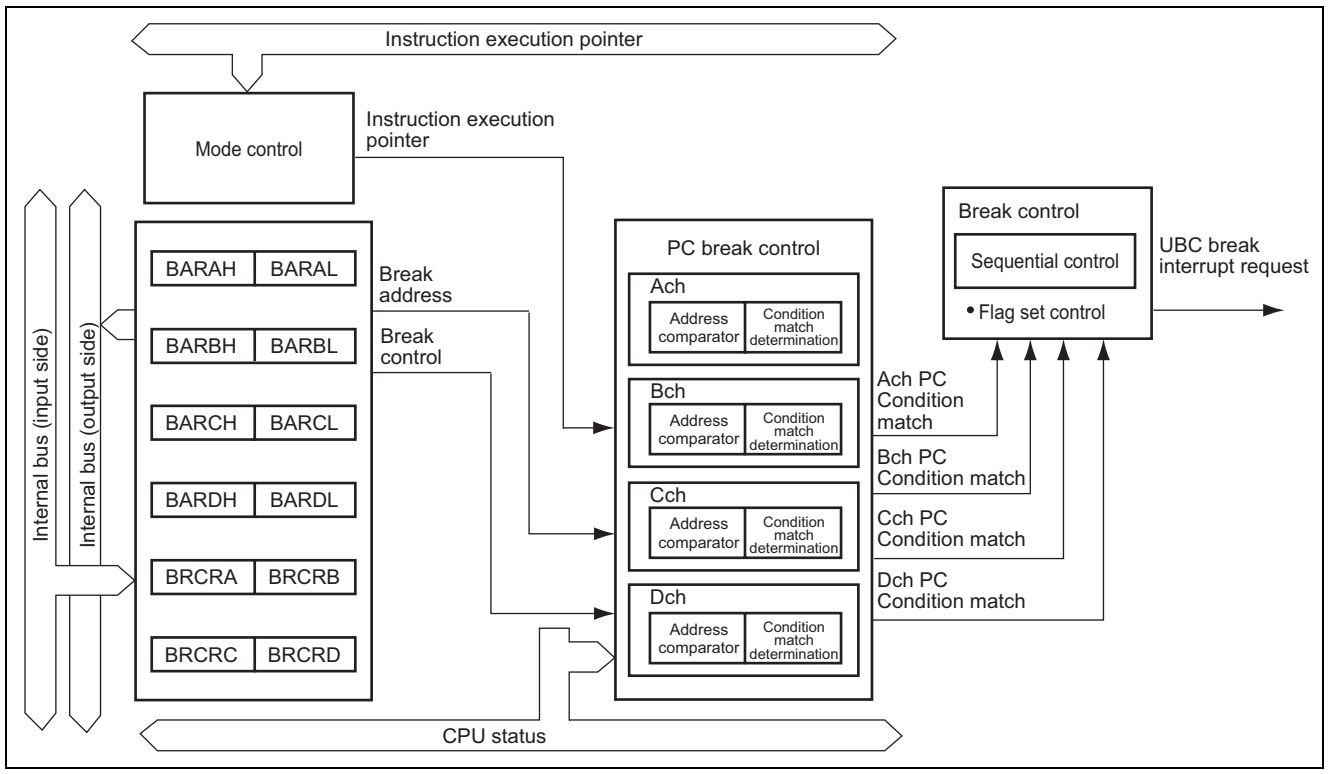

Figure 2 UBC Block Diagram

4. Principle of Operation

Figure 3 shows operation timing in this application note.

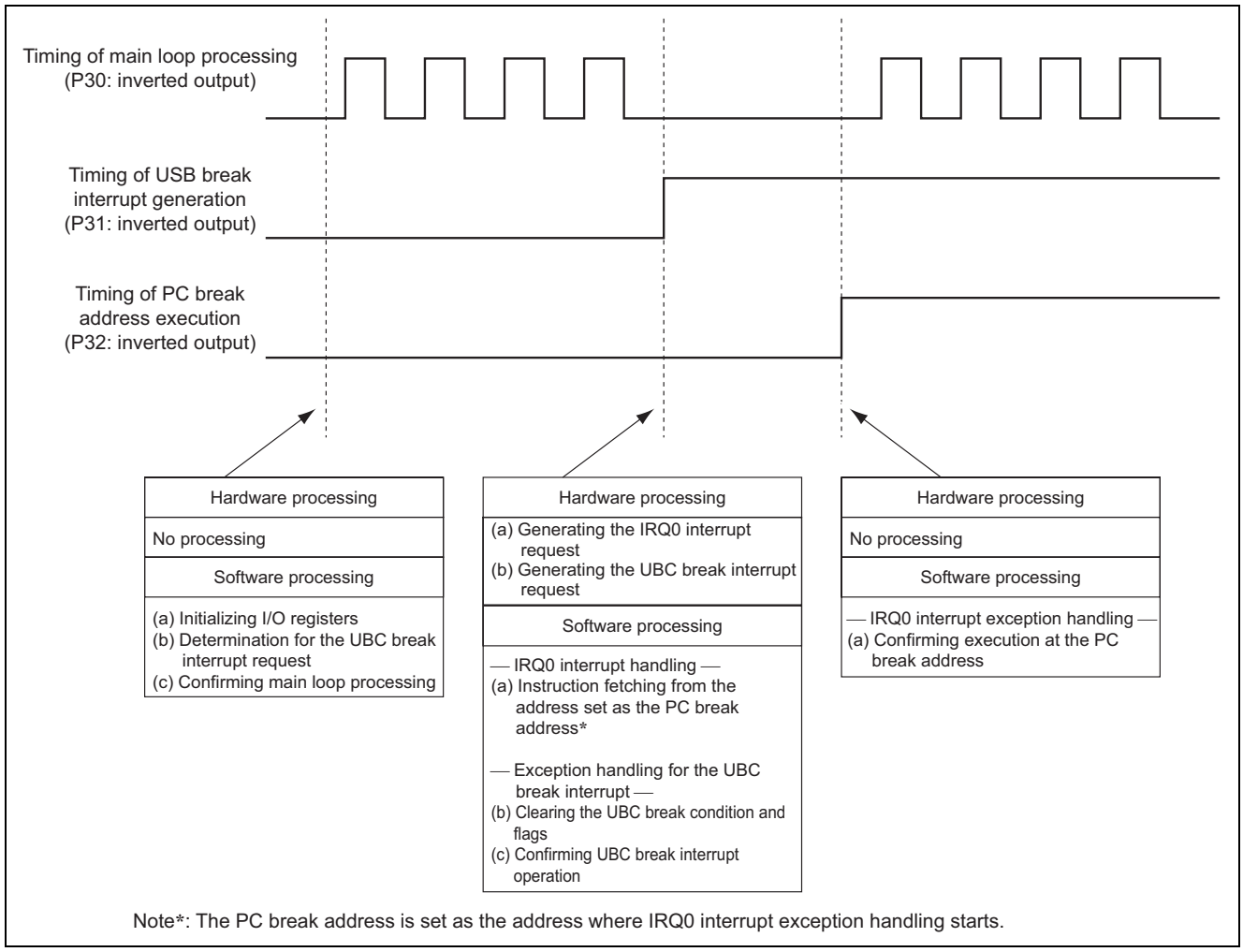

Figure 3 Operation Timing

5. Description of Software

5.1 List of Variables

Table 3 List of RAM

Variable	Label Name	Description	Referred in
unsigned char	g_ubc_flg	UBC break interrupt request flag 0: Request is not generated. 1: Request is generated.	main, init, INT_UBC

5.2 List of Functions

Table 4 List of Functions

Function Name	Description
main	• Main function Calls init function, determines whether or not a UBC break interrupt request has been generated, resets the UBC break condition, and confirms main loop processing.
init	• Initialization function Initializes registers and RAM.
INT_IRQ0	• IRQ0 interrupt function Confirms execution of the instruction at the PC break address.
INT_UBC	• UBC break interrupt function Negates the UBC break condition, sets the UBC break interrupt request flag, and confirms exception handling for the UBC break interrupt.

5.3 Description of Functions

5.3.1 main Function

1. Functional overview
   The main function calls function init to initialize the required registers and make the UBC operate. If a UBC break has been generated, it resets the UBC break condition.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Break control register A (BRCRA) Number of bits: 16 Address: H'FFFA28

Bit	Bit Name	Setting	R/W	Description
13	CMFPn	0	R/W	Condition Match CPU Flag UBC break source flag that indicates satisfaction of a specified CPU bus cycle condition. 0: The CPU cycle condition for channel A break requests has not been satisfied.
11	CPA2	0	R/W	CPU Cycle Select
10	CPA1	0		These bits select CPU cycles as the bus cycle break condition for the given channel.
9	CPA0	1		001: The bus cycle break condition is CPU cycles.
5	IDA1	0	R/W	Break Condition Select
4	IDA1	1		These bits select the PC break as the source of UBC break interrupt requests for the given channel. 01: UBC break condition is the PC break.
3	RWA1	0	R/W	Read Select
2	RWA0	1		These bits select read cycles as the bus cycle break condition for the given channel. 01: The bus cycle break condition is read cycles.

- Data register (P3DR) Number of bits: 8 Address: H'FFFF52
  Description: DR is an 8-bit readable/writable register that stores the output data of the pins to be used as the general output port.
  Setting: Inversion of the output of P30 (output is the inverse of the previous state).

5. Flowchart

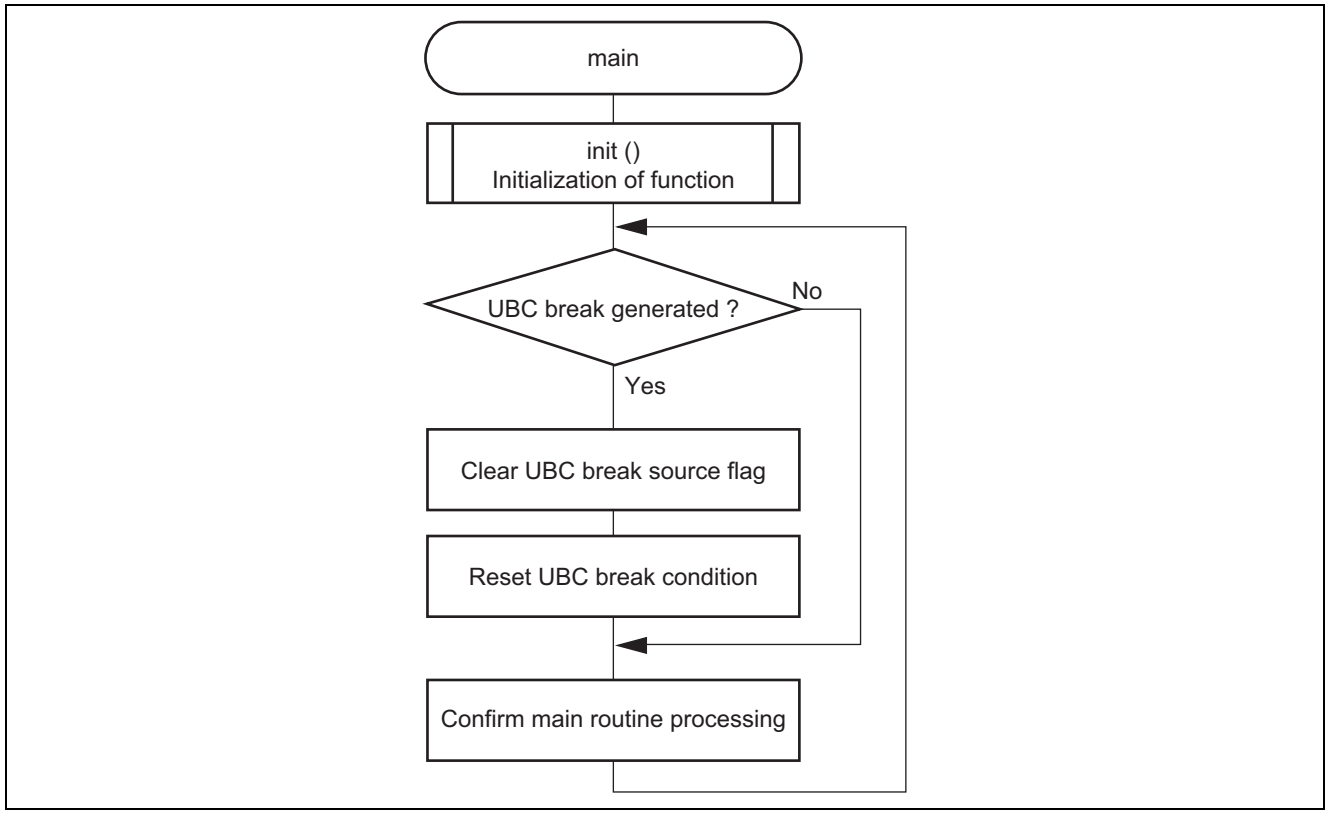

Figure 4 Flowchart (main)

5.3.2 init Function

1. Functional overview
   The init function initializes I/O registers and RAM.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0		These bits select the frequency of the system clock and the clock provided to the CPU, EXDMAC, DMAC, and DTC.
8	ICK0	0		000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0		These bits select the frequency of the peripheral module clock.
4	PCK0	1		001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0		These bits select the frequency of the external bus clock.
0	BCK0	0		000: Input clock × 4

- MSTPCRB controls module stop mode. Setting a bit to 1 makes the corresponding module enter the stop mode, while clearing the bit to 0 makes the module exit the stop mode.

- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
5	MSTPB5	0	R/W	User break controller (UBC)

- Input buffer control register (P5ICR) Number of bits: 8 Address: H'FFFB94
  Description: ICR is an 8-bit readable/writable register that controls the port input buffers.
  Setting: H'01

Note: The setting H'01 is for use of the $\overline{\text{IRQ0}}$ pin as an input pin.

- Data register (P3DR) Number of bits: 8 Address: H'FFFF52
  Description: DR is an 8-bit readable/writable register that stores the output data of the pins to be used as the general output port.
  Setting: H'00

- Data direction register (P3DDR) Number of bits: 8 Address: H'FFFB82
  Description: DDR is an 8-bit write-only register that specifies the port input or output for each bit.
  Setting: H'FF

- Port function control register C (PFCRC) Number of bits: 8 Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Description
0	ITS0	0	R/W	$\overline{\text{IRQ0}}$ Pin Select This bit selects an input pin for $\overline{\text{IRQ0}}$. 1: Selects pin P50 as $\overline{\text{IRQ0}}$-B input

- IRQ enable register (IER) Number of bits: 8 Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Description
0	IRQ0E	1	R/W	IRQ0 Enable The IRQ0 interrupt request is enabled when this bit is 1.

- IRQ sense control register L (ISCRL) Number of bits: 8 Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Description
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1		IRQ0 Sense Control Fall 01: Interrupt request generated at falling edge of $\overline{\text{IRQ0}}$

- Break address mask register A (BAMRA) Number of bits: 32 Address: H'FFFA04
  Description: Be sure to write H'FF000000 to break address mask register A (BAMRA). Operation is not guaranteed if another value is written here.
  Setting: H'FF000000

- Break address register A (BARA) Number of bits: 32 Address: H'FFFA00
  Description: BARA specifies the address used as a break condition on channel A of the UBC.
  Setting: H'00001400 (the address where $\overline{\text{IRQ0}}$ interrupt exception handling starts)

- Break control register A (BRCRA) Number of bits: 16 Address: H'FFFA28

Bit	Bit Name	Setting	R/W	Description
13	CMFPn	0	R/W	Condition Match CPU Flag UBC break source flag that indicates satisfaction of a specified CPU bus cycle condition. 0: The CPU cycle condition for channel A break requests has not been satisfied.
11	CPA2	0	R/W	CPU Cycle Select
10	CPA1	0		These bits select CPU cycles as the bus cycle break condition for the given channel.
9	CPA0	1		001: The bus cycle break condition is CPU cycles.
5	IDA1	0	R/W	Break Condition Select
4	IDA1	1		These bits select the PC break as the source of UBC break interrupt requests for the given channel. 01: UBC break condition is the PC break.
3	RWA1	0	R/W	Read Select
2	RWA0	1		These bits select read cycles as the bus cycle break condition for the given channel. 01: The bus cycle break condition is read cycles.

5. Flowchart

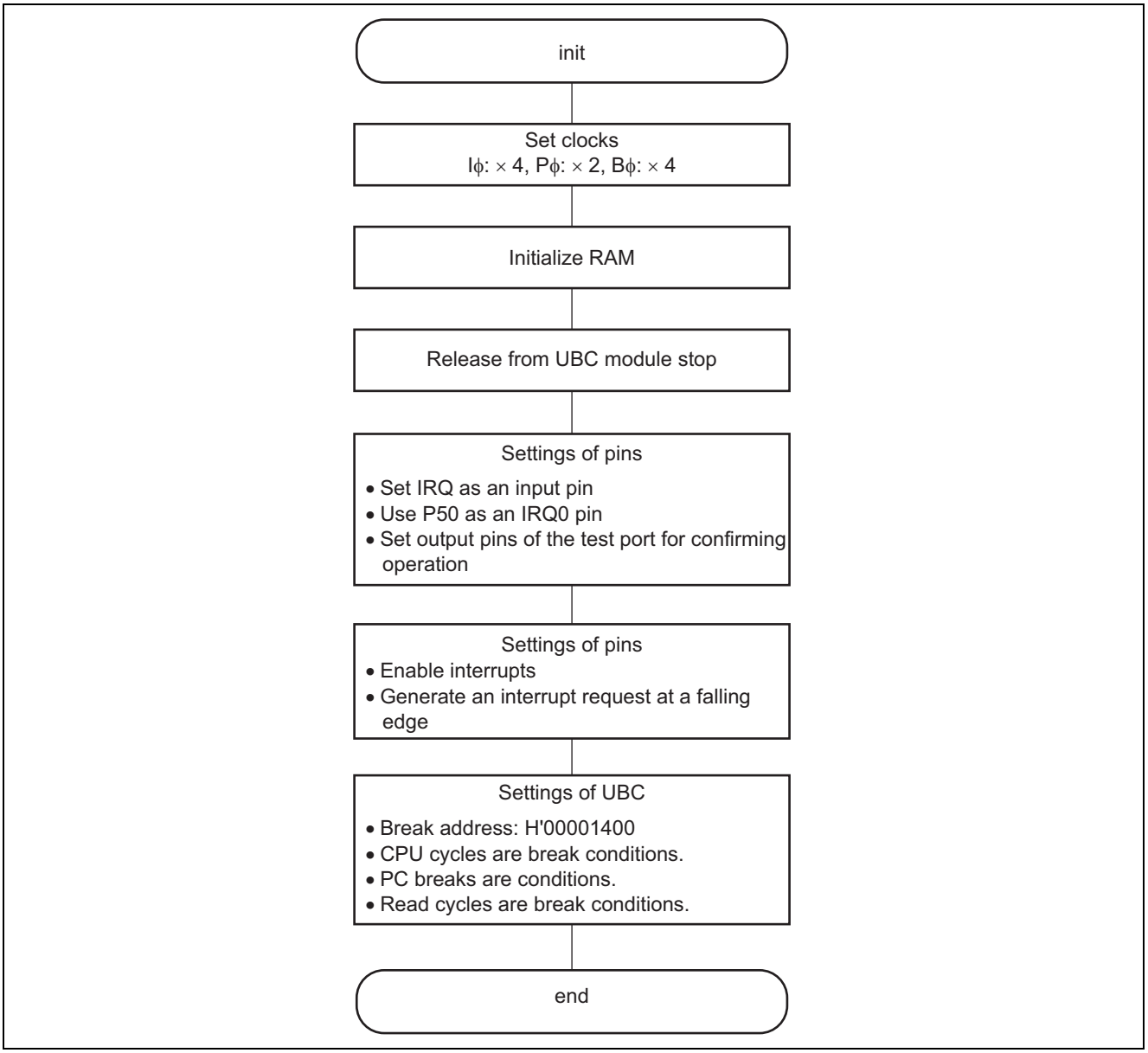

Figure 5 Flowchart (init)

5.3.3 INT_IRQ0 Function

1. Functional overview
   The INT_IRQ0 function confirms its own operation through the output of signals from the test port for confirming operation.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal register used in this sample task is described below. The setting shown in the table is the value used in this sample task and differs from the initial value.

- Data register (P3DR) Number of bits: 8 Address: H'FFFF52
  Description: DR is an 8-bit readable/writable register that is used to store the output data for the pins of the general output port.
  Setting: Output of P32 is inverted (output of the previous value is inverted).

5. Flowchart

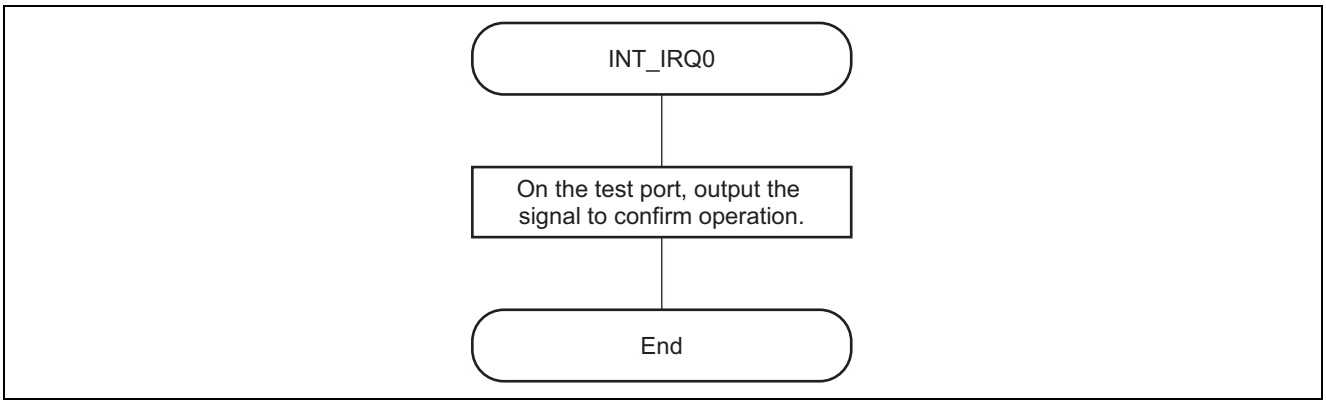

Figure 6 Flowchart (INT_IRQ0)

5.3.4 INT_UBC Function

1. Functional overview
   The INT_UBC function clears the UBC break condition then confirms its own operation through the output of a signal from the test port for confirming operation.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal register used in this sample task is described below. The setting shown in the table is the value used in this sample task and differs from the initial value.

5. Flowchart

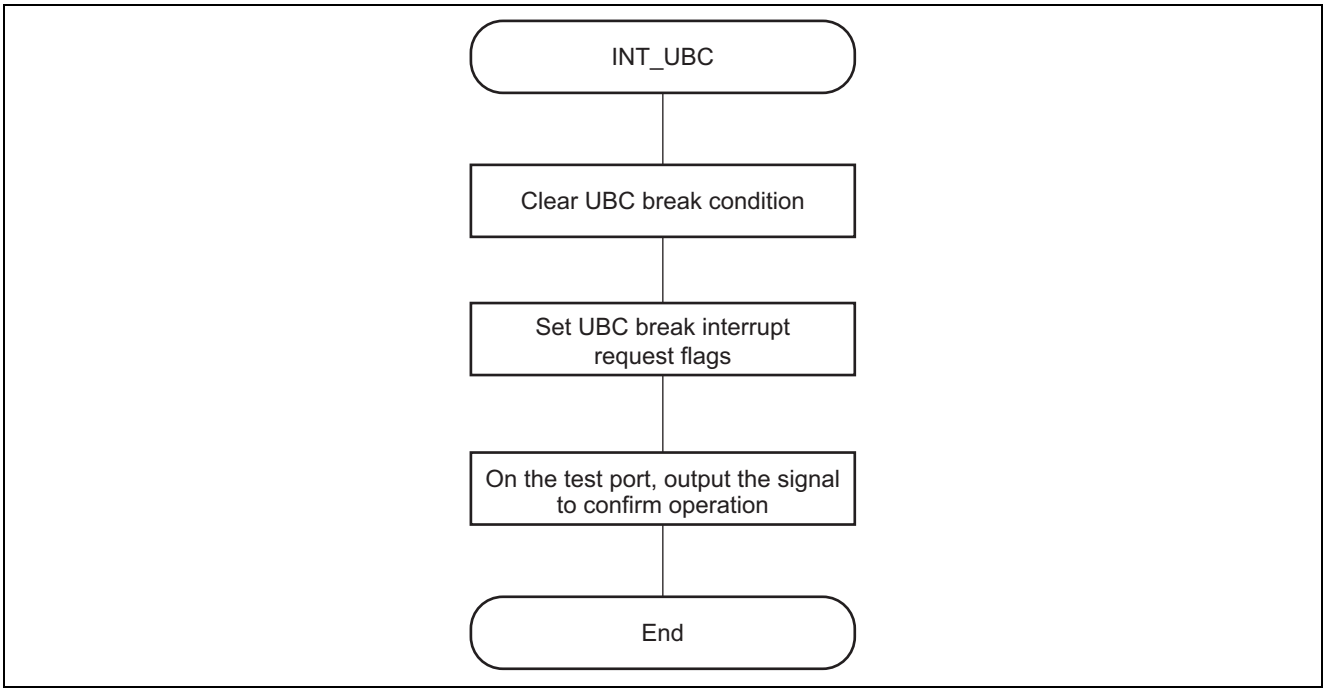

Figure 7 Flowchart (INT_UBC)

6. Precaution

(1) When pins of the device are used as the input pins of peripheral module, the corresponding bit in the input buffer control register (PnICR) is set as 1.
For details, refer to the appropriate hardware manual.

7. Documents for Reference

- Hardware Manual
  H8SX/1668R Group Hardware Manual
  The most up-to-date version of this document is available on Renesas Technology Website.
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