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SH7262/SH7264 Group

Transferring Program to RAM (DMA Transfer)

Summary

This application note describes an example of transferring program to RAM using the SH7262/SH7264 Microcomputers (MCUs) Direct Memory Access Controller (DMAC).

Target Device

SH7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

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1. Introduction

1.1 Specifications

Activates the SH7264 MCU Direct Memory Access Controller (DMAC) to transfer program from an external ROM to internal RAM, and executes the program on internal RAM.

1.2 Modules Used

- Direct Memory Access Controller (DMAC)

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequency	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.04.01
C compiler	Renesas Technology SuperH RISC engine Family C/C++ compiler package Ver.9.02 Release 00
Compiler options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7262/SH7264 Group Example of Initialization
- SH7262/SH7264 Group Transferring Program to RAM (CPU Transfer)

2. Applications

The SH7264 DMAC transfers program from an external ROM to internal RAM, and executes the program on internal RAM.

2.1 Section Alignment in the Sample Program

Use the compiler extended specifications #pragma section to change the section name of the program to transfer. The sample program changes the section of the transfer source program to PROM, and the section of the transfer destination program on internal RAM to PRAM. The following figure shows the memory map in the sample program.

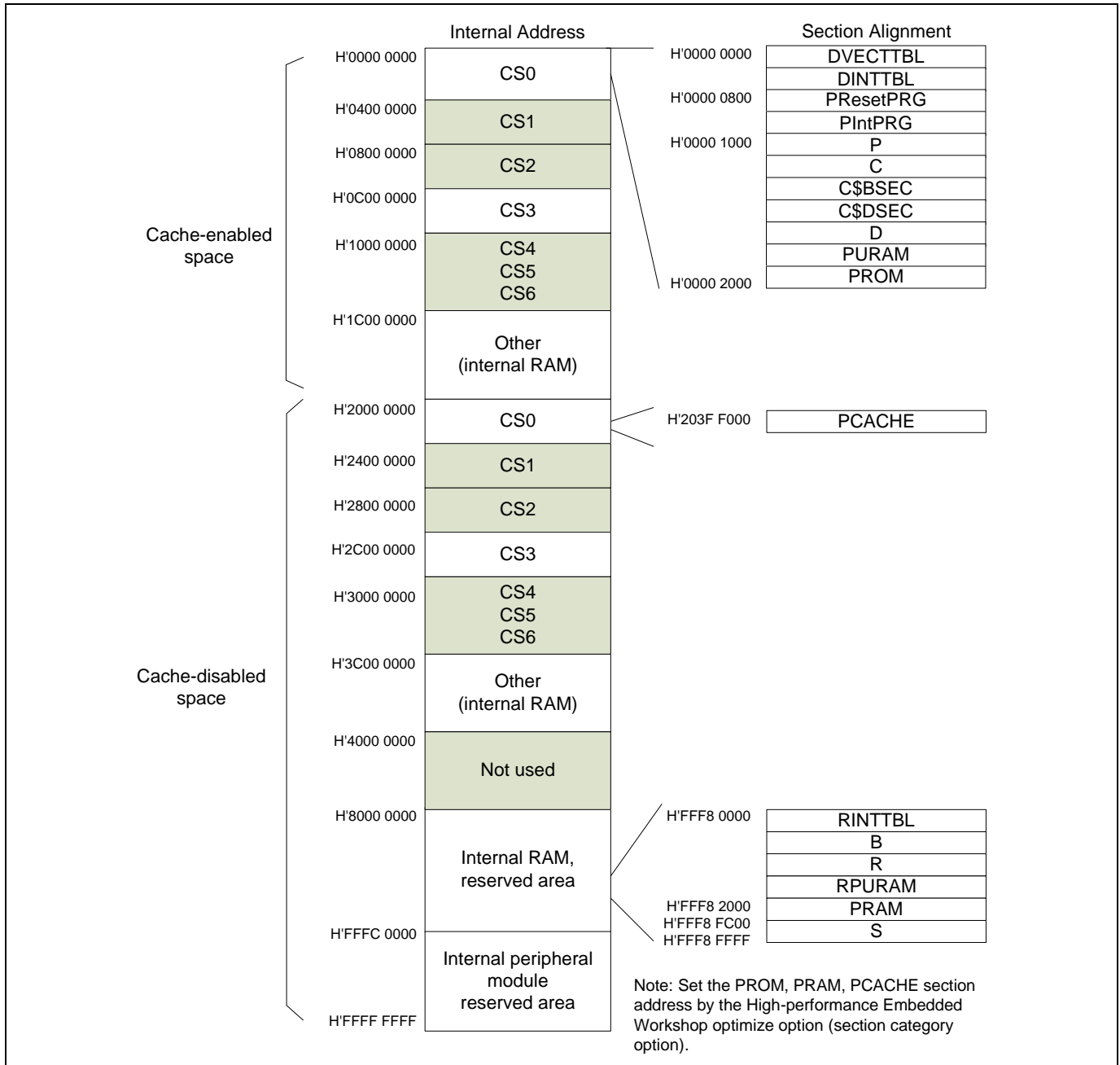


Figure 1 Memory Map

2.2 Linkage Editor Setting

Specify the section address by the linkage editor options. Table 1 lists sections to transfer in the sample program. Table 2 lists linkage editor options to use.

Table 1 Sections to Transfer

Section Name	Description
PROM	Transfer source
PRAM	Transfer destination

Note: When specifying the section address, select [Build] menu on the High-performance Embedded Workshop window, and open the [SuperH RISC engine Standard Toolchain] dialog box. For details, refer to the High-performance Embedded Workshop User's Manual.

Table 2 Linkage Editor Options

Option	Description
-rom=D=R,DINTTBL=RINTTBL, PURAM=RPURAM, PROM=PRAM	Specifies ROM to RAM mapped sections
start=DVECTTBL,DINTTBL/00,PResetPRG, PIntPRG/0800,P,C,C\$BSEC,C\$DSEC,D,PURAM, PROM/01000 ,PCACHE/0203FF000,RINTTBL,B, R,RPURAM/0FFF80000, PRAM/0FFF82000 ,S/0FFF8FC00	Specifies a section starting address

2.3 Retrieving the Section Address

Use the section address operators listed in the following table to retrieve the section address in the program.

Table 3 Address Operators

Format	Description
__sectop (" <section name> ")	Refers to the starting address of the specified <section name>.
__secend (" <section name> ")	Refers to the end address +1 of the specified <section name>.
__secsz (" <section name> ")	Generates the size of the specified <section name>.

2.4 Sample Program Operation

The sample program sets the DMAC in auto request mode, transfers the section PROM size program from the section PROM starting address in CS0 space to the section PRAM allocated on internal RAM. To verify that this works, allocate a function using the compare match timer (io_blink_led function) to the section PROM, and transfers it on internal RAM. When the transfer is completed, the sample program executes the io_blink_led function.

2.5 Note for altering the transfer procedure by CPU

When the CPU transfers the program (transfer by software) to the cache-enabled space while the operand cache (write back mode) is enabled, the program transferred may be fetched by the operand cache and the instruction fetch may not be executed. Write back the operand cache before transferring the program to the cache-enabled space by CPU.

As the sample program transfers program by the DMAC, this is not applicable.

2.6 Sample Program Flow

Table 4 shows the register settings in the sample program. Figure 2 shows flow chart of the sample program.

Table 4 Register Settings for Program Transfer

Register Name	Address	Setting	Function
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP8 = "0": DMAC is operating
DMA channel control register_0 (CHCR_0)	H'FFFE 100C	H'0000 0000	Before enabling DMA <ul style="list-style-type: none"> DE = 0: Disables the DMA transfer
		H'8000 5428	DMA Configuration <ul style="list-style-type: none"> TC = 1: Transfers data for number of times specified by the DMATCR, by a transfer request RLDSAR = 0: Disables the function to reload SAR RLDDAR = 0: Disables the function to reload DAR TEMASK = 0: Stops transfer when TE bit is set to 1 DM [1:0] = B'01: Increments the destination address SM [1:0] = B'01: Increments the source address RS [3:0] = B'0100: Auto request
		H'8000 5429	<ul style="list-style-type: none"> TB = 1: Burst mode TS [1:0] = B'01: Transfers data in words DE = 0: Disables the DMA transfer When DMA transfer is enabled: <ul style="list-style-type: none"> DE = 1: Enables the DMA transfer
DMA source address register_0 (SAR_0)	H'FFFE 1000	–	<ul style="list-style-type: none"> Transfer source address: Starting address in the section PROM
DMA destination address register (DAR_0)	H'FFFE 1004	–	<ul style="list-style-type: none"> Transfer destination address: Starting address in the PRAM section
DMA transfer count register_0 (DMATCR_0)	H'FFFE 1008	–	Number of times of DMA transfer: 1/2 of the section PROM size
DMA operation register (DMAOR)	H'FFFE 1200	H'0000 0001	<ul style="list-style-type: none"> DME = 1: Enables the DMA transfer on all channels

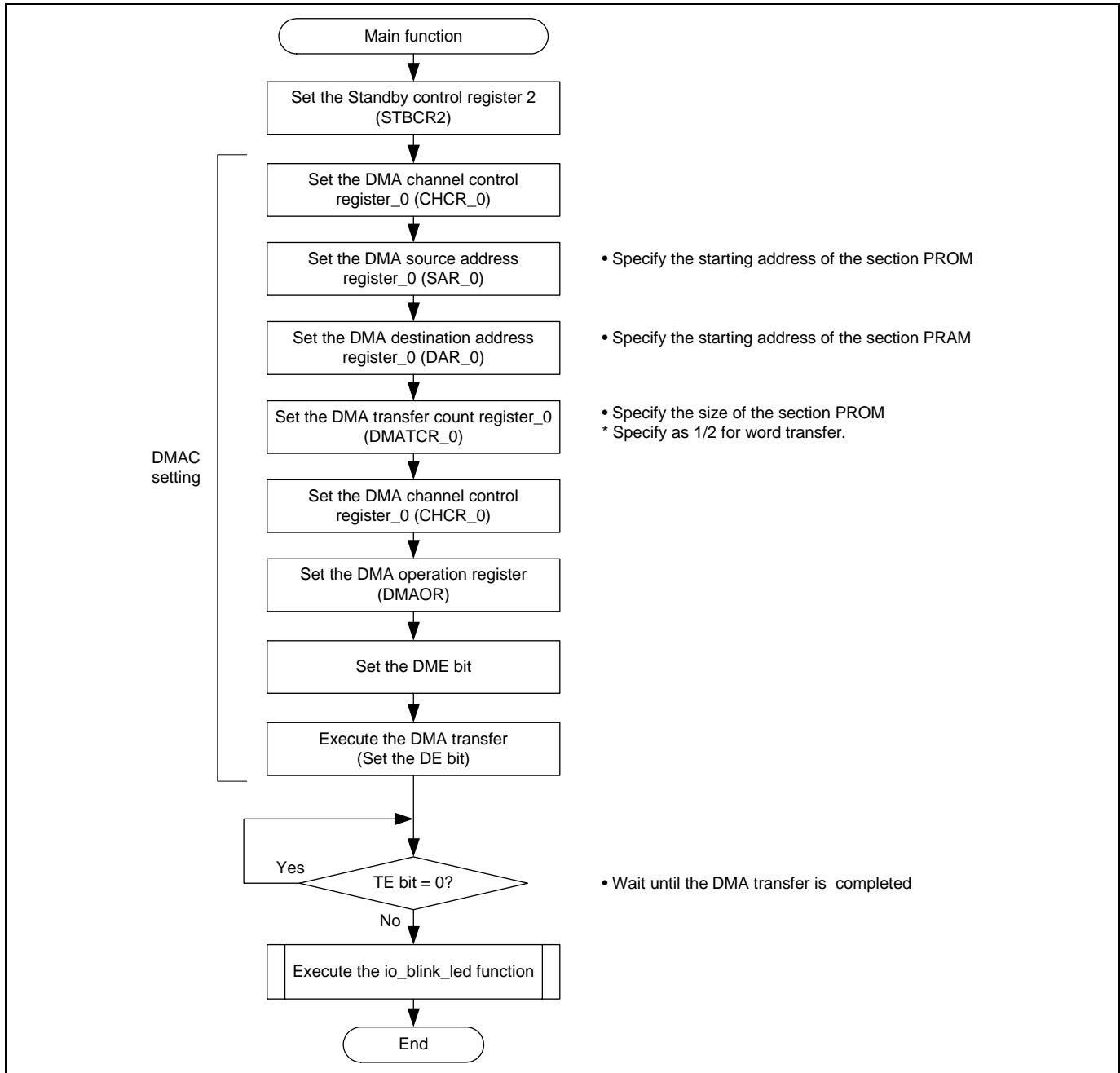


Figure 2 Sample Program Flow Chart

3. Sample Program Listing

3.1 Sample Program Listing "main.c" (1/6)

```

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3      *
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25     *   conditions found by accessing the following link:
26     *   http://www.renesas.com/disclaimer
27     *****/
28     *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29     *"FILE COMMENT"***** Technical reference data *****
30     *   System Name   : SH7264 Sample Program
31     *   File Name    : main.c
32     *   Abstract     : Transferring Program to RAM (DMA Transfer).
33     *   Version      : 1.00.00
34     *   Device       : SH7262/SH7264
35     *   Tool-Chain   : High-performance Embedded Workshop (Ver.4.04.01).
36     *                 : C/C++ compiler package for the SuperH RISC engine family
37     *                 :                               (Ver.9.02 Release00).
38     *   OS           : None
39     *   H/W Platform: M3A-HS64G50 (CPU board)
40     *   Description  :
41     *****/
42     *   History      : Aug.04,2009 Ver.1.00.00
43     *"FILE COMMENT END"*****/
44     #include <machine.h>
45     #include "iodefine.h"

```

3.2 Sample Program Listing "main.c" (2/6)

```

46
47  /* ==== Prototype declaration ==== */
48  void main(void);
49  void io_blink_led(void);
50  void io_init_cmt0(void);
51
52  /*"FUNC COMMENT"*****
53  * ID      :
54  * Outline : Sample program main (Transfer program from ROM to RAM).
55  *-----
56  * Include : iodef.h
57  *-----
58  * Declaration : void main(void);
59  *-----
60  * Description : Transfers the section PROM to the section PRAM allocated on
61  *              : internal RAM by the DMAC, and executes the transferred program
62  *              : (io_blink_led function).
63  *-----
64  * Argument  : void
65  *-----
66  * Return Value : void
67  *-----
68  * Note      :
69  *"FUNC COMMENT END"*****
70  void main(void)
71  {
72     unsigned long dummy;
73
74     /* ==== Sets the Standby control register 2 (STBCR2) ==== */
75     CPG.STBCR2.BIT.MSTP8 = 0;      /* Enables the DMAC */
76
77     /* ---- Sets the DMA channel control register_0 (CHCR_0) ---- */
78     DMAC.CHCR0.BIT.DE = 0;        /* Disables the DMA transfer */
79
80     /* ==== Sets the DMA source address register_0 (SAR_0) ==== */
81     DMAC.SAR0.LONG = (unsigned long)__sectop("PROM"); /* Refers to the starting
82                                                         address in the section PROM */
83
84     /* ==== Sets the DMA destination address register_0 (DAR_0) ==== */
85     DMAC.DAR0.LONG = (unsigned long)__sectop("PRAM"); /* Refers to the starting
86                                                         address in the section PRAM */
87
88     /* ==== Sets the DMA transfer count register_0 (DMATCR_0) ==== */
89     DMAC.DMATCR0.LONG = __seclen("PROM") / sizeof(unsigned short);
90

```

3.3 Sample Program Listing "main.c" (3/6)

```

91      /* ==== Sets the DMA channel control register_0 (CHCR_0) ==== */
92      dummy = DMAC.CHCR0.LONG;
93      DMAC.CHCR0.LONG = 0x80005428ul;
94      /*
95          bit 31      : TC DMATCR transfer: 1----- Number of times
96                                by DMATCR
97          bit 30      : reserve 0
98          bit 29      : RLDSAR: 0----- Disables the function
99                                to reload SAR
100         bit 28      : RLDDAR: 0----- Disables the function
101                                to reload DAR
102         bit 27      : reserve 0
103         bit 26      : DAF: 0----- Not used
104         bit 25      : SAF: 0----- Not used
105         bit 24      : reserve 0
106         bit 23      : DO: 0----- Not used
107         bit 22      : TL: 0----- Not used
108         bit 21      : reserve 0
109         bit 20      : TEMASK: 0----- Stops transfer
110                                when TE bit is 1
111         bit 19      : HE: 0----- Not used
112         bit 18      : HIE: 0----- Not used
113         bit 17      : AM: 0----- Not used
114         bit 16      : AL: 0----- Not used
115         bit 15 to 14: DM [1:0]: B'01----- Increments
116                                the destination address
117         bit 13 to 12: SM [1:0]: B'01----- Increments
118                                the source address
119         bit 11 to 8  : RS [3:0]: B'0100----- Auto request
120         bit 7       : DL: DREQ level : 0 ----- Not used
121         bit 6       : DS: DREQ select : 0 ----- Not used
122         bit 5       : TB: 1----- Burst mode
123         bit 4 to 3  : TS [1:0]: B'01----- Transfers data
124                                in words
125         bit 2       : IE: 0----- Disables interrupts
126         bit 1       : TE: 0----- Clears the TE flag
127         bit 0       : DE: 0----- Disable the DMA transfer
128     */
129

```

3.4 Sample Program Listing "main.c" (4/6)

```

130  /* ==== Sets the DMA operation register (DMAOR) ==== */
131  dummy = DMAC.DMAOR.WORD;
132  DMAC.DMAOR.WORD = 0x0000u;
133  /*
134          bit 15 to 14: reserve 0
135          bit 13 to 12: CMS [1:0]: B'00----- Normal mode
136          bit 11 to 10: reserve 0
137          bit 9 to 8  : PR [1:0]: B'00----- Fixed mode 1
138          bit 7 to 3  : reserve 0
139          bit 2      : AE: 0----- Clears the
140                          address error flag
141          bit 1      : NMIF: 0----- Clears the NMI flag
142          bit 0      : DME: 0----- Disables the DMA
143                          transfer on all channels
144          */
145  /* ==== Sets the DME bit ==== */
146  DMAC.DMAOR.BIT.DME = 1;
147
148  /* ==== Executes the DMA (sets the DE bit) ==== */
149  DMAC.CHCR0.BIT.DE = 1;
150
151  /* ==== Waits for the DMA transfer end ==== */
152  while( DMAC.CHCR0.BIT.TE == 0 ){
153      /* Wait */
154  }
155  /* ==== Executes the CMT0 function ==== */
156  io_blink_led();          /* Inverts port A0 */
157  }
158
159  #pragma section ROM      /* Following section P is handled as section PROM */

```

3.5 Sample Program Listing "main.c" (5/6)

```

160  /*"FUNC COMMENT"*****
161  * ID          :
162  * Outline     : Count at a constant period
163  *-----
164  * Include     : iodef.h
165  *-----
166  * Declaration : void io_blink_led(void);
167  *-----
168  * Description : Initializes the I/O port PA0 (connected to LED) and the
169  *              : compare match timer CMT0 at 1 ms to turn ON or OFF the LED
170  *              : connected to the PA0 once every 1000 times 1 ms flag
171  *              : (interrupt request bit) is set.
172  *-----
173  * Argument    : void
174  *-----
175  * Return Value : void
176  *-----
177  * Note        : Add the section PROM and transfer section PRAM in the linkage editor
178  *              : options and set the [ROM to RAM mapped sections].
179  *"FUNC COMMENT END"*****/
180  void io_blink_led(void)
181  {
182      volatile unsigned int CountCMT0 = 1000;    /* For 1 sec soft count */
183
184      /* ==== Initializes the LED ==== */
185      /* ---- PB22 (Control signal to enable the PA0) ---- */
186      PORT.PBCR5.BIT.PB22MD = 0;                /* Sets the function of the PB22 pin
187                                               to general-purpose I/O */
188      PORT.PBDR1.BIT.PB22DR = 1;                /* Specifies the output data as 1 */
189      PORT.PBIOR1.BIT.PB22IOR = 1;             /* Specifies the direction to output */
190      /* ---- PA0 (Signal to turn ON or OFF the LED) ---- */
191      PORT.PADR0.BIT.PA0DR = 1;                /* Specifies the output data as 1 */
192      PORT.PAIOR0.BIT.PA0IOR = 1;             /* Specifies the direction to output */
193
194      /* ==== Initializes the CMT0 (1 ms periodic timer) ==== */
195      io_init_cmt0();
196
197      while(1){
198          /* ---- Verifies the compare match (1 ms) flag ---- */
199          while (CMT.CMCSR0.BIT.CMF == 0){
200              /* Waits for 1 ms elapsed */
201          }
202          CMT.CMCSR0.BIT.CMF = 0;                /* Clears the compare match flag (CMF) to 0 */
203          CountCMT0--;                          /* Updates the 1 sec soft counter (CountCMT0) */

```

3.6 Sample Program Listing "main.c" (6/6)

```

204     /* ---- Verifies the 1 sec soft counter ---- */
205     if(CountCMT0 == 0u){
206         CountCMT0 = 1000u;          /* Initializes the 1 sec soft counter again */
207         PORT.PADR0.BIT.PA0DR ^= 1u ; /* Inverts the port A0 output */
208     }
209 }
210 }
211 /*"FUNC COMMENT"*****
212 * ID          :
213 * Outline     : CMT0 periodic timer setting
214 *-----
215 * Include     : iodefne.h
216 *-----
217 * Declaration : void io_init_cmt0(void);
218 *-----
219 * Description : Sets the CMT0 to set the CMF flag at every 1 ms.
220 *-----
221 * Argument    : void
222 *-----
223 * Return Value : void
224 *-----
225 * Note        : Add the section PROM and transfer section PRAM in the linkage editor
226 *              : options and set the [ROM to RAM mapped sections].
227 *"FUNC COMMENT END"*****
228 void io_init_cmt0(void)
229 {
230     /* ==== Configures the periodic (1 ms) timer ==== */
231     /* ---- Sets the Standby control register 7 (STBCR7) ---- */
232     CPG.STBCR7.BIT.MSTP72 = 0x0; /* Enables the CMT */
233
234     /* ---- Sets the Compare match timer start register (CMSTR) ---- */
235     CMT.CMSTR.BIT.STR0 = 0;      /* Stops channel 0 to count */
236
237     /* ---- Sets the Compare match timer control/status register (CMCSR0) ---- */
238     CMT.CMCSR0.WORD = 0x0002;    /* Disables the compare match interrupt,
239                                   specifies 1/128 of the peripheral clock */
240
241     /* ---- Sets the Compare match timer counter register (CMCNT0) ---- */
242     CMT.CMCNT0.WORD = 0x0000;    /* Clears the timer counter */
243
244     /* ---- Sets the Compare match timer constant register (CMCOR0) ---- */
245     CMT.CMCOR0.WORD = 280;       /* Sets the period to compare match (1 ms) */
246                                   /* 1ms = 1/P clock (36 MHz) * 128 * (280+1) */
247     /* ---- Sets the Compare match timer start register (CMSTR) ---- */
248     CMT.CMSTR.BIT.STR0 = 1;     /* Starts channel 0 to count */
249 }
250 /* End of File */

```

4. References

- Software Manual
SH-2A/SH-2A-FPU Software Manual Rev. 3.00
(Download the latest version from the Renesas website.)
- Hardware Manual
SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
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		Page	Summary
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