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H8SX Family

Transfer of Longword Data to Odd Addresses—Software Edition

Introduction

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any address, regardless of whether it is odd or even.

In the example given in this application note, this function transfers longword data, altering the boundaries to odd addresses from even addresses, and then allocates word data or longword data to odd addresses by software processing.

Target Device

H8SX/1653F

Contents

1. Specification

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any address, regardless of whether it is odd or even.

In the example given in this application note, this function transfers longword data, altering the boundaries to odd addresses from even addresses, so that the data have been allocated to odd addresses whether they are treated as words or longwords.

1. Data are transferred from the on-chip ROM area to the on-chip RAM area by software processing.
2. Data in the on-chip ROM are allocated to even addresses as the longword boundaries, and the on-chip RAM area is set to odd addresses.
3. The amount of data to be transferred is set to a total of four longwords (16 bytes).

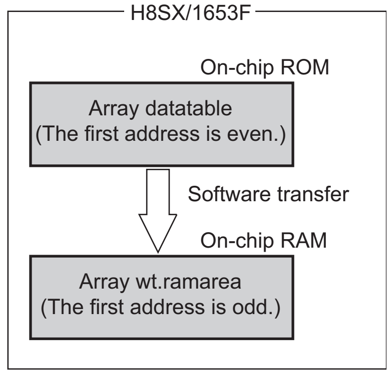


Figure 1 Software Transfer of Data Allocated to Odd Addresses

2. Applicable Conditions

Table 1 Applicable Condition

Item	Details
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Principle of Operation

3.1 Data Format in Memory

Data in memory are accessible to an H8SX CPU as words or longwords. Data thus accessed can be allocated to any addresses, regardless of whether they are odd or even. When the address of a word of data is not even or the address of a longword of data is not a multiple of four, the single access required for each unit of data must be divided into multiple access operations. For example, generation of the bus cycles for access to a longword of data starting at an odd-numbered address is divided up into byte, word, and byte. In such a case, each bus cycle is recognized as separate in terms of bus control.

Furthermore, for words and longwords of data to be handled in instruction-reading, as jump-table entries, on the stack, or as data for block-transfer or multiply-and-accumulate instructions, allocate the data from even addresses.

Ensure that access to data by SP (ER7) as an address register is in word or longword units.

3.2 Example of Data Transfer to an Odd Address

Figures 2 to 5 are schematic views of the data transfer to odd addresses. Four longwords (16 bytes) of data are transferred from H’003000 to H’FF2001. When longwords of data are transferred to odd addresses, the data are written in this order: one byte (see figure 2), one word (see figure 3), and the remaining byte (see figure 4). These steps are repeated four times so that 16 bytes of data are transferred (see figure 5).

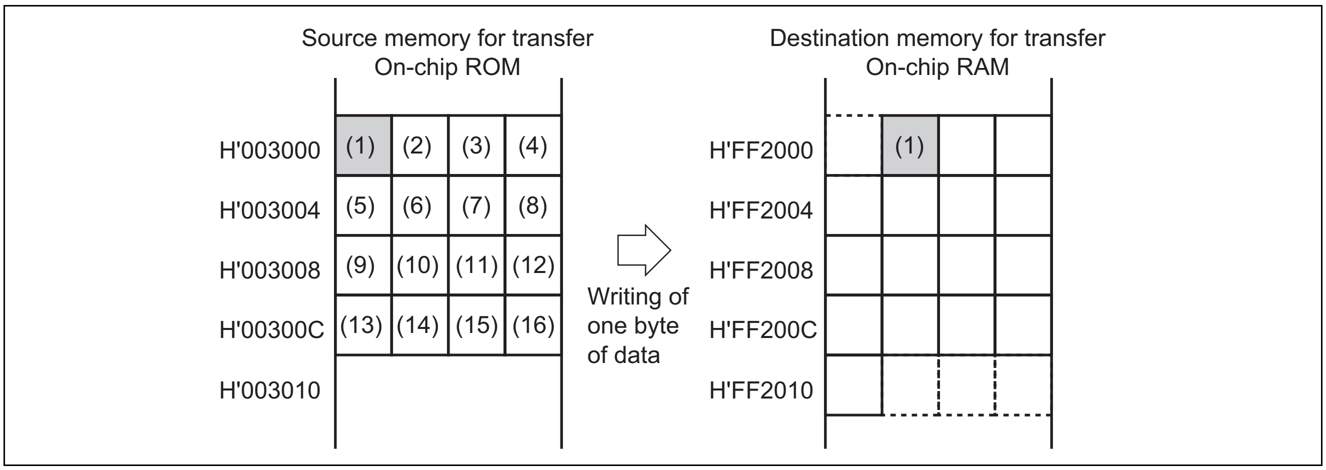


Figure 2 Example of Data Transfer to Odd Addresses, 1

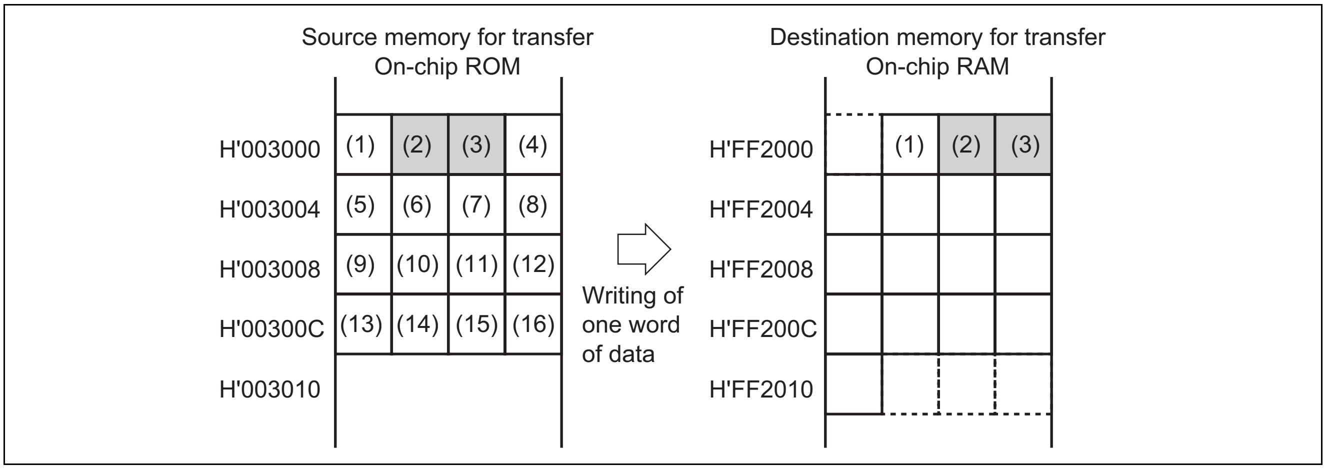


Figure 3 Example of Data Transfer to Odd Addresses, 2

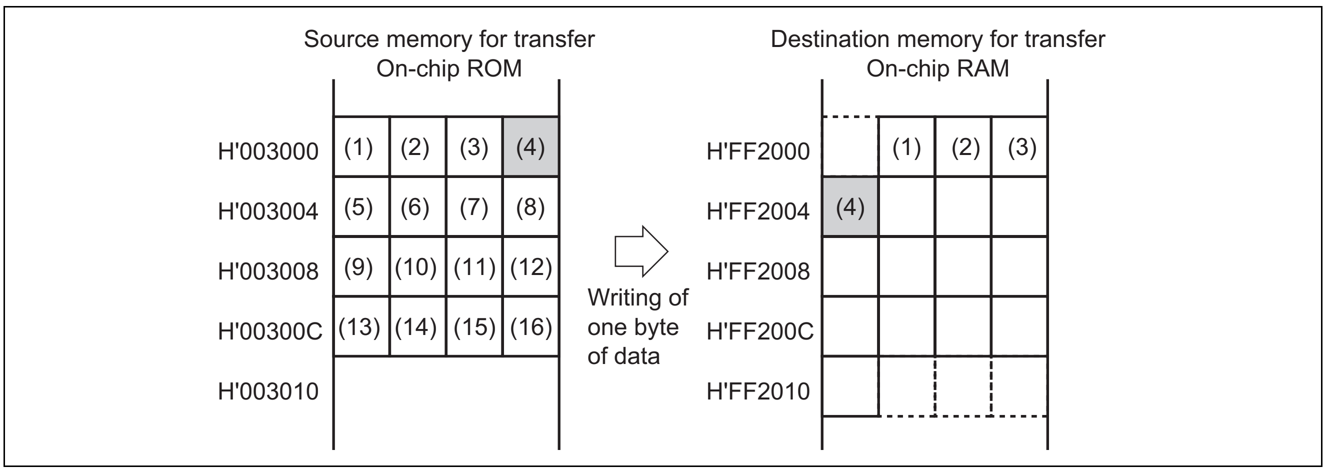


Figure 4 Example of Data Transfer to Odd Addresses, 3

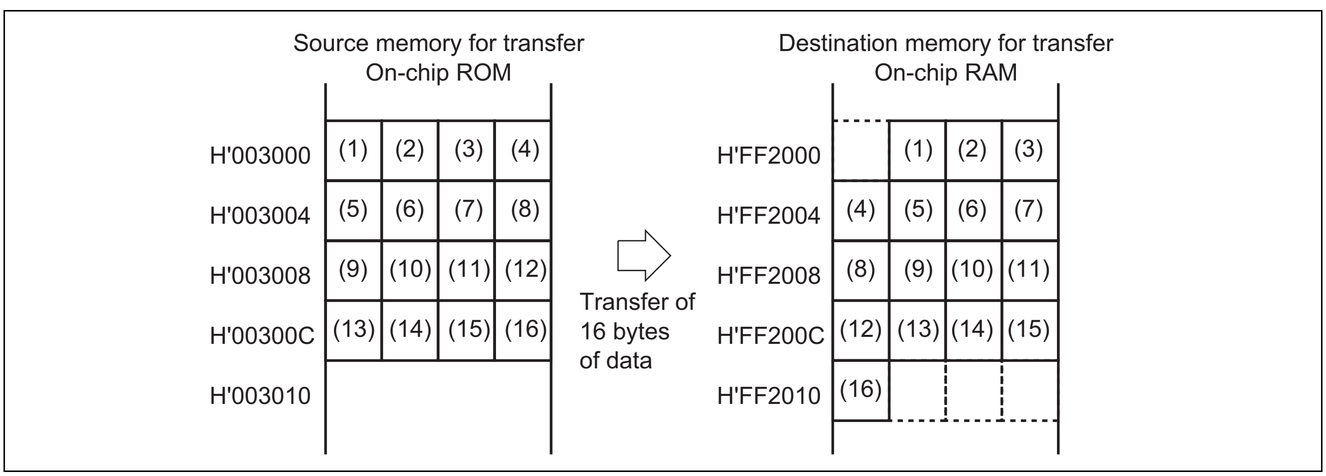


Figure 5 Example of Data Transfer to Odd Addresses, 4

4. Description of Software

4.1 Operating Environment

Table 2 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Version 4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.01 (manufactured by Renesas Technology)
H8SX compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 3 Setting of Sections

Address	Section	Description
H'001000	P	Program area
H'003000	C	Data-table storage area Array datatable is allocated here.
H'FF2000	B	Non-initialized data area (RAM area) The wt structure is allocated here.

Table 4 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	init

4.2 List of Functions

Table 5 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from module stop mode, and calls the main function.
main	Main routine Software handles the transfer of four longwords of data to odd addresses.

4.3 RAM Usage

Table 6 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	wt.dummy	wt structure This dummy variable is used to set wt.ramarea to an odd address.	main
unsigned char	wt.ramarea[16]	wt structure Transfer destination area in RAM	main

4.4 Constants

Table 7 Constants

Type	Variable Name	Settings	Description	Used in
unsigned long	datatable[4]	H'00010203, H'04050607, H'08090A0B, H'0C0D0E0F	Holds source data for transfer.	main

4.5 Description of Functions

4.5.1 init Function

1. Functional overview

Initialization routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latching is released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by pins MD3 to MD0.

Table 8 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock signal, which is provided to the CPU, DMAC, and DTC.
8	ICK0	0	R/W	000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

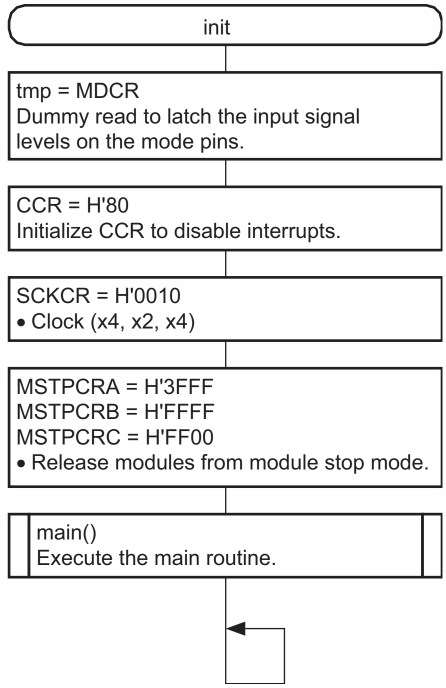
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy checker
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input signal levels on the mode pins.
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0010
• Clock (x4, x2, x4)
MSTPCRA = H'3FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release modules from module stop mode.
main()
Execute the main routine.

4.5.2 main Function

1. Functional overview

Main routine which sets up the software for transfer of 4 longwords of data to odd addresses.

2. Argument

None

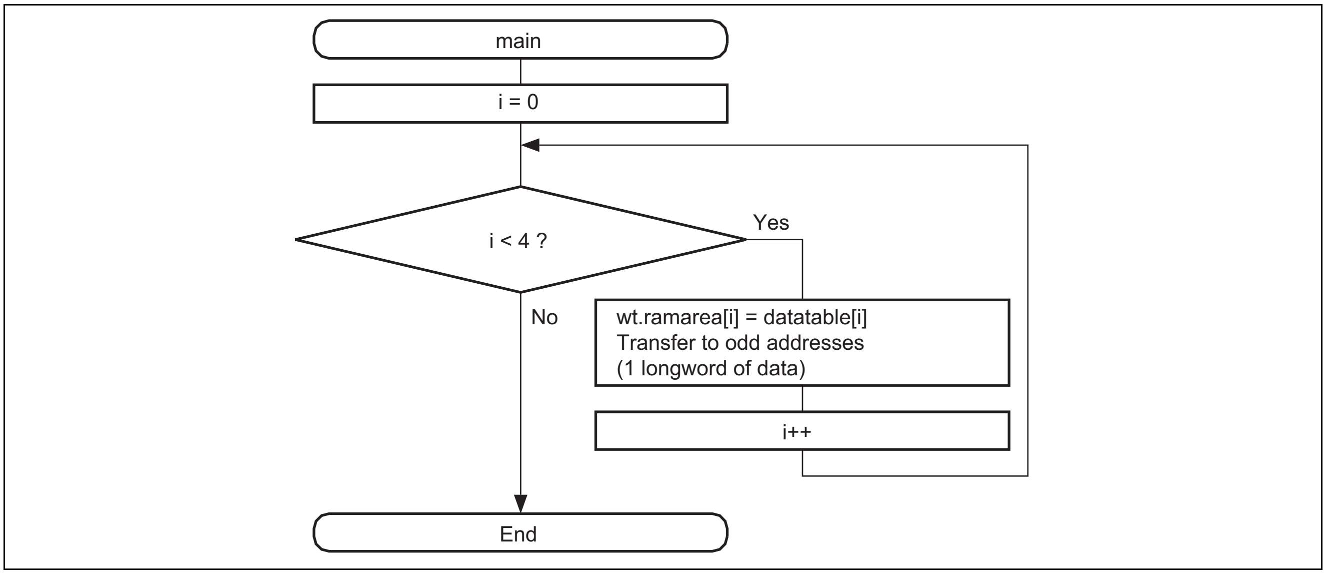
3. Return value

None

4. Description of internal registers

None

5. Flowchart



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