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# R8C/27 Group

## Timer RC in Input Caputure and Output Compare Functions

## 1. Abstract

This document describes a program for timer RC in the input capture and output compare functions.

## 2. Introduction

The application example described in this document applies to the following MCU and parameter(s):

- MCU : R8C/27 Group

This program can be used with other R8C/Tiny Series MCUs which have analogous special function registers (SFRs) as the R8C/27 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

## 3. Application Example Description

Timer RC is a 16-bit timer with four I/O pins.

Timer mode consists of two functions: Input capture and output compare. Both the input capture and output compare functions can be selected individually for each pin.

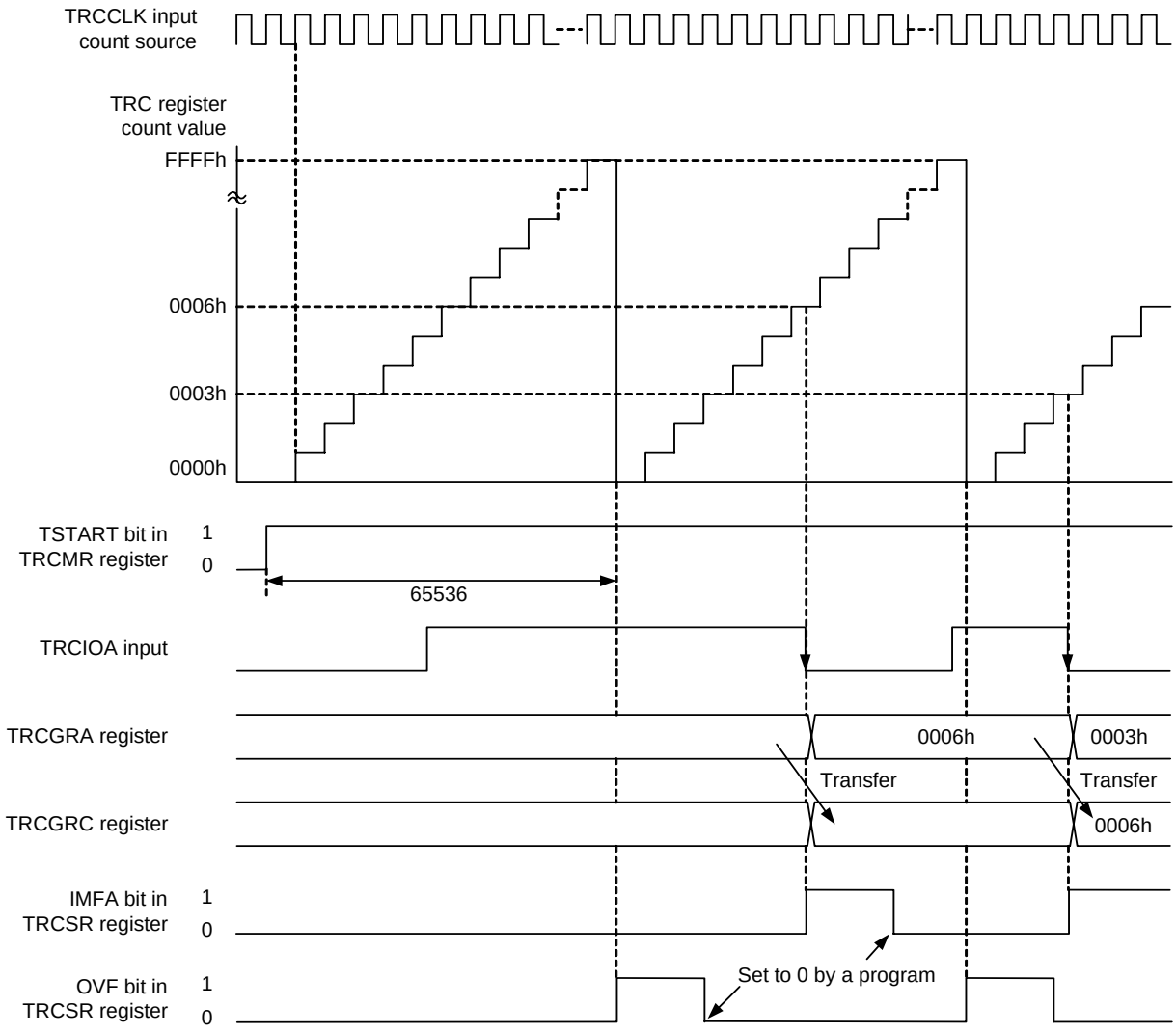
The input capture function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected individually for each pin.

The output compare function detects matches (compare match) between the content of the TRC register (counter) and the content of the TRCGRj (j = A, B, C, or D) register. When the contents match, a given level is output from the TRCIOj pin. The output compare function, or any other mode or function, can be selected individually for each pin.

The setting conditions for this program are as follows:

- Input capture input pin :TRCIOA
- Output compare output pins :TRCIOB and TRCIOD
- TRCGRC register function :Buffer register of TRCGRA register
- TRCGRD register function :General register
- Pin output enable :TRCIOB and TRCIOD pin output enabled; TRCIOA and TRCIOC pin output disabled
- Pulse output forced cutoff input :Disabled
- TRCIOB output level :Initial output “L”
- TRCIOD output level :Initial output “L”
- TRCIOA pin digital filter :Function is used; Clock is set as count source.
- Count source :f1
- TRC counter clear :Clear disabled (free-running operation)
- TRCGRA control :Input capture to TRCGRA at both edges
- TRCGRB control :“H” output at TRCGRB compare match
- TRCGRD control :“H” output at TRCGRD compare match
- Interrupt enable :Interrupt by bits IMFA and OVF enabled; Interrupt by bits IMFB and IMFD disabled
- TRCGRB compare value
  :20000 – 1 (40 MHz × f2 (FRA2) × f1 (TCK0 to TCK2) × 20000 = 1 ms
  Compare match when 1 ms elapses after the TRC count starts
- TRCGRD compare value
  :40000 – 1 (40 MHz × f2 (FRA2) × f1 (TCK0 to TCK2) × 40000 = 2 ms
  Compare match when 2 ms elapses after the TRC count starts

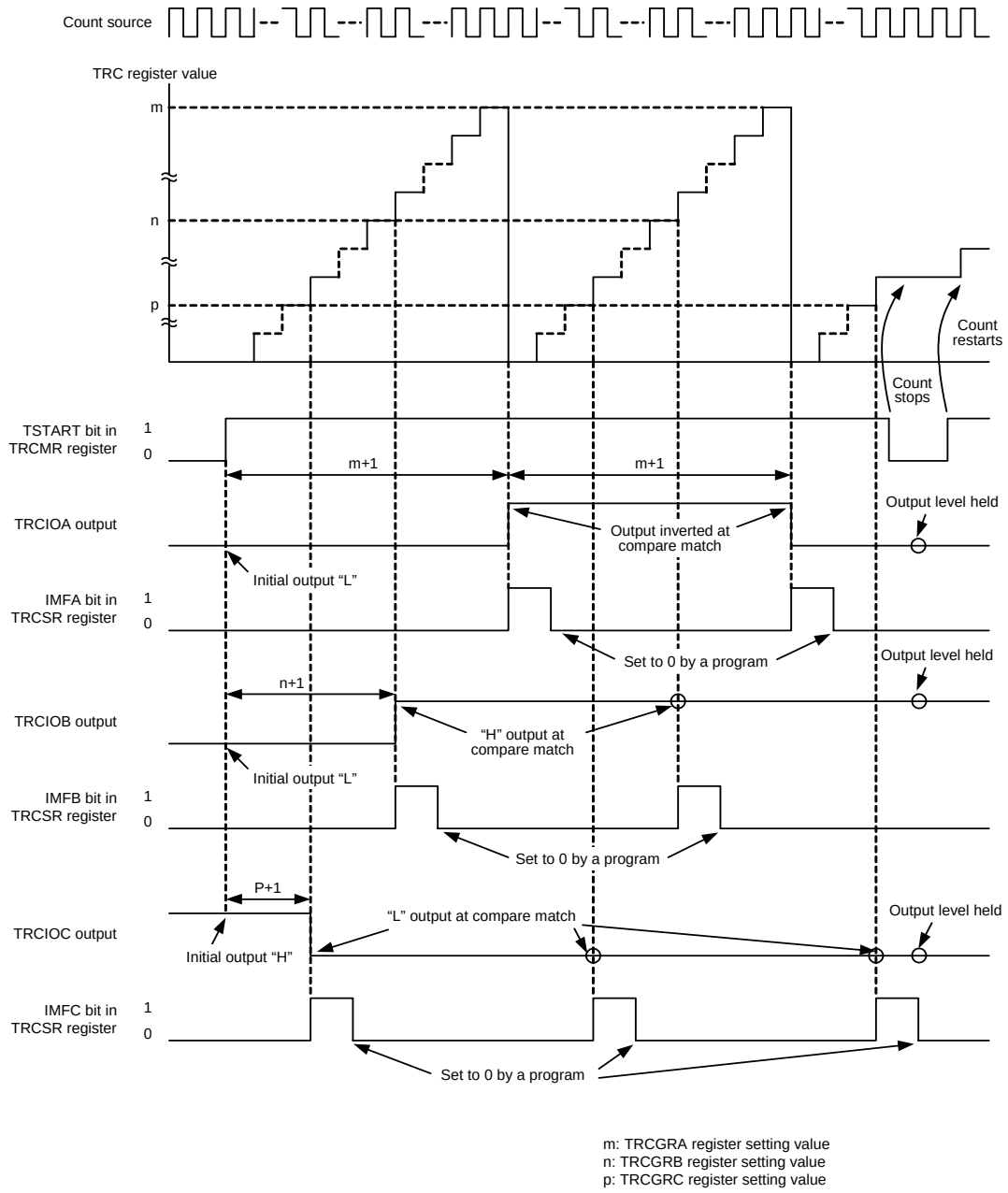
Figure 3.1 shows an Operating Example of Input Capture Function and Figure 3.2 shows an Operating Example of Output Compare Function.




The above applies under the following conditions:

- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (TRCCLK input for the count source).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as a buffer register of the TRCGRA register).

**Figure 3.1 Operating Example of Input Capture Function**




The above applies under the following conditions:

- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD do not operate buffers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (TRCIOA, TRCIOB, and TRCIOC output enabled).
- The CCLR bit in the TRCCR1 register is set to 0 (the TRC register is set to 0000h at the TRCGRA compare match).
- In the TRCCR1 register, bits TOA and TOB are set to 0 ("L" initial output until compare match) and the TOC bit is set to 1 ("H" initial output until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b ("H" TRCIOB output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b ("L" TRCIOC output at TRCGRC compare match).

**Figure 3.2 Operating Example of Output Compare Function**

This sample program may include bit operations of unused functions for the SFR bit layout. Set these values according to the operating conditions of the user system.

## 3.1 Pins Used

**Table 3.1 Pins Used and Their Function**

| Pin Name | I/O | Function |
|---|---|---|
| P1_1/$\overline{KI1}$/AN9/TRCIOA/TRCCLK | Input | Input capture input pin |
| P1_2/$\overline{KI2}$/AN10/TRCIOB | Output | Output compare output pin |
| P5_4/TRCIOD | Output | Output compare output pin |

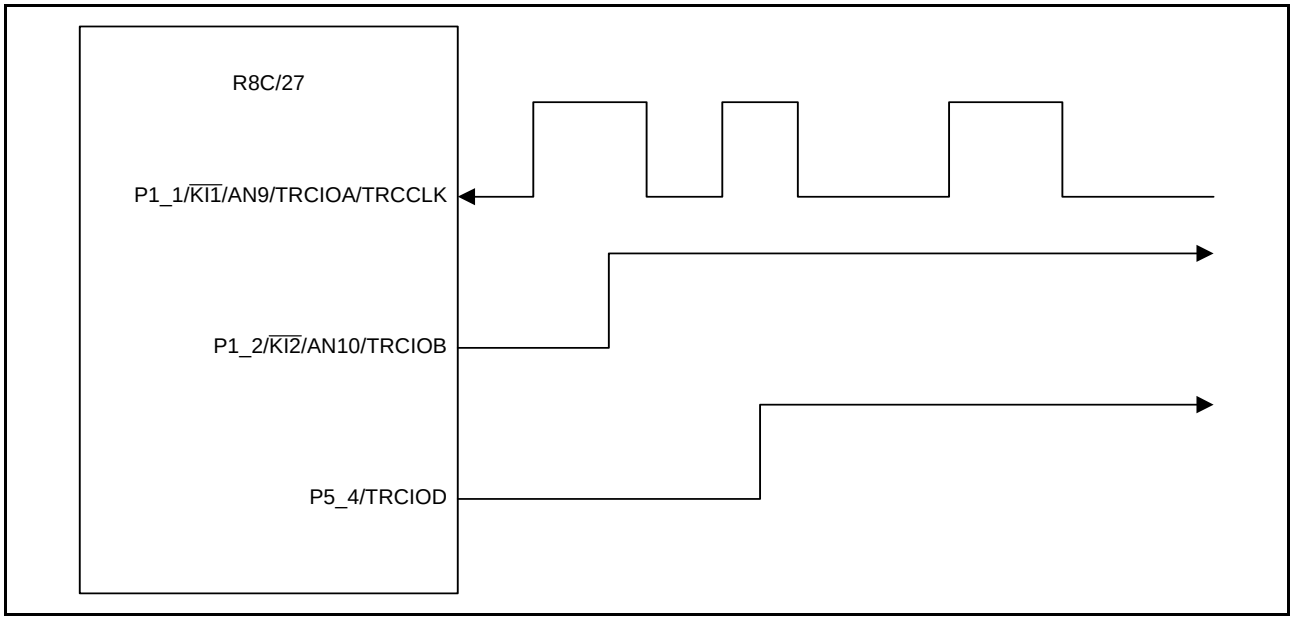



**Figure 3.3 Pins Used**

## 3.2 Memory Usage

**Table 3.2 Memory Usage**

| Memory Usage | Size | Remarks |
|---|---|---|
| ROM | 273 bytes | In main.c module |
| RAM | 11 bytes | In main.c module |
| Maximum user stack usage | 10 bytes | main function: 7 bytes<br>timer_rc_init function: 3 bytes |
| Maximum interrupt stack usage | 18 bytes | TRC_int function: 18 bytes |

Memory usage varies depending on the C compiler version and the compile option.
The above applies under the following conditions:

- C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.40 Release 00
- Compile option: -c -finfo; NOTE: -dir “$(CONFIGDIR)” -R8C

NOTE: Unavailable in the R8C/Tiny-exclusive free version.

# 4. Setup

This section shows the initial setting procedures and values to perform the example described in **3. Application Example Description**. Refer to the **R8C/27 Group Hardware Manual** for details on individual registers.

## 4.1 System Clock Setting

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | 1 |

PRCR [Address 000Ah]

PRC0 Protect bit 0

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 enabled

(2) Start the low-speed on-chip oscilltor.

System Clock Control Register 1

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | | | 0 | | | | |

CM1 [Address 0007h]

CM14 Low-speed on-chip oscillator oscillation stop bit

Low-speed on-chip oscillator oscillates

(3) Set the division ratio of the high-speed on-chip oscillator clock.

High-Speed On-Chip Oscillator Control Register 2

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FRA2 [Address 0025h]

FRA22 to FRA20 High-speed on-chip oscillator frequency switch bits

Divide-by-2 mode

($\overline{b7\text{-}b3}$) Reserved bits

Set to 0.

(4) Start the high-speed on-chip oscilltor.

High-Speed On-Chip Oscillator Control Register 0

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | 1 |

FRA0 [Address 0023h]

FRA00 High-speed on-chip oscillator enable bit

High-speed on-chip oscillator oscillates

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | 1 | |

FRA0 [Address 0023h]

FRA01 High-speed on-chip oscillator select bit

High-speed on-chip oscillator selected

(7) Set system clock division select bits 1.

System Clock Control Register 1

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | | | | | | |

CM1 [Address 0007h]

CM17 and CM16 System clock division select bits 1

No division mode

(8) Set system clock division select bit 0.

System Clock Control Register 0

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | 0 | | | | | | |

CM0 [Address 0006h]

CM06 System clock division select bit 0

CM16 and CM17 enabled

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | 0 |

PRCR [Address 000Ah]

PRC0 Protect bit 0

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 disabled

## 4.2 Timer Mode (Input Capture and Output Compare Functions) Setting

(1) Set the port P1 direction register.

Port P1 Direction Register

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | 0 | |

PD1 [Address 00E3h]

PD1_1 Port P1_1 direction bit
Input mode

(2) Set pin select register 3.

Pin Select Register 3

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |

PINSR3 [Address 00F7h]

($\overline{b2}$-$\overline{b0}$) Reserved bits
Set to 1.

TRCIOCSEL TRCIOC select bit
P5_3

TRCIODSEL TRCIOD select bit
P5_4

($\overline{b5}$) Reserved bit
Set to 1.

($\overline{b7}$-$\overline{b6}$) Nothing is assigned.
Set to 0.

(3) Stop the TRC count.

Timer RC Mode Register

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | | | | | | | |

TRCMR [Address 0120h]

TSTART TRC count start bit
Count stops

(4) Set the timer RC interrupt control register (interrupt disabled).

Timer RC Interrupt Control Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TRCIC [Address 0047h]

| | |
|---|---|
| ILVL2 to ILVL0 | Interrupt priority level select bits 2 to 0<br>Level 0 (interrupt disabled) |
| IR | Interrupt request bit<br>No interrupt request |
| ($\overline{b7}$-$\overline{b4}$) | Nothing is assigned.<br>Set to 0. |

(5) Set the timer RC mode register.

Timer RC Mode Register

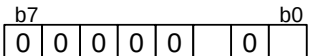
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

TRCMR [Address 0120h]

| | |
|---|---|
| PWMB | TRCIOB PWM mode select bit<br>Timer mode |
| PWMC | TRCIOC PWM mode select bit<br>Timer mode |
| PWMD | TRCIOD PWM mode select bit<br>Timer mode |
| PWM2 | PWM2 mode select bit<br>Timer mode |
| BFC | TRCGRC register function select bit<br>Buffer register of TRCGRA register |
| BFD | TRCGRD register function select bit<br>General register |
| ($\overline{b6}$) | Nothing is assigned.<br>Set to 0. |
| TSTART | TRC count start bit<br>Count stops |

(6) Set timer RC control register 1.

Timer RC Control Register 1

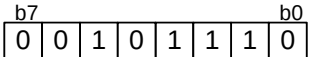



TRCCR1 [Address 0121h]

| | |
|---|---|
| TOA | TRCIOA output level select bit<br>Unavailable. |
| TOB | TRCIOB output level select bit<br>Initial output “L” |
| TOC | TRCIOC output level select bit<br>Unavailable. |
| TOD | TRCIOD output level select bit<br>Initial output “L” |
| TCK2 to TCK0 | Count source select bits<br>f1 selected |
| CCLR | TRD0 counter clear select bit<br>Clear disabled (free-running operation) |

(7) Set timer RC I/O control register 0.

Timer RC I/O Control Register 0

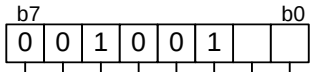



TRCIOR0 [Address 0124h]

| | |
|---|---|
| IOA1 and IOA0 | TRCGRA control bits<br>Input capture to TRCGRA at both edges |
| IOA2 | TRCGRA mode select bit<br>Set to 1 in the input capture function. |
| ($\overline{b3}$) | Reserved bit<br>Set to 1. |
| IOB1 and IOB0 | TRCGRB control bits<br>“H” output at TRCGRB compare match |
| IOB2 | TRCGRB mode select bit<br>Set to 0 in the output compare function. |
| ($\overline{b7}$) | Nothing is assigned.<br>Set to 0. |

(8) Set timer RC I/O control register 1.

Timer RC I/O Control Register 1

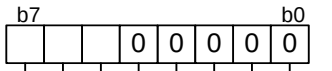



TRCIOR1 [Address 0125h]

| | |
|---|---|
| IOC1 and IOC0 | TRCGRC control bits<br>Unavailable. |
| IOC2 | TRCGRC mode select bit<br>To select 1 (buffer register of TRCGRA register) by the BFC bit in the TRCMR register, set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register. |
| ($\overline{b3}$) | Nothing is assigned.<br>Set to 0. |
| IOD1 and IOD0 | TRCGRD control bits<br>"H" output at TRCGRD compare match |
| IOD2 | TRCGRD mode select bit<br>Set to 0 in the output compare function. |
| ($\overline{b7}$) | Nothing is assigned.<br>Set to 0. |

(9) Set timer RC control register 2.

Timer RC Control Register 2




TRCCR2 [Address 0130h]

| | |
|---|---|
| ($\overline{b4}$-$\overline{b0}$) | Nothing is assigned.<br>Set to 0. |
| CSEL | TRC count operation select bit<br>This bit is disabled in timer mode. |
| TCEG1 and TECG0 | TRCTRG input edge select bits<br>These bits are disabled in timer mode. |

(10) Set the timer RC digital filter function select register.

Timer RC Digital Filter Function Select Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | TRCDF [Address 0131h] |

| | | |
|---|---|---|
| DFA | TRCIOA pin digital filter function select bit | |
| | 1 | Function used |
| DFB | TRCIOB pin digital filter function select bit | |
| | 1 | Function not used |
| DFC | TRCIOC pin digital filter function select bit | |
| | 1 | Function not used |
| DFD | TRCIOD pin digital filter function select bit | |
| | 1 | Function not used |
| DFTRG | TRCTRG pin digital filter function select bit | |
| | 1 | Function not used |
| ($\overline{b5}$) | Nothing is assigned. | |
| | 0 | Set to 0. |
| DFCK1 and DFCK0 | Digital filter function clock select bits | |
| | 0 0 | Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register) |

(11) Set the timer RC output master enable register.

Timer RC Output Master Enable Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | TRCOER [Address 0132h] |

| | | |
|---|---|---|
| EA | TRCIOA output disable bit | |
| | 1 | This bit is disabled for use as input capture input |
| EB | TRCIOB output disable bit | |
| | 0 | Output enabled |
| EC | TRCIOC output disable bit | |
| | 1 | Output disabled (The TRCIOC pin is used as a programmable I/O port.) |
| ED | TRCIOD output disable bit | |
| | 0 | Output enabled |
| ($\overline{b6\text{-}b4}$) | Nothing is assigned. | |
| | 0 | Set to 0. |
| PTO | Pulse output forced cutoff signal input $\overline{INT0}$ enable bit | |
| | 0 | Pulse output forced cutoff input disabled |

(12) Set the timer RC counter.

Timer RC Counter

| (b15) b7 | | | | | | | | (b8) b0 | b7 | | | | | | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TRC [Address 0127h to 0126h]

Initialization

0 (0x0000) setting

(13) Set timer RC general register A.

Timer RC General Register A

| (b15) b7 | | | | | | | | (b8) b0 | b7 | | | | | | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

TRCGRA [Address 0129h to 0128h]

Initialization

0xFFFF setting

(14) Set timer RC general register B.

Timer RC General Register B

| (b15) b7 | | | | | | | | (b8) b0 | b7 | | | | | | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

TRCGRB [Address 012Bh to 012Ah]

The compare value with the TRC register (counter) is stored

20000 – 1 (0x4E1F) setting

(15) Set timer RC general register C.

Timer RC General Register C

| (b15) b7 | | | | | | | | (b8) b0 | b7 | | | | | | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

TRCGRC [Address 012Dh to 012Ch]

Initialization

0xFFFF setting

(16) Set timer RC general register D.

Timer RC General Register D

| (b15) b7 | | | | | | | (b8) b0 | b7 | | | | | | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

TRCGRD [Address 012Fh to 012Eh]

The compare value with the TRC register (counter) is stored

40000 – 1 (0x9C3F) setting

(17) Set the timer RC interrupt enable register.

Timer RC Interrupt Enable Register

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

TRCIER [Address 0122h]

| | |
|---|---|
| IMIEA | Input capture/compare match interrupt enable bit A<br>Interrupt (IMIA) by IMFA bit enabled |
| IMIEB | Input capture/compare match interrupt enable bit B<br>Interrupt (IMIB) by IMFB bit disabled |
| IMIEC | Input capture/compare match interrupt enable bit C<br>Interrupt (IMIC) by IMFC bit disabled |
| IMIED | Input capture/compare match interrupt enable bit D<br>Interrupt (IMID) by IMFD bit disabled |
| ($\overline{\text{b6-b4}}$) | Nothing is assigned.<br>Set to 0. |
| OVIE | Overflow interrupt enable bit<br>Interrupt (OVI) by OVF bit enabled |

(18) Set the timer RC status register.

Timer RC Status Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TRCSR | [Address 0123h] |
| | | | | | | | | IMFA | Input capture/compare match flag A<br>Set to 0. |
| | | | | | | | | IMFB | Input capture/compare match flag B<br>Set to 0. |
| | | | | | | | | IMFC | Input capture/compare match flag C<br>Set to 0. |
| | | | | | | | | IMFD | Input capture/compare match flag D<br>Set to 0. |
| | | | | | | | | ($\overline{b6\text{-}b4}$) | Nothing is assigned.<br>Set to 0. |
| | | | | | | | | OVF | Overflow flag<br>Set to 0. |

(19) Set the timer RC interrupt control register.

Timer RC Interrupt Control Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | TRCIC | [Address 0047h] |
| | | | | | | | | ILVL2 to ILVL0 | Interrupt priority level select bits 2 to 0<br>Level 7 |
| | | | | | | | | IR | Interrupt request bit<br>No interrupt request |
| | | | | | | | | ($\overline{b7\text{-}b4}$) | Nothing is assigned.<br>Set to 0. |

(20) Start the TRC count.

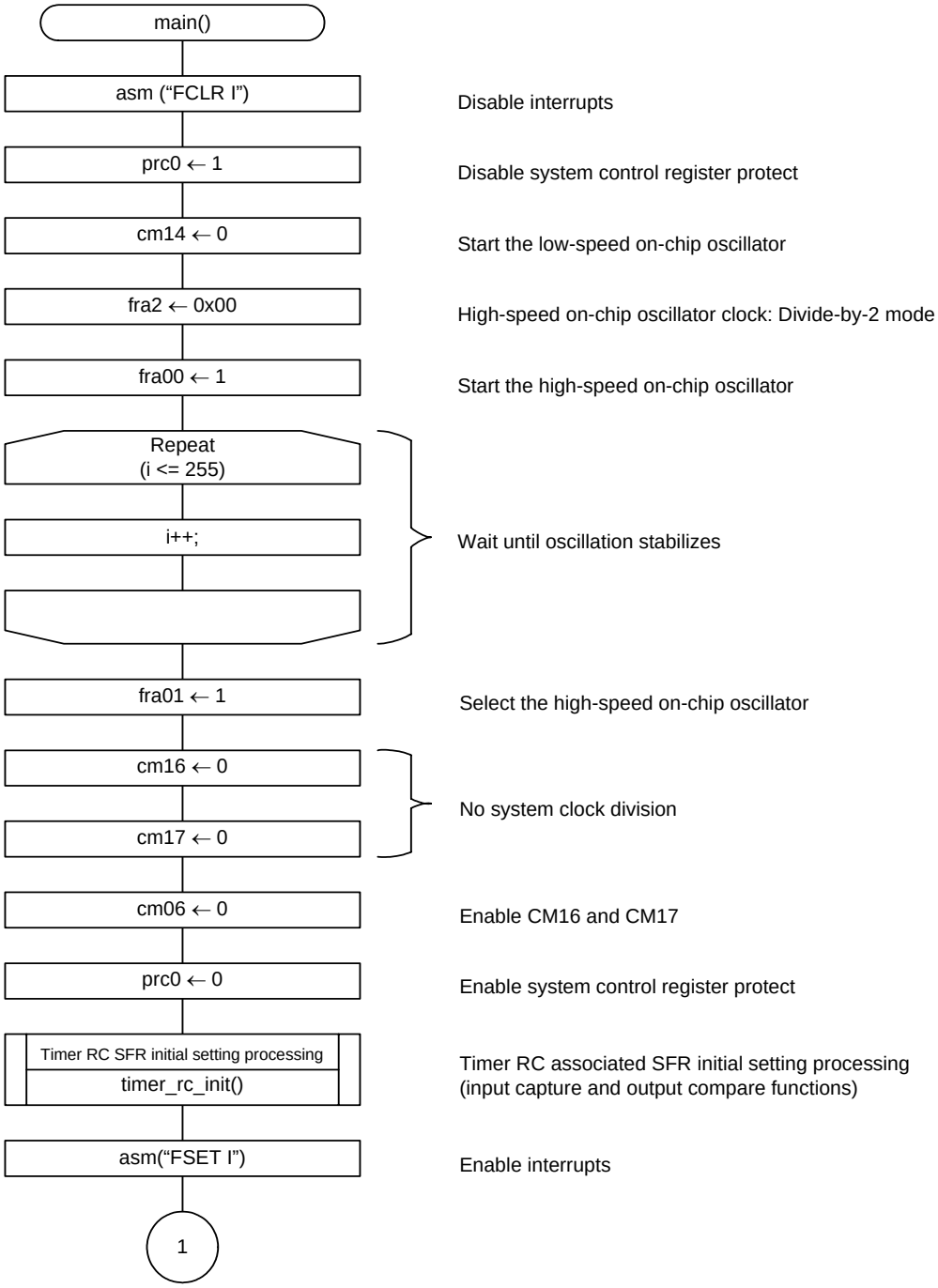
Timer RC Mode Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | | | | | | | | TRCMR | [Address 0120h] |
| | | | | | | | | TSTART | TRC count start bit<br>Count starts |

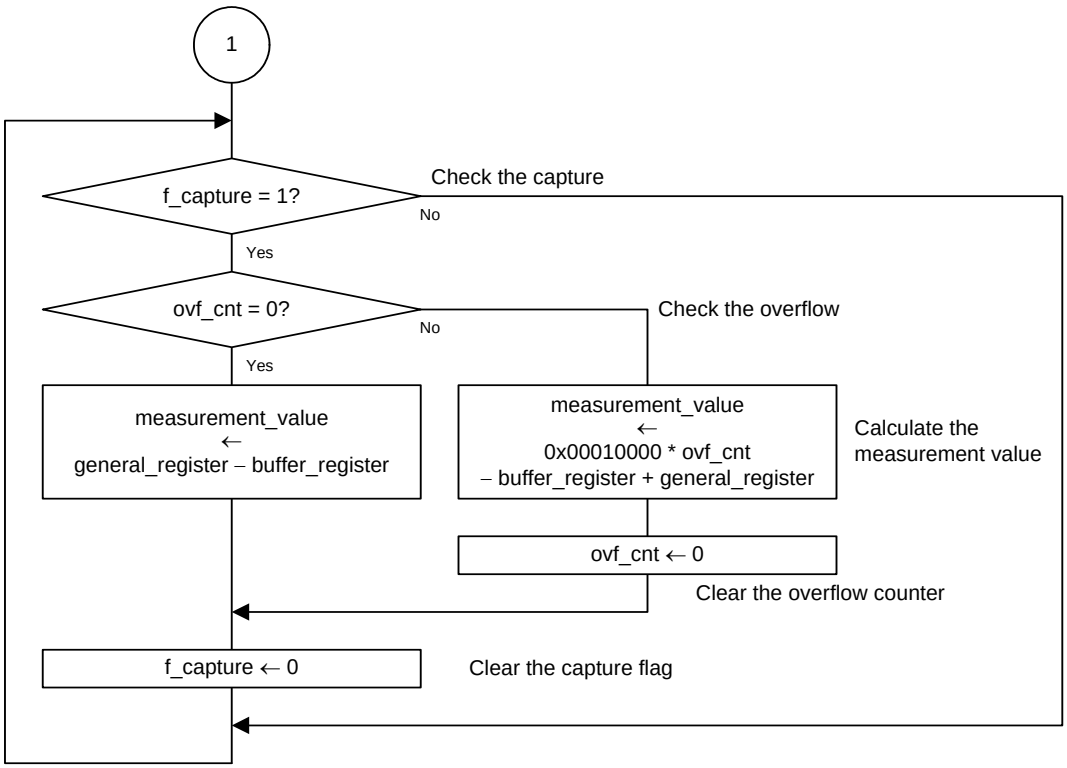
# 5. Flowchart

## 5.1 Main Function

### 5.1.1 Main Function 1

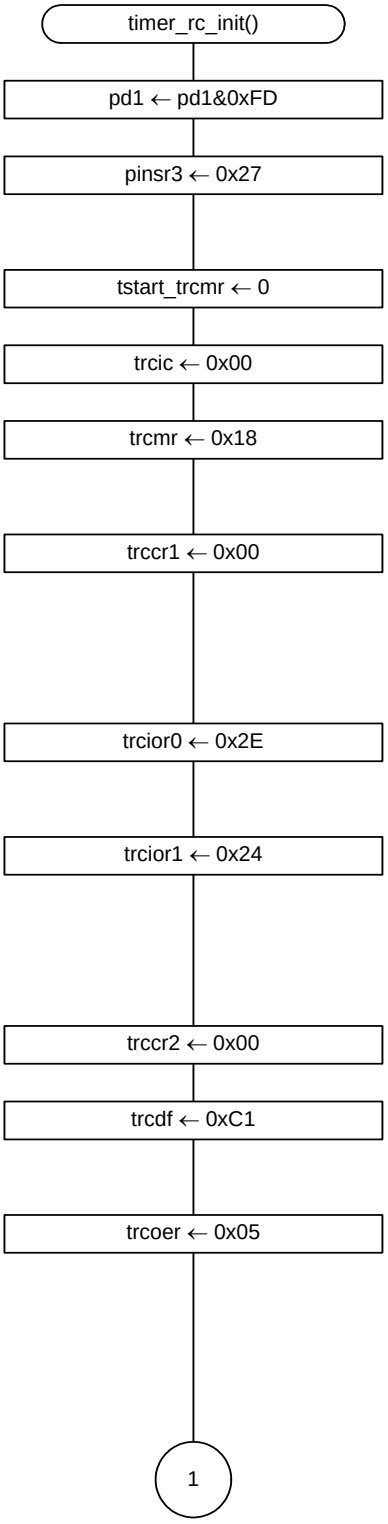


### 5.1.2 Main Function 2



## 5.2 Timer RC Associated SFR Initial Setting Processing

### 5.2.1 Timer RC Associated SFR Initial Setting Processing 1




P1_1 (TRCIOA) pin: Set to an input port

TRCIOC pin: P5_3
TRCIOD pin: P5_4

Stop the TRC count

TRC interrupt: Interrupt level 0 (interrupt disabled)

Operate the TRCGRC register as a buffer register of the TRCGRA register
Operate the TRCGRD register as a general register

TRCIOB pin: Initial output “L”
TRCIOD pin: Initial output “L”
Count source: Select f1
TRC counter: Disable clear (free-running operation)

TRCIOA input: Input capture to TRCGRA at both edges
Output “H” at the TRCGRB compare match

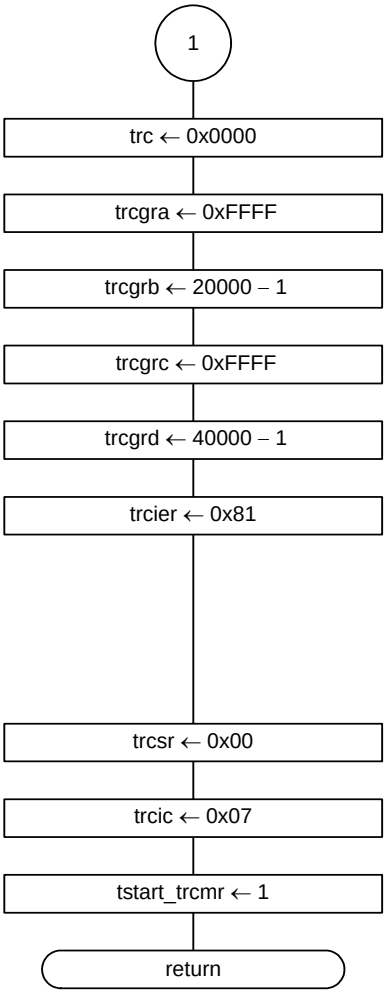
To select 1 (buffer register of TRCGRA register) by the BFC bit in the TRCMR register, set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
Output “H” at the TRCGRD compare match

Initialization

TRCIOA pin: Digital filter function used
Digital filter function clock: Select the count source

TRCIOA pin: Disable output
TRCIOB pin: Enable output
TRCIOC pin: Disable output
TRCIOD pin: Enable output
Disable the pulse output forced cutoff input

### 5.2.2 Timer RC Associated SER Initial Setting Processing 2




Initialize the TRC register count value to 0x0000.

Initialize the TRCGRA register count value to 0xFFFF.

Count period: Set to 1 ms (25 ns × f2 (FRA2) × f1 (TCK0 to TCK2) × 20000 = 1 ms)

Initialize the TRCGRC register count value to 0xFFFF.

Count period: Set to 2 ms (25 ns × f2 (FRA2) × f1 (TCK0 to TCK2) × 40000 = 2 ms)

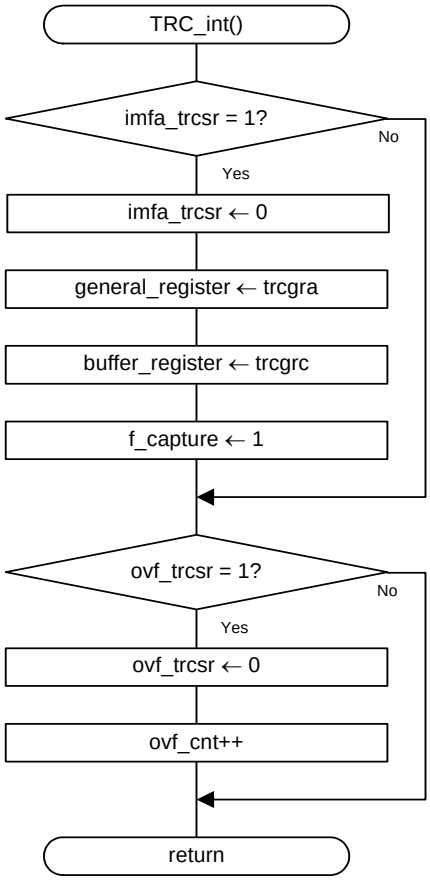
Enable interrupt (IMIA) by the IMFA bit
Disable interrupt (IMIB) by the IMFB bit
Disable interrupt (IMIC) by the IMFC bit
Disable interrupt (IMID) by the IMFD bit
Enable interrupt (OVI) by the OVF bit

Initialize the timer RC status flag

TRC interrupt: Interrupt priority level 7

Start the TRC count

## 5.3 Timer RC Interrupt Handling




Any input capture signal to the TRCIOA pin detected?

Clear input capture flag A

Read the TRCGRA register

Read the TRCGRC register

Set the capture flag

Overflow?

Clear the overflow flag

Increment the overflow counter

## 6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Series page.

## 7. Reference Documents

Hardware Manual
R8C/27 Group Hardware Manual
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

## Website and Support

Renesas Technology website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

| REVISION HISTORY | R8C/27 Group<br>Timer RC in Input Caputure and Output Compare Functions |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | June 29, 2007 | – | First Edition issued |

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