R32C/100 Series

Timer A Operation in Timer Mode Using the Pulse Output Function

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1. Abstract

This document describes the setting procedure and operation example for timer A in timer mode using the pulse output function.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):
MCU: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/111 Group. Check the user's manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

In timer mode, the timer counts an internally generated count source. The timer decrements until it underflows. Subsequently, the timer then generates an interrupt request.
This document also describes setting the peripheral clock source to 25 MHz, how to generate a timer interrupt request of timer A with a 1 ms period using the peripheral count source f8, and how to output a 1 kHz rectangular wave generated at TAiOUT pin from a port (i = 0 to 4).
Table 3.1 lists the Maximum Period of Timer A Interrupt Request Per Count Source.

Timer A Interrupt Request Period = (timer register value + 1) × Timer Count Source Period

Table 3.1 Maximum Period of Timer A Interrupt Request Per Count Source

Count Source	Count Source Period	Maximum Period of Timer A Interrupt Request
f1	40 ns	2.621 ms
f8	320 ns	20.972 ms
f2n (n = 15)	1200 ns (1)	78.64 ms (1)
fC32	Approx. 0.977 ms	64 s

Xin (main clock) = 16 MHz, PLL clock = 100 MHz, f1 = 25 MHz, fC = 32.768 kHz
Note:
1. Value when selecting the peripheral count source as the f2n clock source.

When outputting the timer Ai pulse from the TAiOUT pin, set the corresponding direction bit of the pin to 1 (output) and TAiOUT output to function registers PSEL2 to PSEL0.
Table 3.2 lists the Port Assigned to TAiOUT Pin and Related Output Register.

Table 3.2 Port Assigned to TAiOUT Pin and Related Output Register

Timer Pin	Port	Port Direction Register	Function Select Register	Setting Value
TA0OUT	P3_0	PD3_0	P3_0S	01h
	P7_0 (1)	PD7_0	P7_0S	01h
TA1OUT	P3_2	PD3_2	P3_2S	01h
	P7_2	PD7_2	P7_2S	01h
TA2OUT	P3_4	PD3_4	P3_4S	01h
	P7_4	PD7_4	P7_4S	01h
TA3OUT	P3_1	PD3_1	P3_1S	01h
	P7_6	PD7_6	P7_6S	01h
TA4OUT	P3_6	PD3_6	P3_6S	01h
	P8_0	PD8_0	P8_0S	01h

Note:
1. This port is N-channel open drain output.

3.1 Timer Mode Operation

The following describes timer mode operation of timer A.

(1) While the timer counter is stopped, the value written to the timer Ai register is written to both the reload register and the counter (i = 0 to 4).
(2) After setting the TAiS bit in the TABSR register to 1 (count started), the counter decrements the count source.
(3) When the counter underflows, the value from the reload register is reloaded, and the count continues. At the same time, the IR bit in the TAiIC register becomes 1 (interrupt requested), and the TAiOUT pin is inverted.
(4) After setting the TAiS bit to 0 (count stopped), the counter holds the count value and stops. At this time, the TAiOUT pin outputs a low signal.
(5) The IR bit in the TAiIC register becomes 0 by accepting an interrupt request, or setting it to 0 by a program.

Figure 3.1 shows the operation timing, Figure 3.2 shows the Flowchart of main Process, and Figure 3.3 shows the Process Flowchart of Initial Timer A0 Setting.

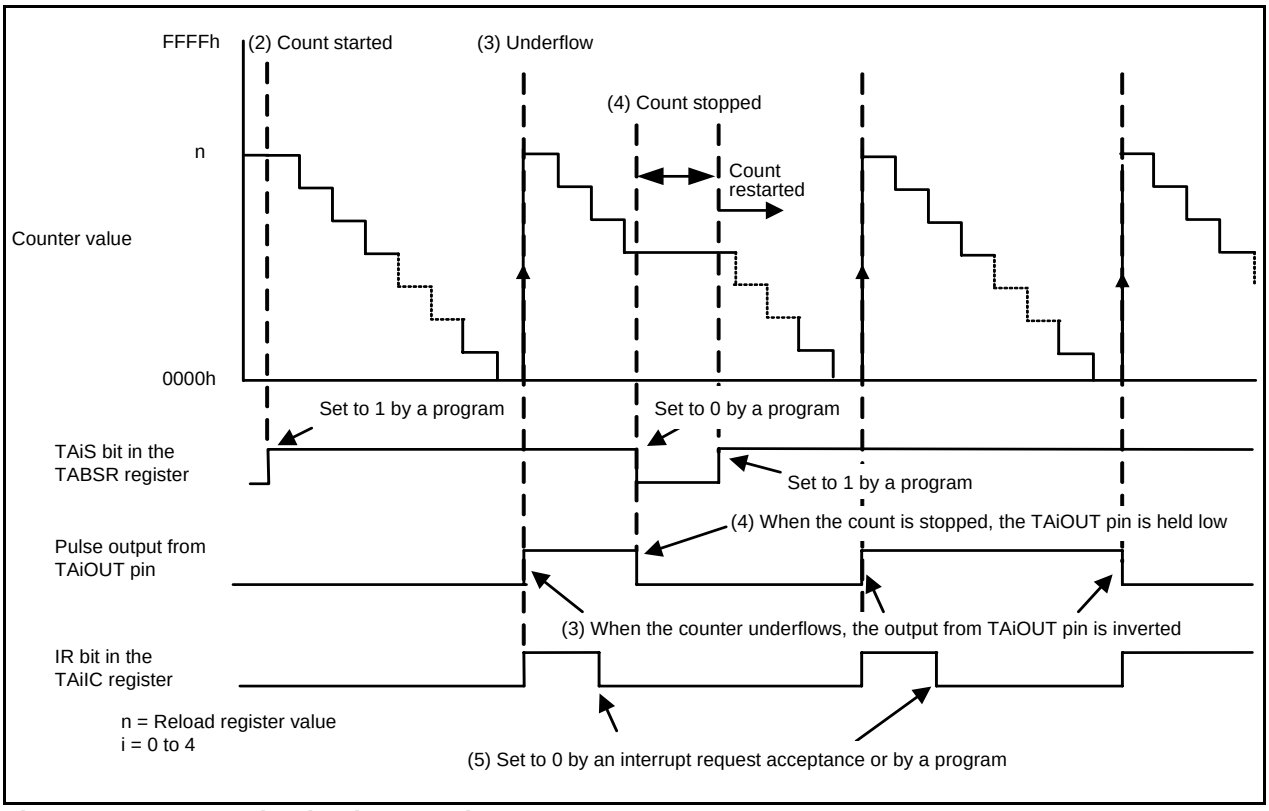


Figure 3.1 Operation in Timer Mode

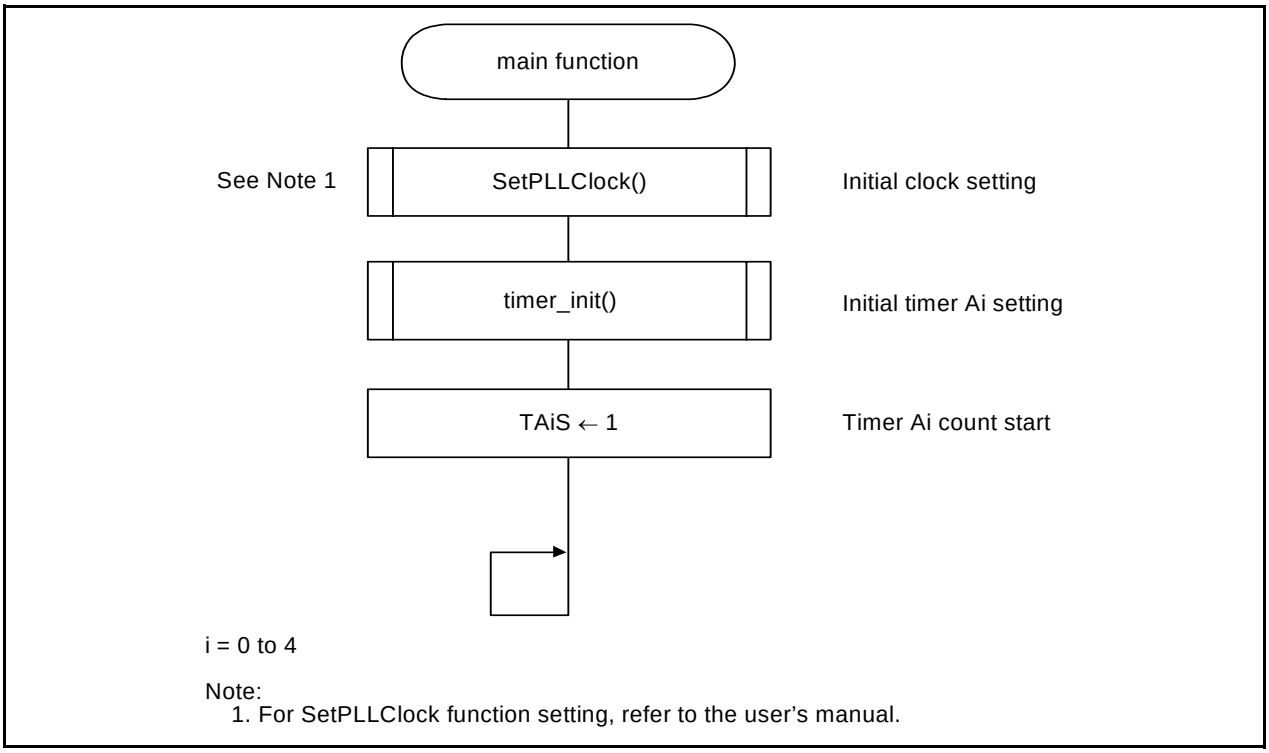


Figure 3.2 Flowchart of main Process

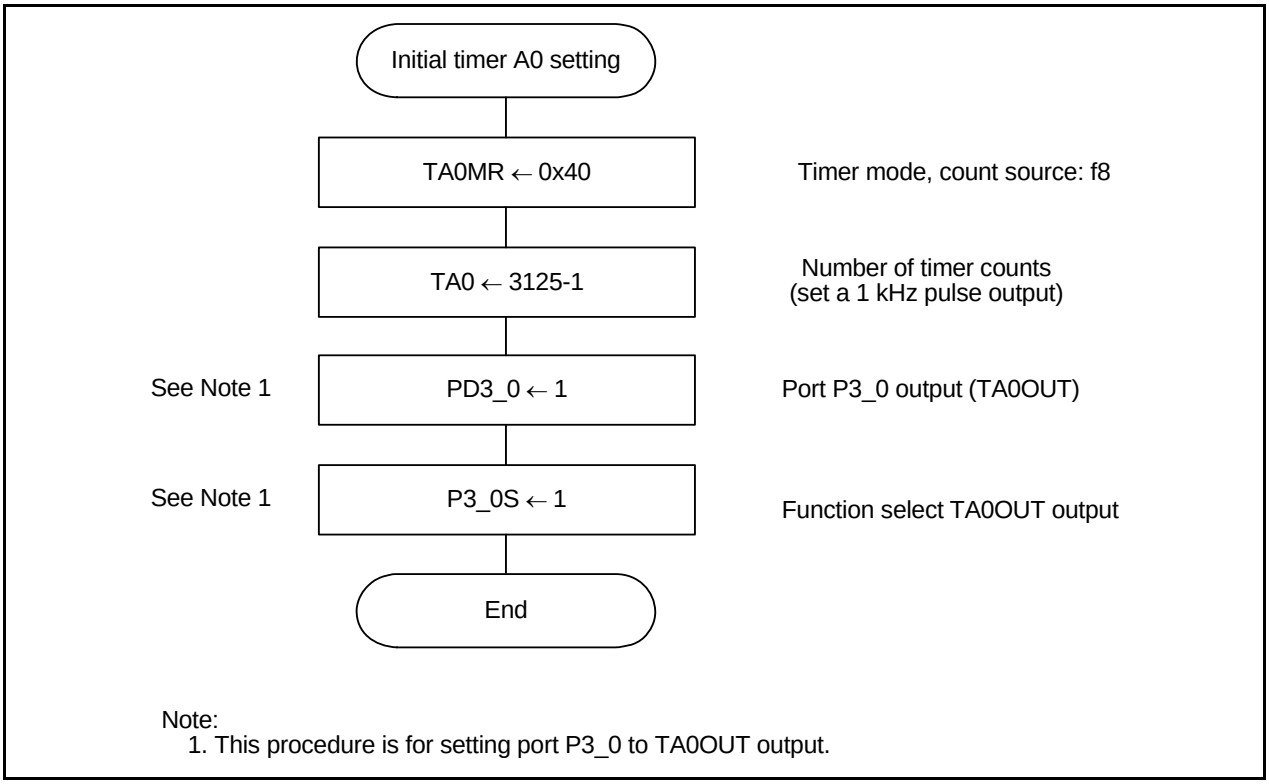
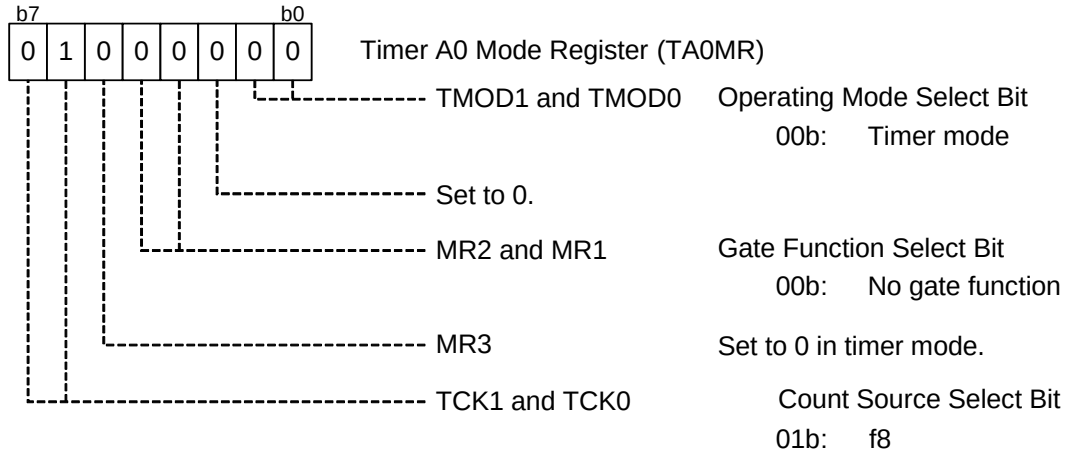


Figure 3.3 Process Flowchart of Initial Timer A0 Setting

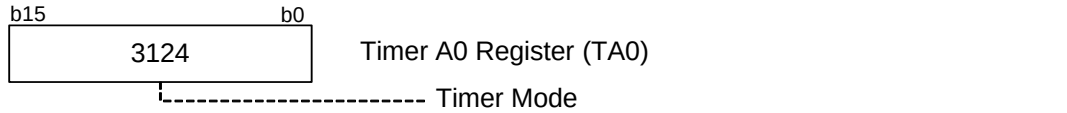
3.2 Settings

This section shows the setting procedures and values to set the example shown in section 3.1 “Timer Mode Operation”. Refer to the user’s manual for details on individual registers.

Set the timer A0 mode register.

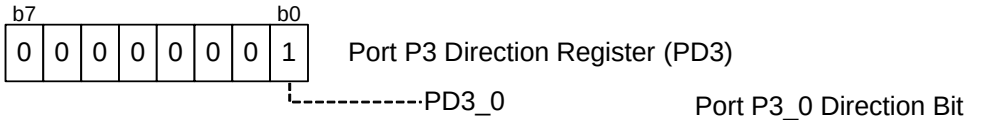


Set the timer A0 register.



A 16-bit read/write access to this register should be performed.

Set the port P3 direction register.



When setting port P3_0 to TA0OUT output, set the port P3_0 direction bit to 1.

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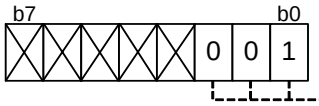
Set the function select register.

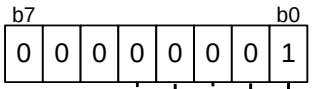


Port P3_0 Function Select Register (P3_0S)

PSEL2 to PSEL0 — Port P3_0 Output Function Select Bit
001b: Timer output

When setting port P3_0 to pulse output using timer A0 timer mode, set the port P3_0 output function select bit in the port P3_0 function select register to 001b (TA0OUT output).

Set the count start register.



Count Start Register (TABSR)

TA0S — Timer A0 Count Start Bit
1: Start counter

TA1S — Timer A1 Count Start Bit

TA2S — Timer A2 Count Start Bit

TA3S — Timer A3 Count Start Bit

TA4S — Timer A4 Count Start Bit

4. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5. Reference Documents

User's Manual
R32C/111 Group User's Manual Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C compiler manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R32C/100 Series Timer A Operation in Timer Mode Using the Pulse Output Function

Rev.	Date	Description	
		Page	Summary
1.00	June 4, 2010	-	First Edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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