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Renesas Electronics Corporation

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APPLICATION NOTE

Synchronous Operation Mode

Introduction

Applies the synchronous operation mode of the H8/3687's timer Z block to output PWM waveforms.

Target Device

H8/300H Tiny Series H8/3687

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1. Specifications

1. Applies the synchronous operation mode of the H8/3687's timer Z block to output PWM waveforms.
2. As is shown in figure 1.1, pulses with variable duty cycle are output by controlling the high-level widths of the pulses (the high-level width and pulse period are independently specified for each of the two pulse outputs).
3. Any desired duty cycle, 0% to 100%, can be obtained with the settings in registers.

$$\text{Duty cycle} = \frac{\text{High-level pulse width}}{\text{Period pulse}} \times 100\ (\%)$$

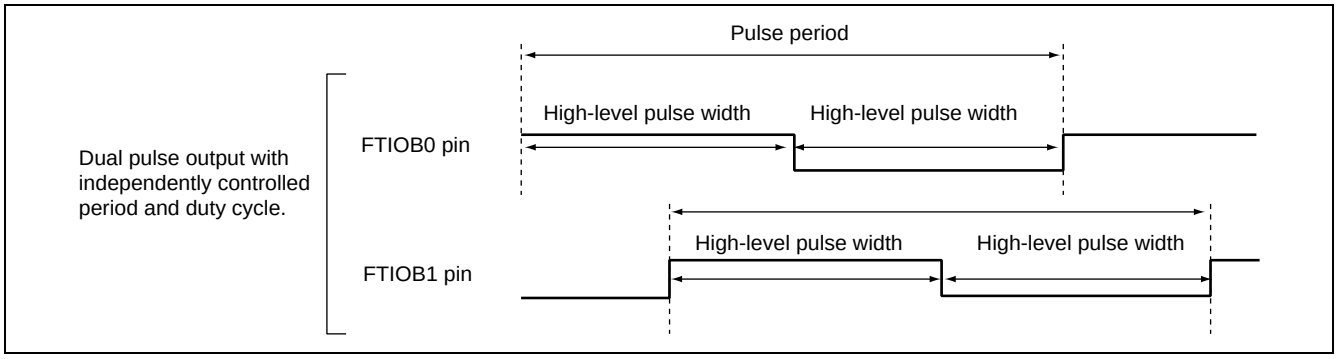


Figure 1.1 PWM Output

2. Function Usage

1. In this sample task, PWM waveforms are output through channel 0 of Timer Z.
   1) Figure 2.1 is a diagram of the Timer Z functions used in this sample task.
      The following Timer Z functions are used:

— Clearing of the timer counter upon a compare-match (counter clearing function).

— Combined use of the channels 0 and 1 (CH0 and CH1) to produce two PWM waveforms, where the level changes of the second waveform are controlled by compare-matches of the other channel (synchronous operation mode).

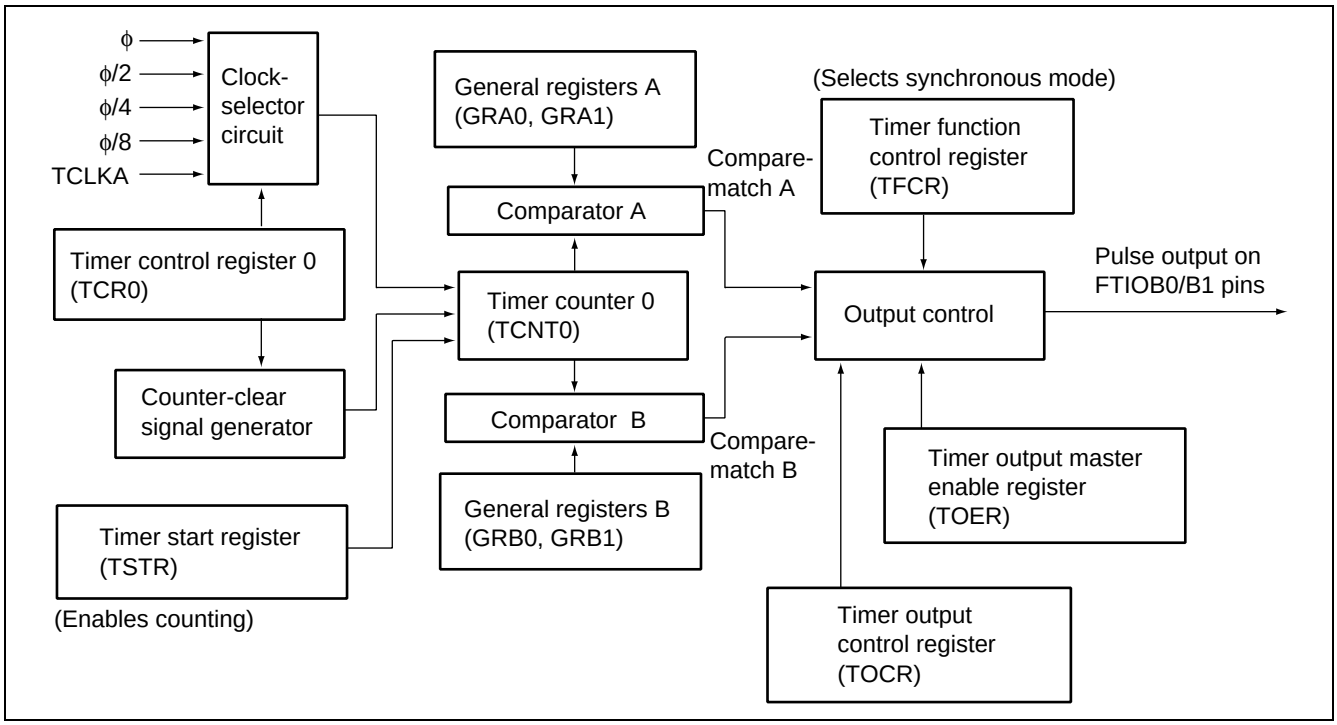


Figure 2.1 Timer Z Channels 0 and 1 in the Synchronous Operation Mode

2. Function assignments for this task are shown in table 2.1.

   To implement PWM waveform output in the synchronous operation mode, timer Z functions are assigned as listed below.

Table 2.1 Function Assignments

Pin/Register	Assigned Function
FTIOB0	Pulse output (pins)
FTIOB1	
TSTR	Starts/stops counting by the CH0 timer counter.
TCR0	Selects the input clock for and trigger for clearing of the CH0 timer counter.
TMDR	Selects the synchronous operation mode.
TOCR	Sets the initial output value, i.e., the value in effect until the first match.
TOER	Enables/disables the timer output.
GRA0	Sets the duty cycle of the output pulses on the FTIOA0 pin.
GRB0	Sets the period of the output pulses on the FTIOB0 pin.
GRA1	Sets the duty cycle of the output pulses on the FTIOA1 pin.
GRB1	Sets the period of the output pulses on the FTIOB1 pin.
TCNT0	Timer counter of CH0

3. Operation

The principle of operation is illustrated in figure 3.1. A PWM waveform is output through hardware and software processing by the H8/3687.

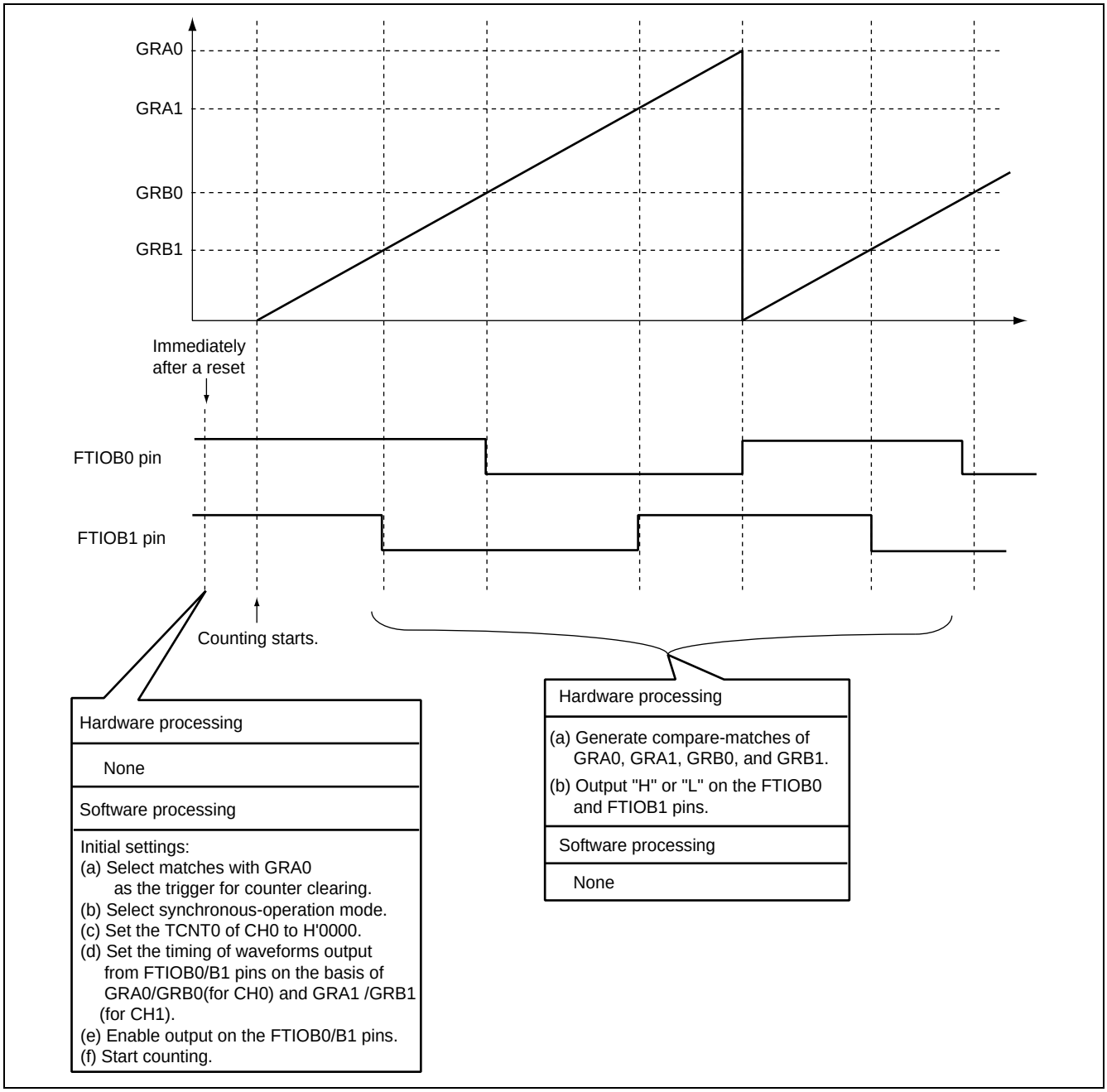


Figure 3.1 Principle of Operation: Output of Two PWM Waveforms in Synchronous Operation Mode

4. Description of the Software

4.1 Module

Module	Label	Function Assignment
Main routine	main	Sets the transition timing for the output pulse waveforms in GRA0, GRA1, GRB0, and GRB1; selects synchronous operation; and outputs the PWM waveforms.

4.2 Internal registers used

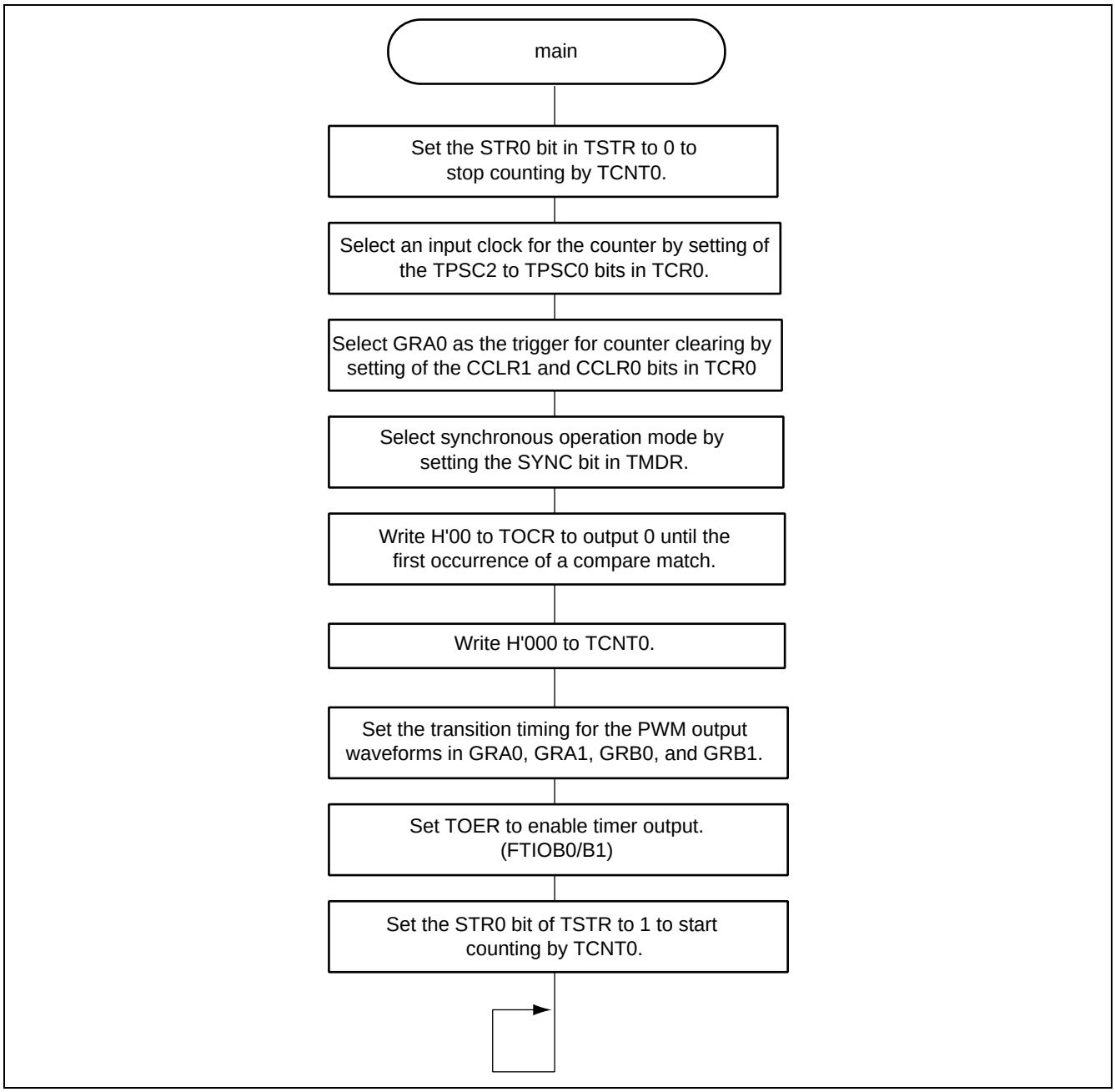
Pin/Register	Function Assignment
TSTR	Enables/disables the timer counter operation of CH0 and CH1.
TCR0	Selects the trigger of CH0 timer counter clearing and the input clock.
TMDR	Should be set for the synchronous operation mode.
TOCR	Sets the initial output value that is applied until the first match occurs.
TOER	Enables/disables the timer output.
GRA0	Sets a transition time for one of the PWM output waveform (duty cycle).
GRB0	Sets a transition time for one of the PWM output waveform (period).
GRA1	Sets a transition time for one of the PWM output waveform (duty cycle).
GRB1	Sets a transition time for one of the PWM output waveform (period).
TCNT0	Timer counter for CH0

4.3 RAM used

In this sample task, RAM is only used to hold the arguments.

5. Flowchart

1. Main routine



6. Program Listing

```
/************************************************************/
/*                                                          */
/*    H8/300HN Series -H8/368                               */
/*    Application Note                                      */
/*                                                          */
/*    'Synchronous Mode'                                    */
/*                                                          */
/*    Function                                              */
/*    :Timer Z Synchronous Mode                             */
/*                                                          */
/*    External Clock: 16 MHz                                */
/*    Internal Clock: 16 MHz                                */
/*    Sub Clock: 32.768kHz      */
/*                                                          */
/************************************************************/
#include    <C:\ch38\include\machine.h>

/************************************************************/
/*    Symbol Definition                                     */
/************************************************************/

struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define    TCR0   *(volatile unsigned char *)0xF700        /* Timer Control Register 0                    */
#define    TIORA0 *(volatile unsigned char *)0xF701        /* Timer I/O Control Register A0               */
#define    TIORC0 *(volatile unsigned char *)0xF702        /* Timer I/O Control Register C0               */
#define    TSR0   *(volatile unsigned char *)0xF703        /* Timer Status Register 0                     */
#define    TSR0_BIT (*(struct BIT *)0xF703)                /* Timer Status Register 0                     */
#define    IMIFA_0             TSR0_BIT.b0                 /* Input Caputure/Compare match Flag A         */
```

```
#define     TIER0  *(volatile unsigned char *)0xF704        /* Timer Interrupt Enable Register 0             */
#define     POCR0  *(volatile unsigned char *)0xF705        /* Port Output Level Control Register            */
#define     TCNT0  *(volatile unsigned short *)0xF706       /* Timer Counter 0                               */
#define     GRA0   *(volatile unsigned short *)0xF708       /* General Register A0                           */
#define     GRB0   *(volatile unsigned short *)0xF70A       /* General Register B0                           */
#define     GRC0   *(volatile unsigned short *)0xF70C       /* General Register C0                           */
#define     GRD0   *(volatile unsigned short *)0xF70E       /* General Register D0                           */

#define     TCR1   *(volatile unsigned char *)0xF710        /* Timer Control Register 1                      */
#define     TIORA1 *(volatile unsigned char *)0xF711        /* Timer I/O Control Register A1                 */
#define     TIORC1 *(volatile unsigned char *)0xF712        /* Timer I/O Control Register C1                 */
#define     TSR1   *(volatile unsigned char *)0xF713        /* Timer Status Register 1                       */
#define     TIER1  *(volatile unsigned char *)0xF714        /* Timer Interrupt Enable Register 0             */
#define     POCR1  *(volatile unsigned char *)0xF715        /* Port Output Level Control Register            */
#define     TCNT1  *(volatile unsigned short *)0xF716       /* Timer Counter 1                               */
#define     GRA1   *(volatile unsigned short *)0xF718       /* General Register A1                           */
#define     GRB1   *(volatile unsigned short *)0xF71A       /* General Register B1                           */
#define     GRC1   *(volatile unsigned short *)0xF71C       /* General Register C1                           */
#define     GRD1   *(volatile unsigned short *)0xF71E       /* General Register D1                           */

#define     TSTR   *(volatile unsigned char *)0xF720        /* Timer Start Register                          */
#define     TMDR   *(volatile unsigned char *)0xF721        /* Timer Mode Register                           */
#define     TPMR   *(volatile unsigned char *)0xF722        /* Timer PWM Mode Register                       */
#define     TFCR   *(volatile unsigned char *)0xF723        /* Timer Function Control Register               */
#define     TOER   *(volatile unsigned char *)0xF724        /* Timer Output Master Enable Register           */

/************************************************************/
/*    Function Definition                                   */
/************************************************************/
extern    void    INIT ( void );                            /* SP Set                                        */
void      main     ( void );

extern void _INITSCT();

/************************************************************/
/*    Vector Address                                         */
/************************************************************/
#pragma    section        V1                                /* VECTOR SECTION SET                            */
void       (*const VEC_TBL1[])(void) = {                     /* 0x00 - 0x0f                                   */
    INIT                                                     /* 00 Reset                                      */
```

```
};

#pragma    section                                          /* P                                          */
/*********************************************************/
/*    Main Program                                         */
/*********************************************************/
void main ( void )
{
   _INITSCT();

    set_imask_ccr(1);                                       /* Disable interrupts                         */

    TSTR = 0xFC;                                            /* Timer Stop                                 */
    TOCR = 0x00;                                            /* PWM initial output "0"                     */
    TPMR = 0x8F;                                            /* FTIOB0,FTIOC0,FTIOD0 PWM Mode              */

    TCR0 = 0x20;                                            /* GRA Compare match Clear Mode               */
    POCR0 = 0xFF;                                           /* FTIOB0,FTIOC0,FTIOD0 Active high           */

    GRA0 = 0x320;                                           /* Cycle 50us                                 */
    GRB0 = 0x230;                                           /* Duty 30%                                   */
    GRC0 = 0x230;                                           /* Duty 30%                                   */
    GRD0 = 0x230;                                           /* Duty 30%                                   */

    TOER = 0xF1;                                            /* FTIOB0,FTIOC0,FTIOD0 Output Enable         */

    TSTR = 0xFD;                                            /* TCNT0 Start                                */

    set_imask_ccr(0);                                       /* Interrupt Enable                           */

    while(1)    {
        ;
        }
}
```

INIT.SRC (Program list)

```
      .EXPORT_INIT
      .IMPORT_main
  ;
      .SECTION    P,CODE
  _INIT:
      MOV.W  #H'FF80,R7
      LDC.B  #B'10000000,CCR
      JMP           @_main
  ;
      .END
```

Link Addresses

Section Name	Address
CV1	H'0000
P	H'0100
B	H'F780