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SH7080 Group

SSU Master Reception (Reading from EEPROM via the SPI Bus)

Introduction

This application note describes master reception on the SPI interface using the SSU (Synchronous Serial Communication Unit) module. You can use this application note as reference information for designing user software.

Target Device

SH7085 (R5F7085)

Contents

1. Specifications 2
2. Description of Functions Used 4
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4. Description of Software 9
5. Flowcharts 16
Website and Contact Information 21

1. Specifications

Applicable Conditions

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 80 MHz
- C compiler: V.7.1.04 manufactured by Renesas Technology Corp.

(1) The SSU (Synchronous Serial Communication Unit) module of the SH7085 is used to read 10-byte data from a 4-wire serial-transmission (SPI bus) EEPROM (HN58X25128I, 128 Kbits, 16 Kwords × 8 bits).
(2) The connection is a single-master configuration with the SH7085 used as the master device.
(3) PE12 (general input/output port) is used as the chip select pin*.
(4) Data is read from the EEPROM in the address range of H'0000 to H'0009.
(5) The data transfer clock on the SPI bus is set to 2.5 MHz.
(6) Figure 1 shows an example of connection between the SH7085 and the EEPROM. Table 1 shows the SH7085 SSU settings.
(7) Table 2 is a list of EEPROM instruction codes used in this sample task.

Note: * The SSU module enables the $\overline{SCS}$ pin for each frame.
When one or more frames is transmitted or received, the $\overline{SCS}$ pin is used for general output.

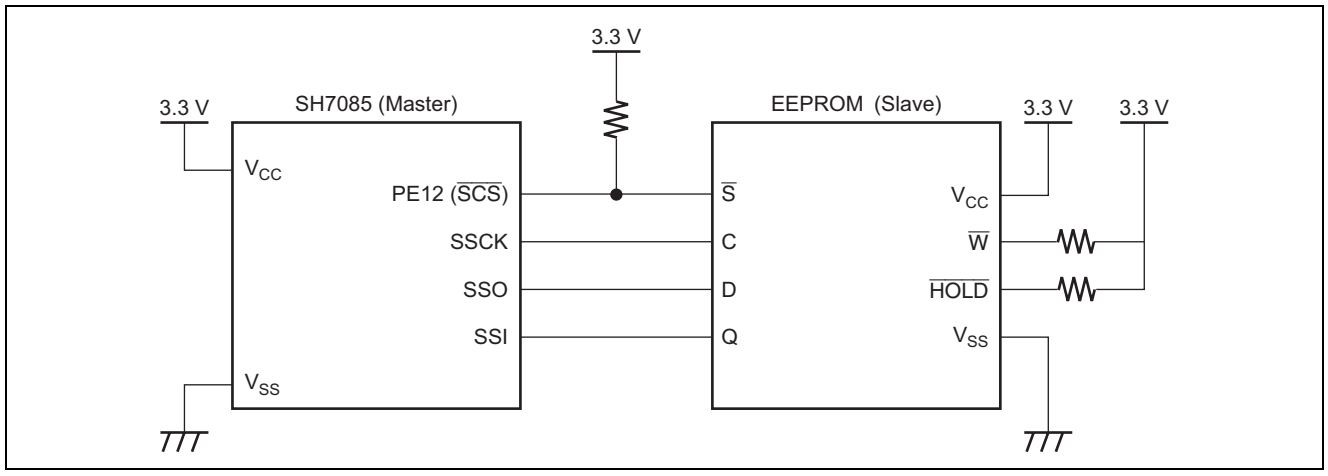


Figure 1 Example of Connection between the SH7085 and EEPROM

Table 1 SH7085 SSU Settings

Format	Settings
Operating mode	SSU master mode
Data input/output pin	Normal mode (input pins and output pins are independent)
Transfer clock	2.5MHz (Pϕ=40 MHz)
Number of data bits	8 bits
MSB/LSB first	MSB first
Timing for setting the TEND bit	After the final bit is transmitted

Table 2 EEPROM Instruction Codes

Code Name	Operation	Code [B']
WREN	Sets the EEPROM to be writable.	0000 0110
WRDI	Sets the EEPROM to be unwritable.	0000 0100
RDSR	Reads the EEPROM Status Register.	0000 0101
WRSR	Writes to the EEPROM Status Register.	0000 0001
READ	Reads stored data.	0000 0011
WRITE	Writes data.	0000 0010

2. Description of Functions Used

This sample task reads data from EEPROM through the SSU (Synchronous Serial Communication Unit).

2.1 Synchronous Serial Communication Unit (SSU)

The SSU supports a master mode (with clock output from this LSI) and a slave mode (clock input from an external device). In addition, the SSU allows synchronous serial communication between devices with different clock polarities and clock phases.

Figure 2 shows a block diagram of the SSU module.

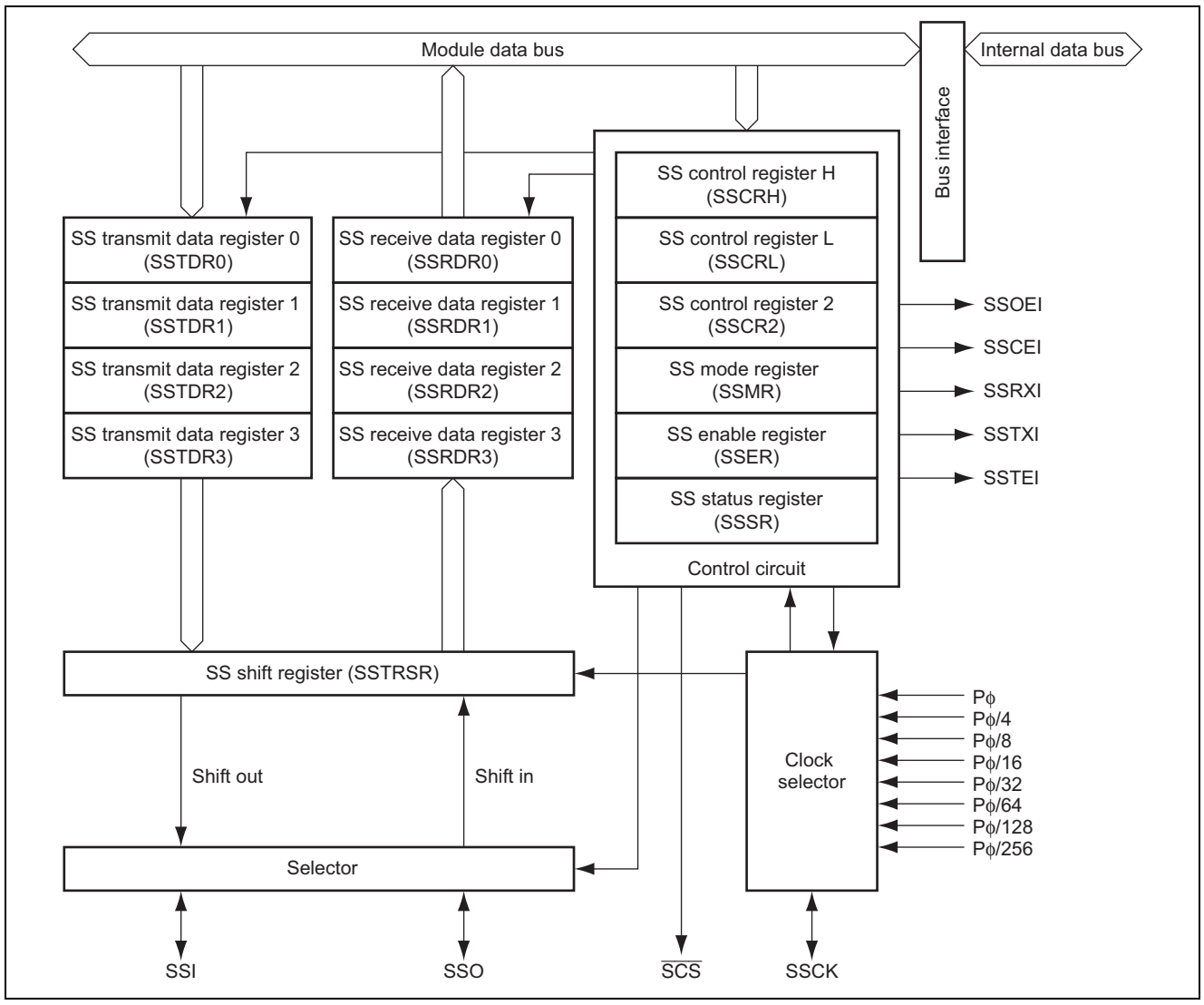


Figure 2 Block Diagram of the SSU Module

- SS Control Register H (SSCRH) selects the master or slave mode, selects the input/output pin mode, selects the SSO pin output value, and selects the $\overline{SCS}$ pin function.
- SS Control Register L (SSCRL) selects the operating mode, software reset, and the transmit/receive data length.
- The SS Mode Register (SSMR) selects MSB first or LSB first, the clock polarity, the clock phase, and the transfer clock rate.
- The SS Enable Register (SSER) enables and disables transmission, reception, and interrupts requests.
- The SS Status Register (SSSR) handles the status flags for various interrupts.
- SS Control Register 2 (SSCR2) sets open drain output of the SSO pin, SSI pin, SSCK pin, and $\overline{SCS}$ pin, the timing for asserting the $\overline{SCS}$ signal, the timing for outputting data from the SSO pin, and the timing for setting the TEND bit.
- SS Transmit Data Registers 0 to 3 (SSTDR0 to 3) are 8-bit registers used to store transmit data.
- SS Receive Data Registers 0 to 3 (SSRDR0 to 3) are 8-bit registers used to store receive data.
- The SS Shift Register (SSTRSR) is dedicated to serial data transmission and reception.

3. Principles of Operation

This sample task reads data from an EEPROM using concurrent transmit and receive operations in the SSU mode.

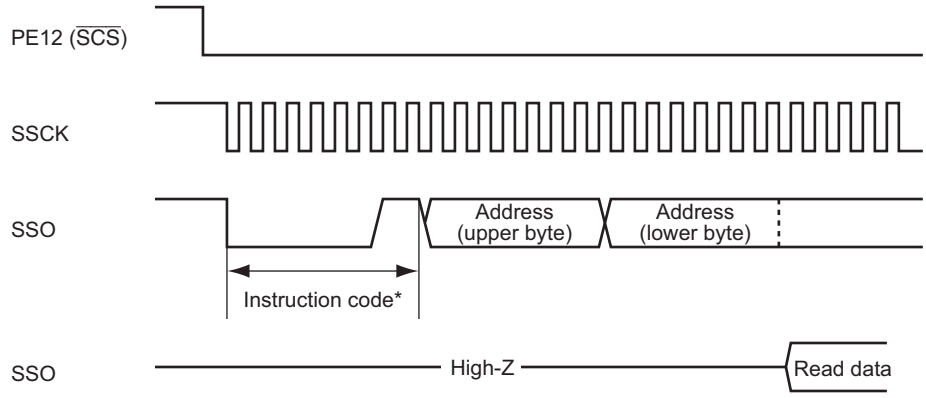
3.1 Reading Data from an EEPROM

The following procedure can be used to read from EEPROM:

1. Transmit the read code (READ) to the EEPROM
2. Transmit the read start address to the EEPROM
3. Output data from the EEPROM (receive data from the EEPROM)

Figure 3 shows the communication format for a data read from an EEPROM.

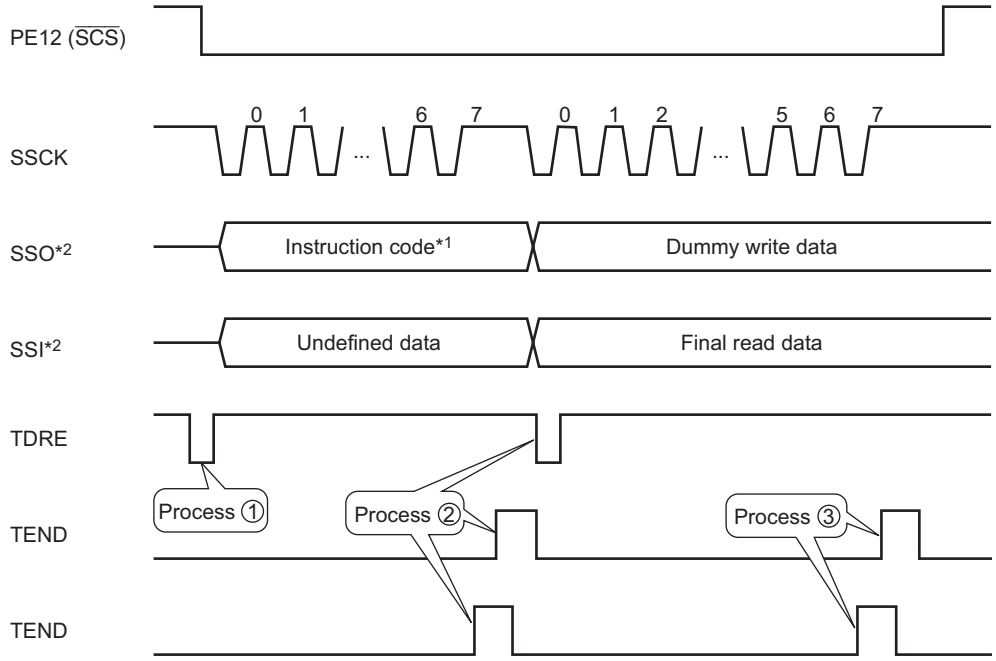
When data is read from an EEPROM, selecting the device (setting PE12 low) and continuously inputting the clock outputs data from the EEPROM. When one byte has been output, the EEPROM internally increments the address and outputs the data at the next address. When reading from the EEPROM is complete, the device is deselected (PE12 is set high). Any timing can be used to deselect the device.



Note: *The read code (READ) is set. For details of the code, see table 2.

Figure 3 Communication Processing for Reading Data from the EEPROM

Figure 4 illustrates how data is read from an EEPROM. The software and hardware processing illustrated in figure 4 is described in table 3.



Notes: *1. The read code (READ) is set. For details of the code, see table 2.
*2. After the read operation, the SSO and SSI signals retain the level of the final bit.

Figure 4 Operations for Reading Data

Table 3 Description of Software and Hardware Processing

Procedure	Software Processing	Hardware Processing
Process ①	• Set PE12 low (output; EEPROM selected). • Set transmit data (instruction code) in SSTDR0.	• Setting transmit data in SSTDR0 clears the TDRE bit to 0. • Transfer the transmit data from SSTDR0 to SSTRSR. • Set the TDRE bit to 1. • Transmit and receive the data.
Process ②	• Confirm RDRF = 1, and read the SSRDR0 register. • Confirm TDRE = 1, and set transmit data in the SSTDR0 register.	• Transmit and receive 1 frame (8 bits) of data. • Transfer data from the SSTRSR register to the SSRDR0 register. • Set the RDRF bit to 1. • After the last bit is transmitted with TDRE = 1, set the TEND bit to 1. • Clear the RDRF bit to 0 by reading the SSRDR0 register. • Setting transmit data in the SSTDR0 register clears the TDRE and TEND bits to 0. • Transfer the transmit data from the SSTDR0 register to the SSTRSR register. • Set the TDRE bit to 1. • Transmit and receive the data.
Process ③	• Confirm RDRF = 1, and read the SSRDR0 register. • Set PE12 high (output; EEPROM deselected). • Clear the TEND bit to 0. • Clear the TE and RE bits to 0 to disable the transmit and receive operations.	• Transmit and receive 1 frame (8 bits) of data. • Transfer data from the SSTRSR register to the SSRDR0 register. • Set the RDRF bit to 1. • After the last bit is transmitted with TDRE = 1, set the TEND bit to 1.

4. Description of Software

4.1 Descriptions of Modules

The modules used in this application sample are described in table 4.

Table 4 Description of Modules

Module Name	Label Name	Description
Main function	main()	Sets the operating frequency, sets the address to start reading from, calls the SSU initialization function, and calls the EEPROM data-read function.
SSU initialization function	init_ssu()	Takes the module out of module standby mode, makes the the pin function controller (PFC) setting, and sets the SSU.
EEPROM data-read function	read_EEPROM()	Reads data from the EEPROM.
Instruction code setting function	set_inst_code()	Sets an instruction code in the EEPROM Status Register.
EEPROM addressing function	set_addr_EEPROM()	Sets the read start address in the EEPROM.

4.2 Variables Used

The variables used in this application sample are described in table 5.

Table 5 Variables

Variable, Label Name	Description	Used In
read_data[0-9]	Array for storing read data	Main function
address	EEPROM address to start reading from	Main function
addr	Copy of the EEPROM read start address	EEPROM data-read function EEPROM addressing function
*r_data	Pointer variable to the array for storing the read data	EEPROM data-read function
num	Number of receive data	EEPROM data-read function
dmmy_w	Variable for a dummy write	EEPROM data-read function
dmmy_r	Variable for a dummy read	EEPROM data-read function Instruction code setting function EEPROM addressing function
code	Instruction code	Instruction code setting function

4.3 Setting the Registers

This section describes the setting of registers used in this sample application. Note that the settings presented below are used in the sample task and are not initial values.

4.3.1 Register Setting the Clock Pulse Generator (CPG)

(1) Frequency Control Register (FRQCR)

This register specifies the division ratio of the frequency.

Setting: H'0241

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	IFC[2:0]	000	Division ratio of the internal clock (Iϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
11-9	BFC[2:0]	001	Division ratio of the bus clock (Bϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
8-6	PFC[2:0]	001	Division ratio of the peripheral clock (Pϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
5-3	MIFC[2:0]	000	Division ratio of the MTU2S clock (MIϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
2-0	MPFC[2:0]	001	Division ratio of the MTU2 clock (MPϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz

4.3.2 Setting the Power-Down Mode

(1) Standby Control Register 3 (STBCR3)

This register controls the operation of each module in the power-down mode.

Setting: H'FB

Bit	Bit Name	Setting Value	Function
7	MSTP15	1	1: Stops clock supply to I^2C2.
6	MSTP14	1	1: Stops clock supply to the SCIF.
5	MSTP13	1	1: Stops clock supply to SCI_2.
4	MSTP12	1	1: Stops clock supply to SCI_1.
3	MSTP11	1	1: Stops clock supply to SCI_0.
2	MSTP10	0	0: SSU in operation.
1-0	—	11	Reserved

4.3.3 Register for Setting the Synchronous Serial Communication Unit (SSU)

(1) SS Control Register H (SSCRH)

This register selects the master or slave mode and sets the $\overline{SCS}$ pin function.

Setting: H'8F

Bit	Bit Name	Setting Value	Function
7	MSS	1	1: Master mode
6	BIDE	0	0: Normal mode (two input/output pins used for communication)
5	—	0	Reserved
4	SOL	0	0: Changes the serial data output to a low level.
3	SOLP	1	SOL write-protect Setting 0 changes the SOL bit.
2	—	1	Reserved
1-0	CSS[1:0]	11	11: The $\overline{SCS}$ pin is used as the automatic output function.

(2) SS Control Register L (SSCRL)

This register selects the operating mode, software reset, and the transmit/receive data length.

Setting: H'80

Bit	Bit Name	Setting Value	Function
7	FCLRM	0	0: Clears the interrupt flag when the register is accessed.
6	SSUMS	0	0: SSU mode
5	SRES	0	Setting 1 forcibly resets the SSU internally.
4-2	—	000	Reserved
1-0	DATS[1:0]	00	00: 8-bit data length

(3) SS Mode Register (SSMR)

This register selects MSB-first and the transfer clock.

Setting: H'83

Bit	Bit Name	Setting Value	Function
7	MLS	1	1: MSB first
6	CPOS	0	0: Outputs high from the SSCK pin in the idle state and low in the active state.
5	CPHS	0	0: Changes the data at the first edge on the SSCK pin.
4-3	—	00	Reserved
2-0	CKS[2:0]	011	011: Transfer clock = Pϕ/16 (Pϕ = 40 MHz)

(4) SS Enable Register (SSER)

This register enables transmit/receive operation.

Setting: H'C0

Bit	Bit Name	Setting Value	Function
7	TE	1	1: Enables transmit operation.
6	RE	1	1: Enables receive operation.
5-4	—	00	Reserved
3	TEIE	0	0: Disables SSTEI interrupts.
2	TIE	0	0: Disables SSTXI interrupts.
1	RIE	0	0: Disables SSRXI and SSOEI interrupts.
0	CEIE	0	0: Disables SSCEI interrupts.

(5) SS Status Register (SSSR)

This register shows the interrupt request flags and indicates status.

Setting: H'04

Bit	Bit Name	Setting Value	Function
7	—	0	Reserved
6	ORER	0	Overrun error
5-4	—	00	Reserved
3	TEND	0	Transmission end
2	TDRE	1	Transmit data empty
1	RDRF	0	Receive data register full
0	CE	0	Conflict error/incompletion error

(6) SS Control Register 2 (SSCR2)

This register selects the timing for setting the TEND bit.

Setting: H'10

Bit	Bit Name	Setting Value	Function
7	SDOS	0	0: Sets the serial data output pin to TTL output.
6	SSCKOS	0	0: Sets the SSCK pin to TTL output.
5	SCSOS	0	0: Sets the $\overline{\text{SCS}}$ pin to TTL output.
4	TENDSTS	1	1: Sets the TEND bit after transmission of the last bit.
3	SCSATS	0	Selects the timing for asserting the $\overline{\text{SCS}}$ signal*.
2	SSODTS	0	Selects the timing for outputting data from the SSO pin*.
1-0	—	00	Reserved

(7) SS Transmit Data Register 0 (SSTDR0)*

This register is an 8-bit register that stores transmit data.

Setting: H'00 (initial value)

Note: * Since the length of the transmit/receive data is 8 bits, SSTDR1 to SSTDR3 are not used.

(8) SS Receive Data Register 0 (SSRDR0)*

This register is an 8-bit register that stores receive data.

Setting: H'00 (initial value)

Note: * Since the length of the transmit/receive data is 8 bits, SSRDR1 to SSRDR3 are not used.

4.3.4 Registers for Setting the Pin Function Controller (PFC)

(1) Port E Control Register L4 (PECRL4)

This register selects the functions of multiplexed pins in port E (PE15-PE12).

Setting: H'0000

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PE15MD[2:0]	000	000: PE15 input/output (port)
11	—	0	Reserved
10-8	PE14MD[2:0]	000	000: PE14 input/output (port)
7-6	—	00	Reserved
5-4	PE13MD[1:0]	00	00: PE13 input/output (port)
3	—	0	Reserved
2-0	PE12MD[2:0]	000	000: PE12 input/output (port)

(2) Port E Control Register L3 (PECRL3)

This register selects the functions of multiplexed pins in port E (PE11-PE8).

Setting: H'0505

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PE11MD[2:0]	000	000: PE11 input/output (port)
11	—	0	Reserved
10-8	PE10MD[2:0]	101	101: Sets SSO (SSU data input/output).
7	—	0	Reserved
6-4	PE9MD[2:0]	000	000: PE9 input/output (port)
3	—	0	Reserved
2-0	PE8MD[2:0]	101	101: Sets SSCK (SSU clock input/output).

(3) Port E Control Register L2 (PECRL2)

This register selects the functions of multiplexed pins in port E (PE7-PE4).

Setting: H'5000

Bit	Bit Name	Setting Value	Function
15	—	0	Reserved
14-12	PE7MD[2:0]	101	101: Sets SSI (SSU data input/output).
11	—	0	Reserved
10-8	PE6MD[2:0]	000	000: PE6 input/output (port)
7	—	0	Reserved
6-4	PE5MD[2:0]	000	000: PE5 input/output (port)
3	—	0	Reserved
2-0	PE4MD[2:0]	000	000: PE4 input/output (port)

(4) Port E I/O Register L (PEIORL)

This register selects the input/output directions of the port E pins.

Setting: H'5000

Bit	Bit Name	Setting Value	Function
15	PE15IOR	0	0: PE15 input
14	PE14IOR	0	0: PE14 input
13	PE13IOR	0	0: PE13 input
12	PE12IOR	1	1: PE12 output ($\overline{\text{SCS}}$ used as a general input/output port)
11	PE11IOR	0	0: PE11 input
10	PE10IOR	0	0: PE10 input
9	PE9IOR	0	0: PE9 input
8	PE8IOR	0	0: PE8 input
7	PE7IOR	0	0: PE7 input
6	PE6IOR	0	0: PE6 input
5	PE5IOR	0	0: PE5 input
4	PE4IOR	0	0: PE4 input
3	PE3IOR	0	0: PE3 input
2	PE2IOR	0	0: PE2 input
1	PE1IOR	0	0: PE1 input
0	PE0IOR	0	0: PE0 input

4.3.5 Setting the I/O Port

(1) Port E Data Register L (PEDRL)

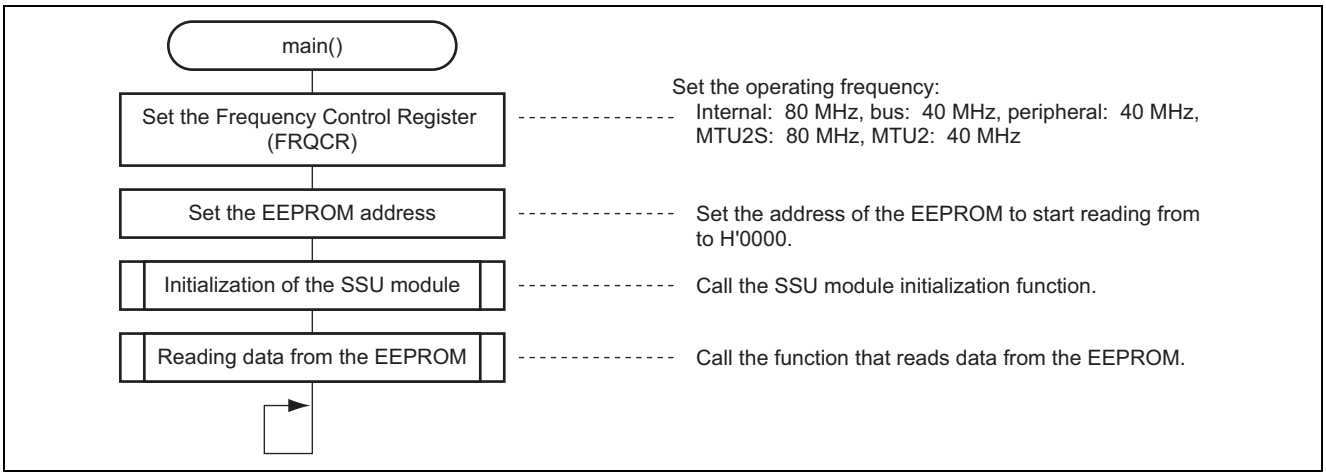
This register stores port E data.

Setting: H'1000

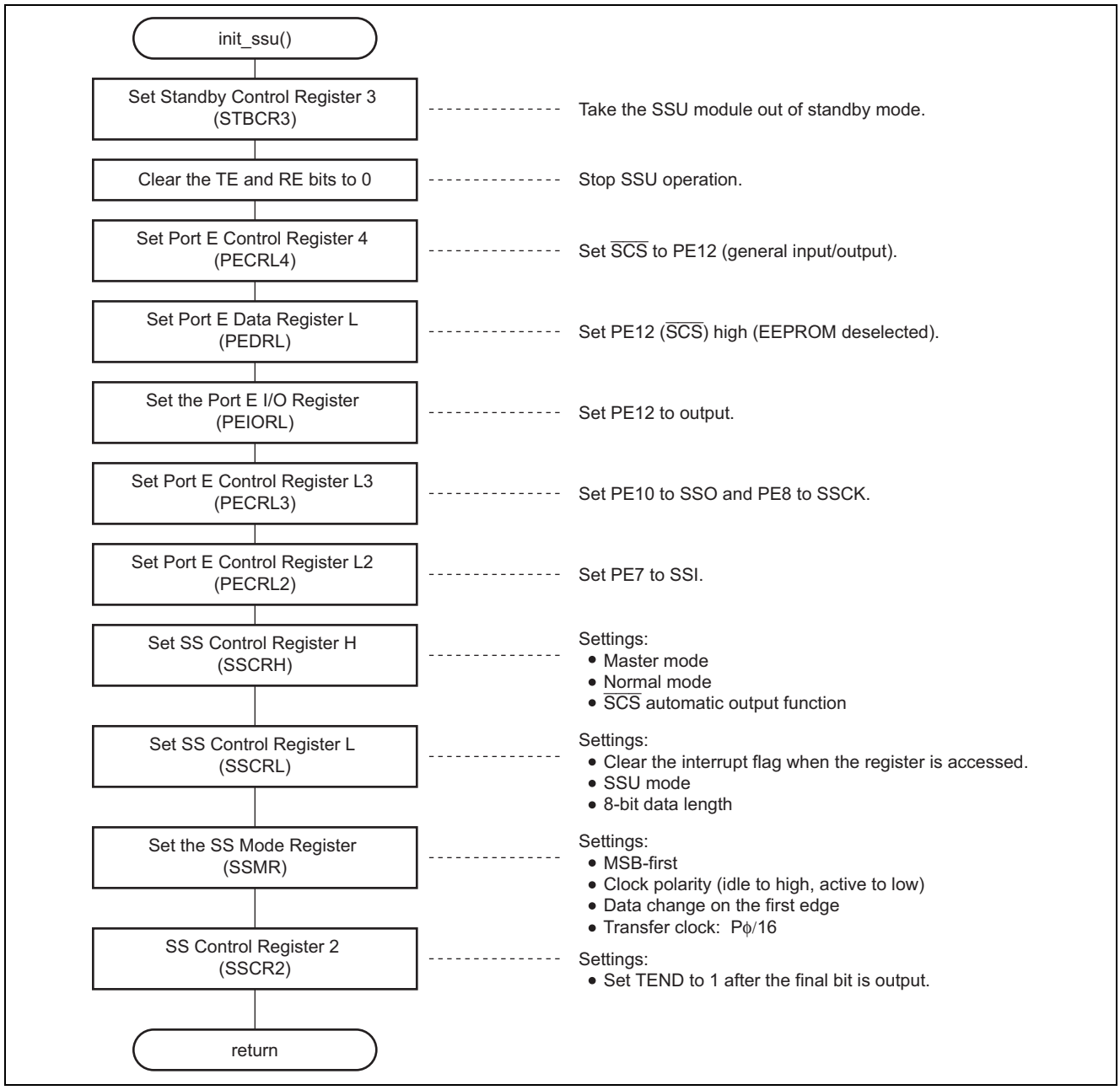
Bit	Bit Name	Setting Value	Function
15	PE15DR	0	0: The port state is low level.
14	PE14DR	0	0: The port state is low level.
13	PE13DR	0	0: The port state is low level.
12	PE12DR	1	0: The EEPROM is selected. 1: The EEPROM is deselected.
11	PE11DR	0	0: The port state is low level.
10	PE10DR	0	0: The port state is low level.
9	PE9DR	0	0: The port state is low level.
8	PE8DR	0	0: The port state is low level.
7	PE7DR	0	0: The port state is low level.
6	PE6DR	0	0: The port state is low level.
5	PE5DR	0	0: The port state is low level.
4	PE4DR	0	0: The port state is low level.
3	PE3DR	0	0: The port state is low level.
2	PE2DR	0	0: The port state is low level.
1	PE1DR	0	0: The port state is low level.
0	PE0DR	0	0: The port state is low level.

5. Flowcharts

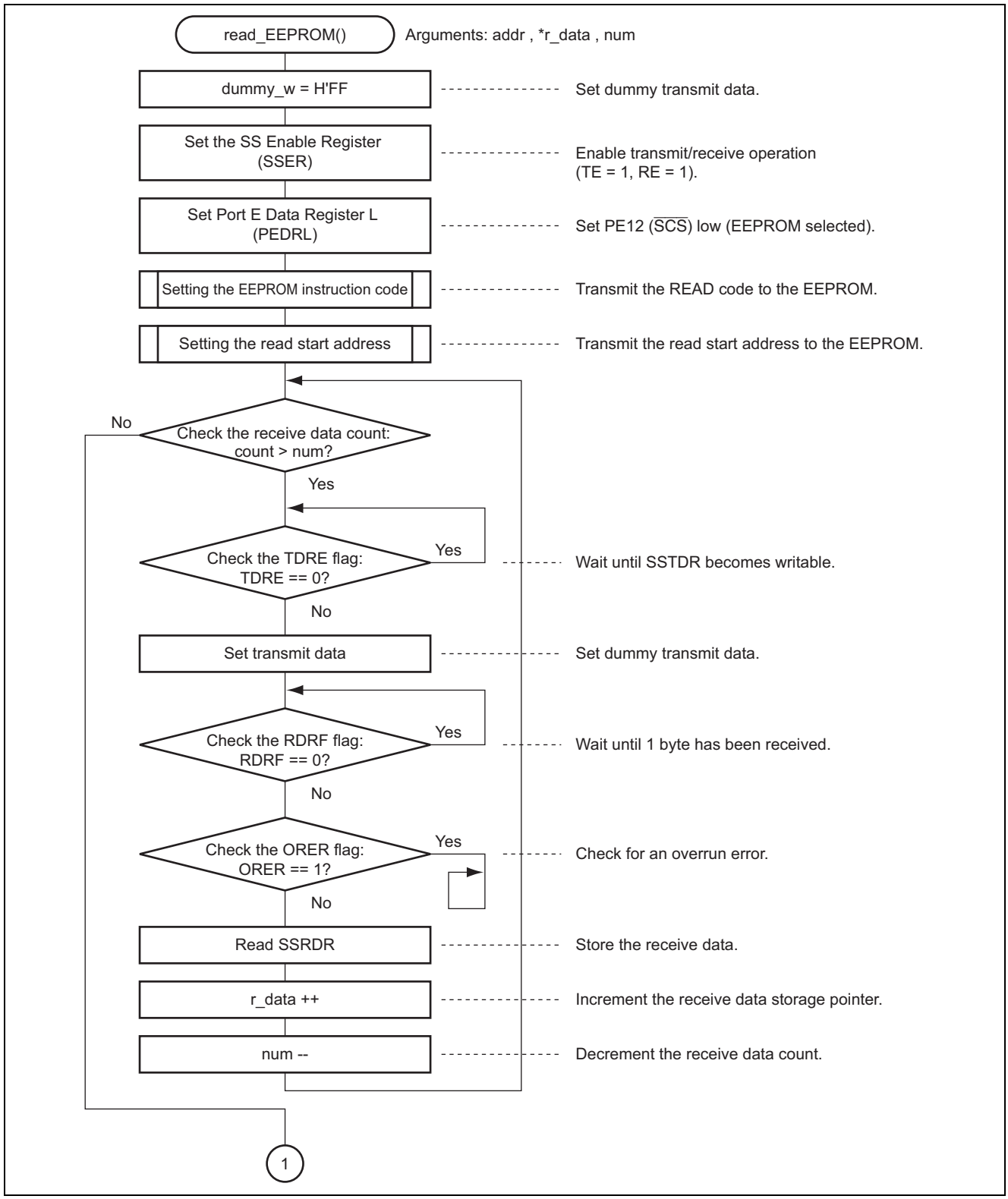
5.1 Main Function

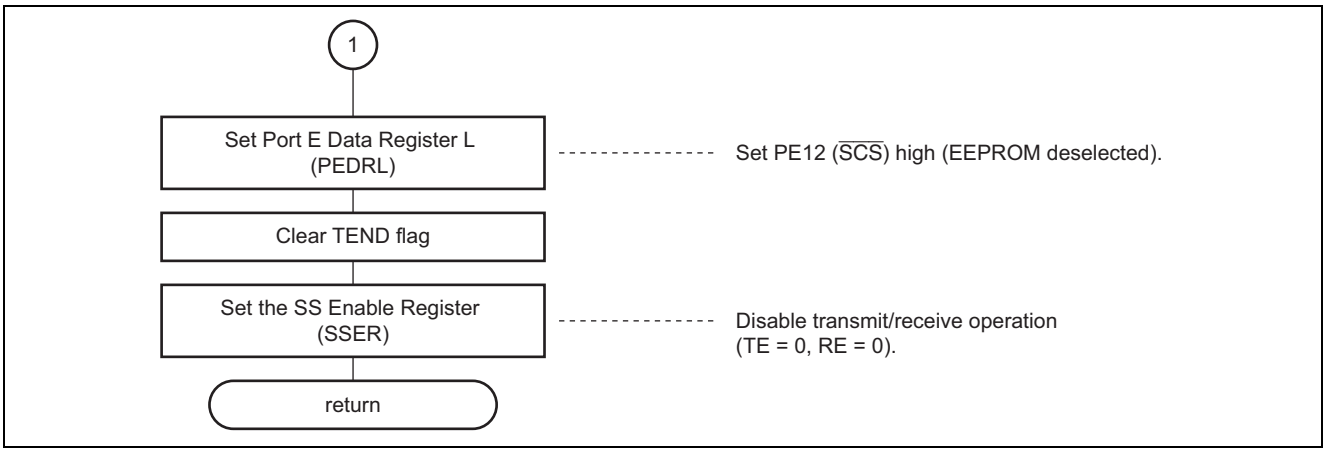


5.2 SSU Initialization Function

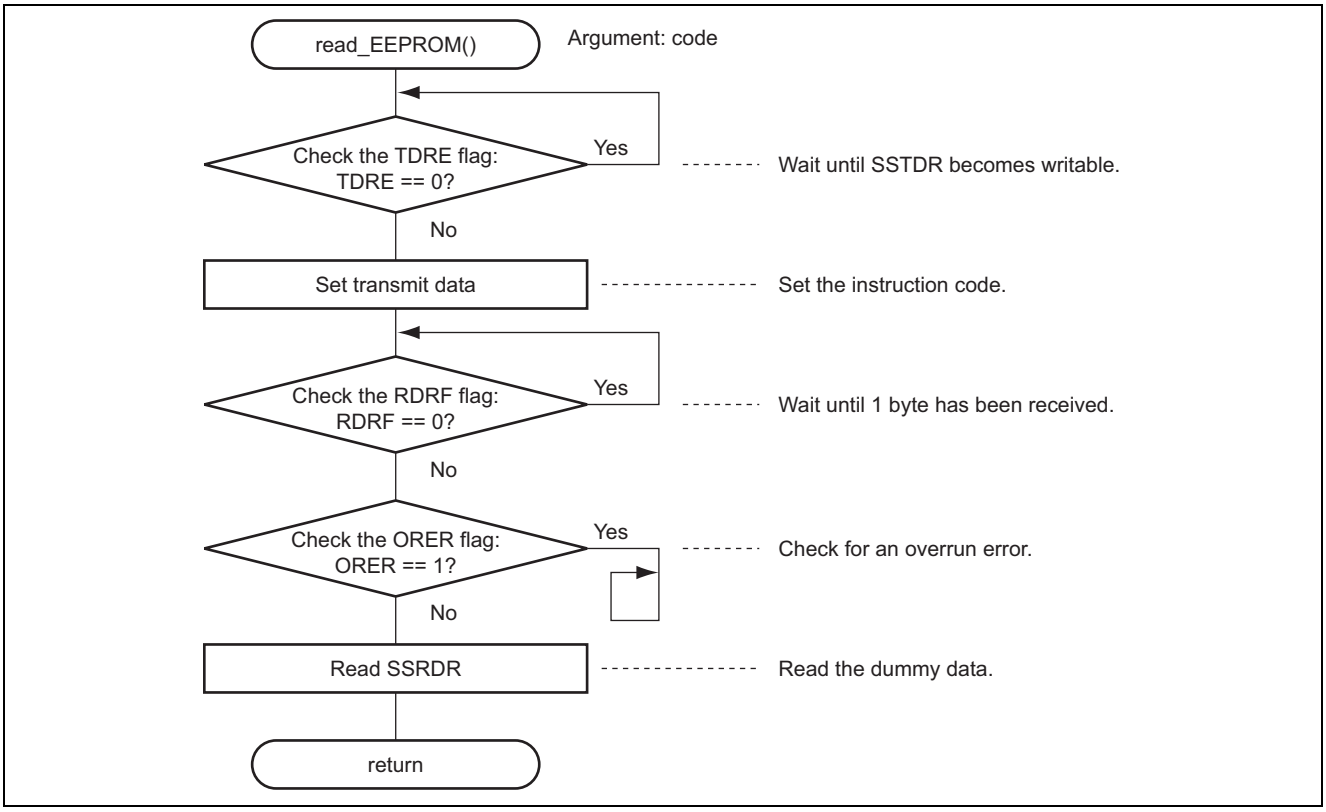


5.3 EEPROM Data-Read Function

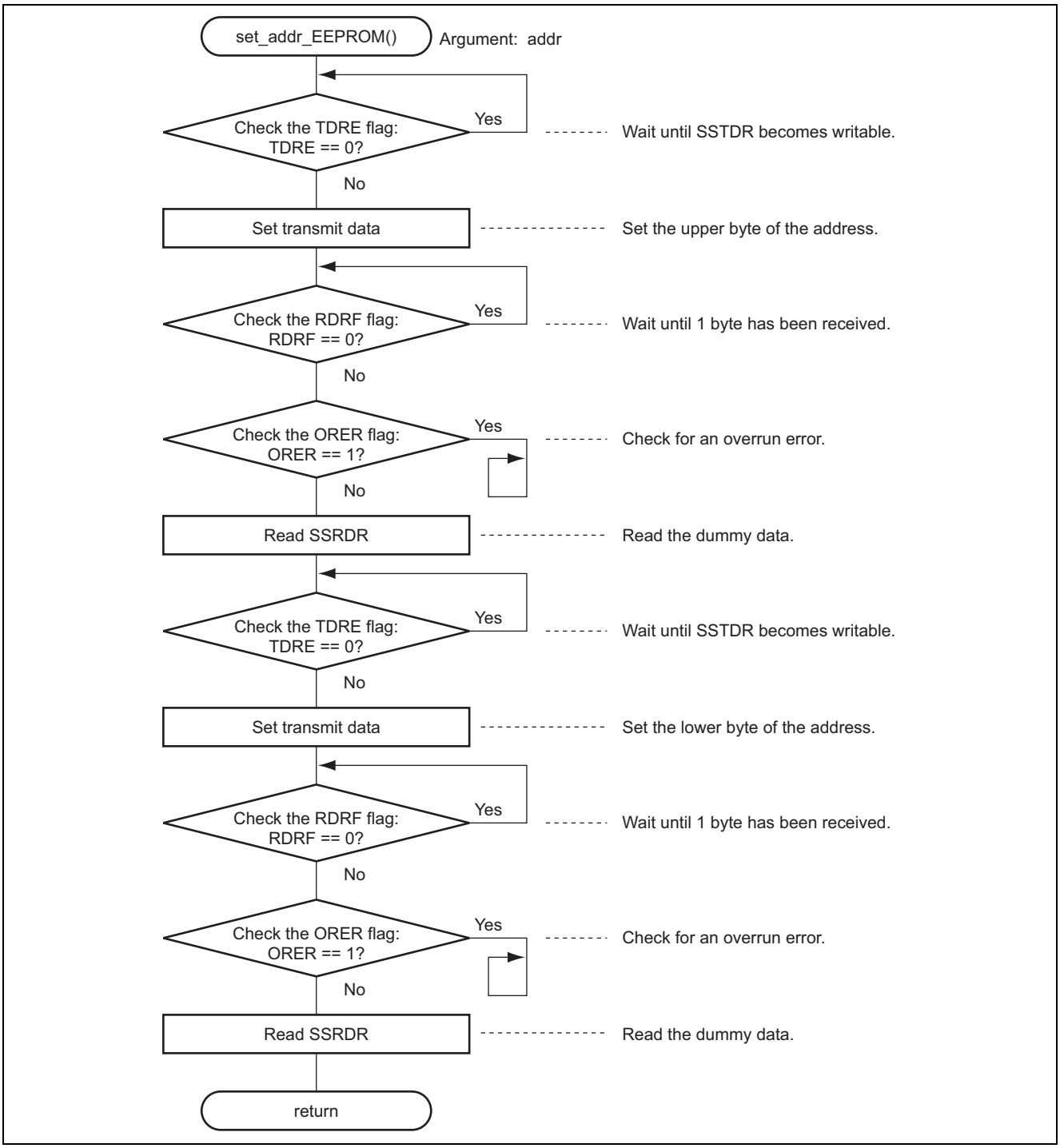




5.4 Instruction Code Setting Function



5.5 EEPROM Addressing Function



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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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