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H8/300H Tiny Series

Square Root of a 32-Bit Binary Number (SQRT)

Introduction

Produces the square root of a 32-bit binary number as a 16-bit binary number.

Target Device

H8/300H Tiny Series

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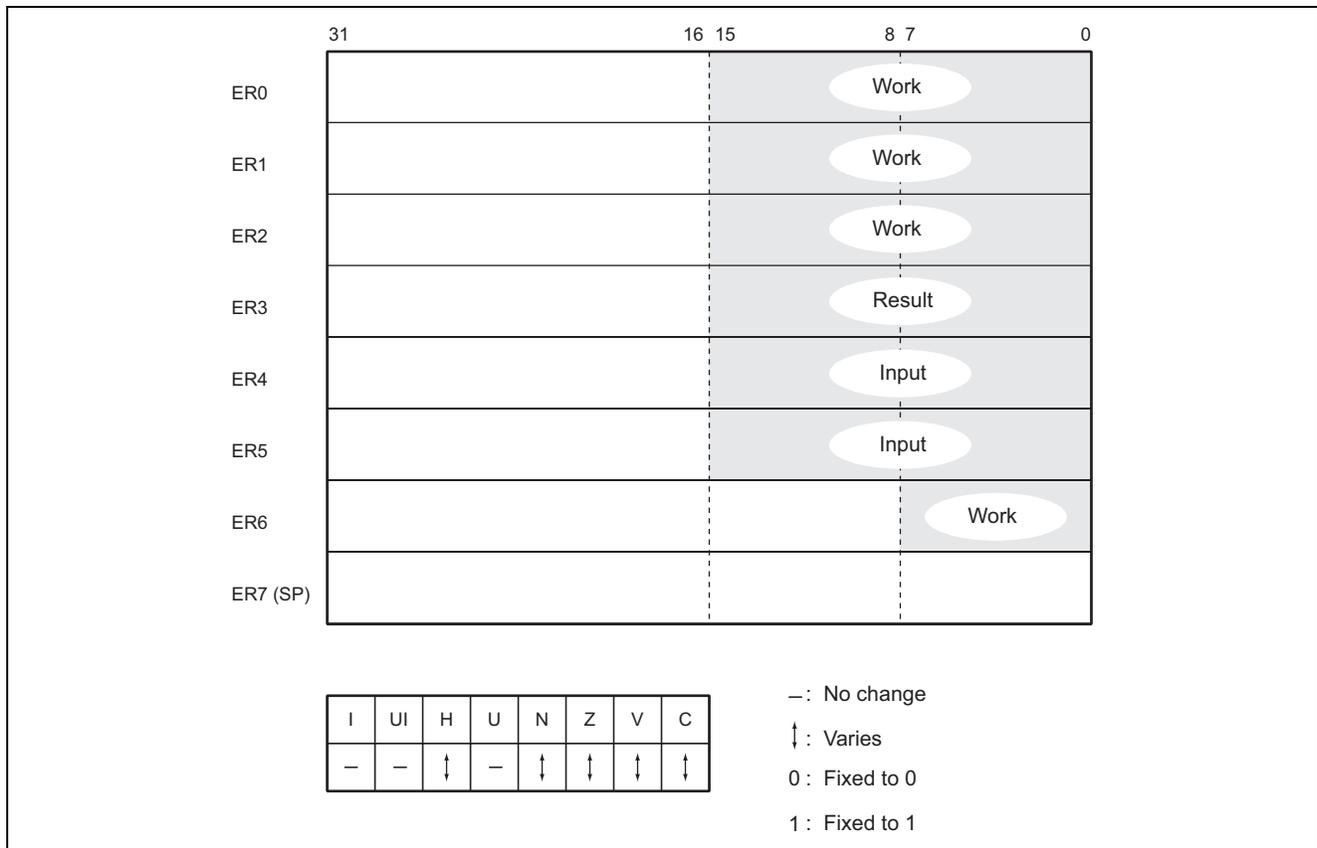
1. Function

1. Produces the square root of a 32-bit binary number as a 16-bit binary number.
2. Finds and outputs the square root of a 32-bit binary number as a 16-bit binary number.
3. The arguments are all unsigned integers. All data operations are on the general registers.

2. Arguments

	Contents	Storage Location	Data Length (Bytes)
Input	Original number (binary number for square-root extraction)	R4, R5	4
Output	Square root	R3	2

3. Changes to Internal Registers and Flags



4. Programming Specifications

	Program memory (bytes)	
	94	
	Data memory (bytes)	
	0	
	Stack (bytes)	
	0	
	Number of cycles	
	1340	
	Re-entrant	
	Yes	
	Relocatable	
	Yes	
	Interrupts during execution	
	Yes	

5. Note

The number of cycles in the programming specifications is the value in the execution of SQRT as shown in figure 1.

6. Description

6.1 Description of Functions

- The arguments are as follows.
 - R4: Set the higher-order word of the original number in 32-bit binary here, as an input argument.
 - R5: Set the lower-order word of the original number here.
 - R3: The square root (16-bit binary) is set here, as an output argument.
- The following figure illustrates the execution of the SQRT subroutine. When the input arguments are set as shown below, the corresponding square root is set in R3.

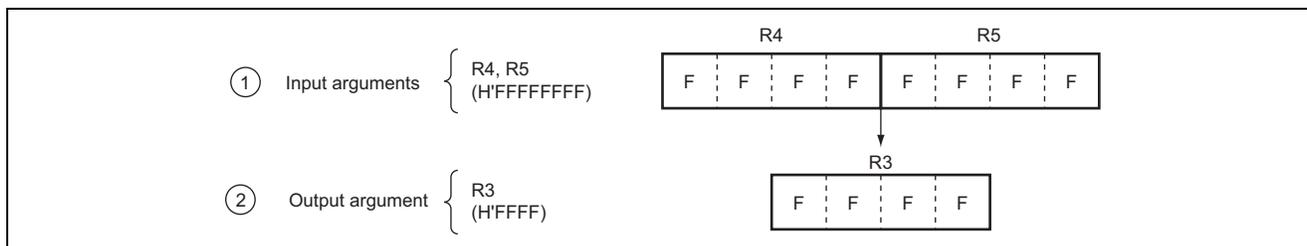


Figure 1 Example of SQRT Execution

6.2 Usage Notes

- Any higher-order bits of the input argument that are unused must be explicitly set to "0", as shown in figure 2. Otherwise, the correct result might not be obtained because undefined data in the higher-order bits is included in computation of the square root.

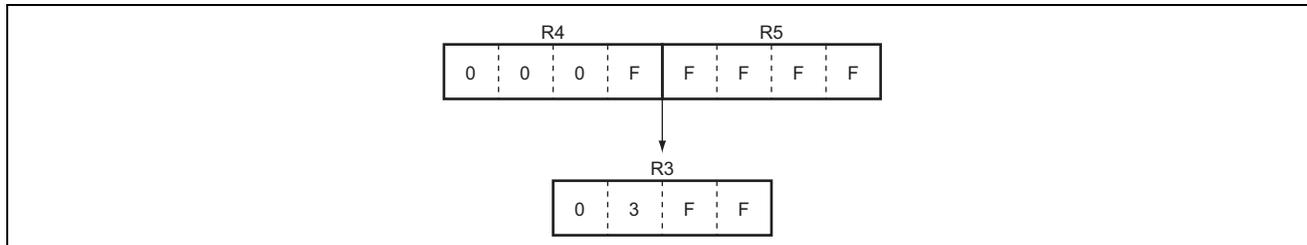


Figure 2 Example when Higher-order Bits are not Used

- The fractional part of the result is discarded.

6.3 Description of Data Memory

No data memory is used by SQRT.

6.4 Example of Usage

After setting the number for which the square root is to be extracted, call the SQRT subroutine.

```

WORK1 . RES. W 2      ..... Reservation of the data memory area for setting by the user program of the 32-bit binary
                        ..... number for square-root extraction.
WORK2 . RES. W 2      ..... Reservation of a data memory area to hold the 16-bit binary square root for the user program.
      .
      .
MOV. W @WORK1, R4     ..... Sets, as the input argument, the 32-bit binary number for square-root extraction that is specified
                        ..... by the user program.
MOV. W @WORK1+2, R5
JSR @SQRT             ..... Subroutine call of SQRT.
MOV. W R3, @WORK 2   ..... Transfers , to the data memory of the user program, the 16-bit binary square root the output by
                        ..... the subroutine.
      .
      .
  
```

6.5 Principles of Operation

1. The following figure shows the method used to calculate the square root (H'05) of the hexadecimal number H'22.

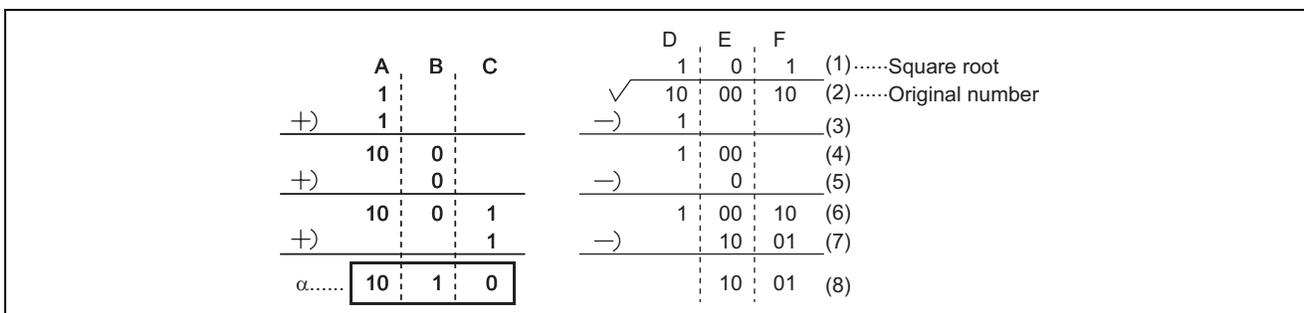
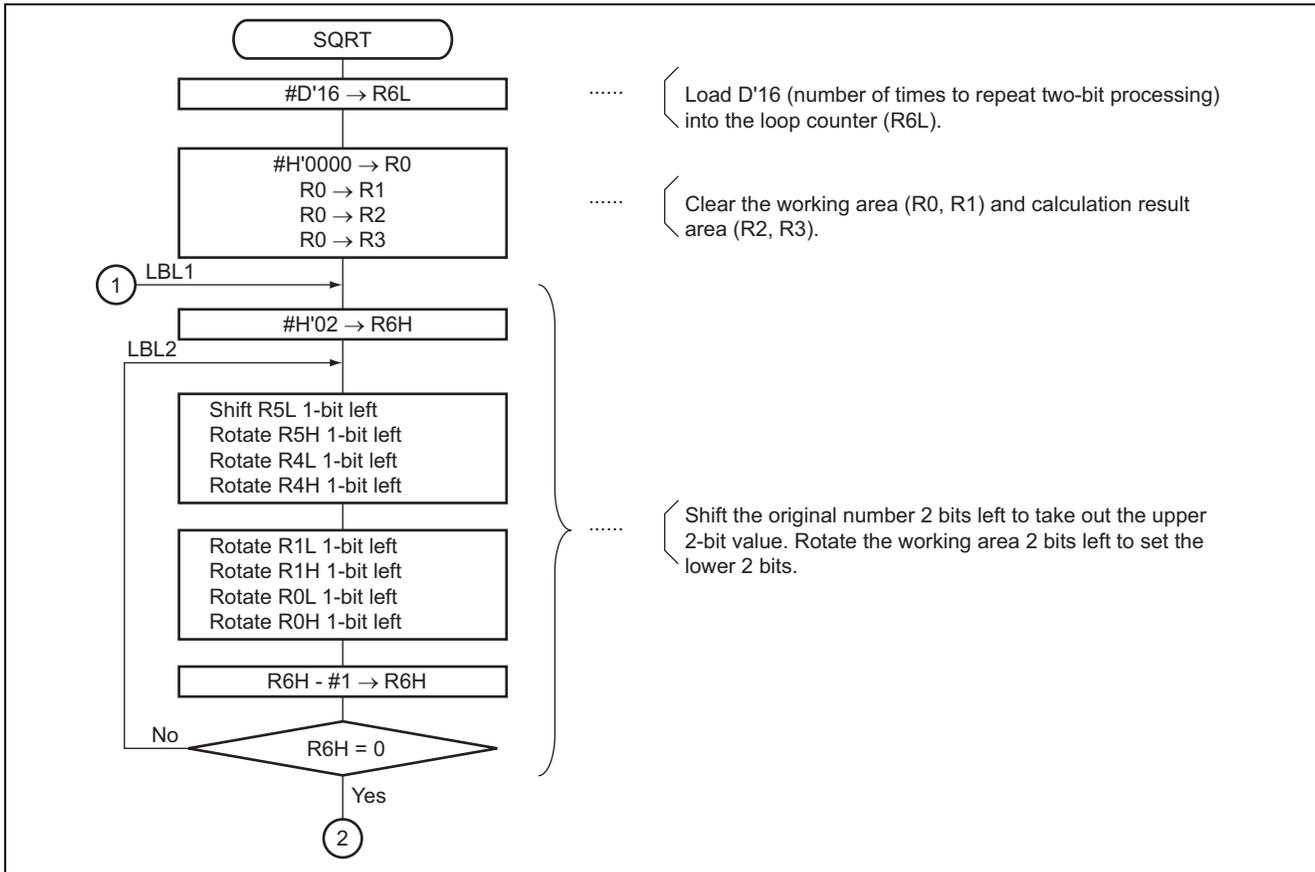
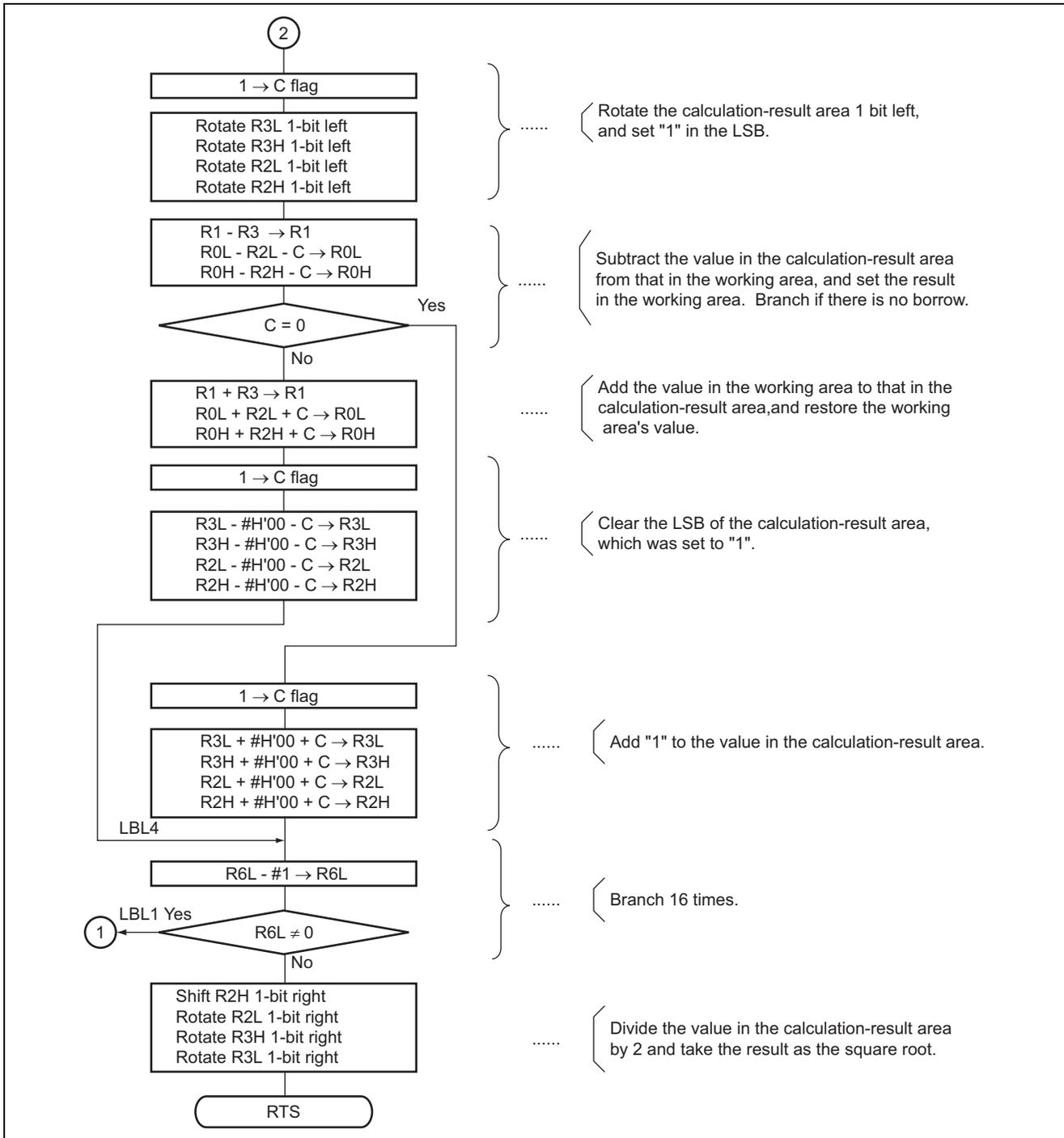


Figure 3 Calculation of Square Root

- 1) As shown in the figure, the square root can be found by processing every two-bit unit, from highest to lowest order, of the original number.
- 2) The square root (1) is equivalent to the quotient when α is divided by two. Parameter α is found through the operations A, B, and C in the figure. The SQRT subroutine finds the square root by calculating the value of α and then dividing it by two.
2. Details on the program are given below.
The program:
 - a) sets D'16 in R6L, which is the number of two-bit units in a 32-bit binary number;
 - b) clears the area for storage of the square root (R2, R3) and the working area (R0, R1);
 - c) extracts the two highest-order bits of the input binary number to R0 and R1, by rotating R4, R5, R0, and R1 two bits to the left;
 - d) places "1" in R2, R3;
 - e) subtracts R2, R3 from R0, R1 to find the difference (D, (2), (3), and (4)), then sets difference thus found in R0, R1; and
 - f) if the result is positive, increments R2, R3 (A to (4)); if the result is negative, decrements R2, R3, and adds R2, R3 to R0, R1 (D, E, and (6)).
3. In SQRT, R6 is decremented each time steps c) through f) above are performed, and this processing is repeated until R6 has reached "0".

7. Flowchart





8. Program Listing

```

1          1          ;*****
2          2          ;*
3          3          ;*          NAME : 32 BIT SQUARE ROOT (SQRT)
4          4          ;*
5          5          ;*****
6          6          ;*
7          7          ;*          ENTRY : R4,R5 (32 BIT BINARY)
8          8          ;*
9          9          ;*          RETURNS : R3 (SQUARE ROOT)
10         10         ;*
11         11         ;*****
12         12         ;
13         13         .CPU          300HN
14         14         .SECTION     SQRT_code, CODE, ALIGN=2
15         15         .EXPORT     SQRT
16         16         ;
17         17         SQRT        .EQU          $          ;Entry point
18         18         0000 FE10    18         MOV.B          #D'16,R6L      ;Set shift counter
19         19         0002 79000000 19         MOV.W          #H'0000,R0    ;Clear R0
20         20         0006 0D01    20         MOV.W          R0,R1      ;Clear R1
21         21         0008 0D02    21         MOV.W          R0,R2      ;Clear R2
22         22         000A 0D03    22         MOV.W          R0,R3      ;Clear R3
23         23         000C          23         LBL1
24         24         000C F602    24         MOV.B          #H'02,R6H
25         25         000E          25         LBL2
26         26         000E 100D    26         SHLL.B         R5L          ;Shift 32 bit binary 1 bit left
27         27         0010 1205    27         ROTXL.B        R5H
28         28         0012 120C    28         ROTXL.B        R4L
29         29         0014 1204    29         ROTXL.B        R4H
30         30         0016 1209    30         ROTXL.B        R1L
31         31         0018 1201    31         ROTXL.B        R1H
32         32         001A 1208    32         ROTXL.B        R0L
33         33         001C 1200    33         ROTXL.B        R0H
34         34         001E 1A06    34         DEC.B          R6H          ;Decrement R6H
35         35         0020 46EC    35         BNE          LBL2      ;Branch if Z=0
36         36         0022 0401    36         ORC.B         #H'01,CCR    ;Set C flag of CCR
37         37         0024 120B    37         ROTXL.B        R3L      ;Rotate square root
38         38         0026 1203    38         ROTXL.B        R3H
39         39         0028 120A    39         ROTXL.B        R2L
40         40         002A 1202    40         ROTXL.B        R2H
41         41         002C 1931    41         SUB.W          R3,R1      ;R1 - R3 -> R1
42         42         002E 1EA8    42         SUBX.B         R2L,R0L    ;R0L - R2L - C -> R0L
43         43         0030 1E20    43         SUBX.B         R2H,R0H    ;R0H - R2H - C -> R0H
44         44         0032 4412    44         BCC          LBL3      ;Branch if C=0
45         45         0034 0931    45         ADD.W          R3,R1      ;R1 + R3 -> R1
46         46         0036 0EA8    46         ADDX.B         R2L,R0L    ;R0L + R2L + C -> R0L
47         47         0038 0E20    47         ADDX.B         R2H,R0H    ;R0H + R2H + C -> R0H
48         48         003A 0401    48         ORC.B         #H'01,CCR    ;Bit set C flag of CCR
49         49         003C BB00    49         SUBX.B         #H'00,R3L    ;R3L - #H'00 - C -> R3L
50         50         003E B300    50         SUBX.B         #H'00,R3H    ;R3H - #H'00 - C -> R3H
51         51         0040 BA00    51         SUBX.B         #H'00,R2L    ;R2L - #H'00 - C -> R2L
52         52         0042 B200    52         SUBX.B         #H'00,R2H    ;R2H - #H'00 - C -> R2H

```

```

53      0044  400A      53      BRA      LBL4      ;
54      0046      54      LBL3
55      0046  0401      55      ORC.B      #H'01,CCR      ;Bit set C flag of CCR
56      0048  9B00      56      ADDX.B     #H'00,R3L      ;R3L + #H'00 + C -> R3L
57      004A  9300      57      ADDX.B     #H'00,R3H      ;R3H + #H'00 + C -> R3H
58      004C  9A00      58      ADDX.B     #H'00,R2L      ;R2L + #H'00 + C -> R2L
59      004E  9200      59      ADDX.B     #H'00,R2H      ;R2H + #H'00 + C -> R2H
60      0050      60      LBL4
61      0050  1A0E      61      DEC.B      R6L      ;Decrement shift counter
62      0052  46B8      62      BNE      LBL1      ;Branch if
63      0054  1102      63      SHLR.B     R2H
64      0056  130A      64      ROTXR.B    R2L
65      0058  1303      65      ROTXR.B    R3H      ;Rotate square root
66      005A  130B      66      ROTXR.B    R3L
67      005C  5470      67      RTS
68      68      ;
69      69      .END
***** TOTAL ERRORS 0
***** TOTAL WARNINGS 0

```

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Jun.12.06	—	Format has been changed from Hitachi version to Renesas version.

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