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Renesas Electronics Corporation

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H8/300H Tiny Series

Signed 32-Bit Binary Multiplication (MULS)

Introduction

Carries out binary multiplication in this format:
multiplicand (signed, 32 bits) × multiplier (signed, 32 bits) = product (signed, 64 bits).

Target Device

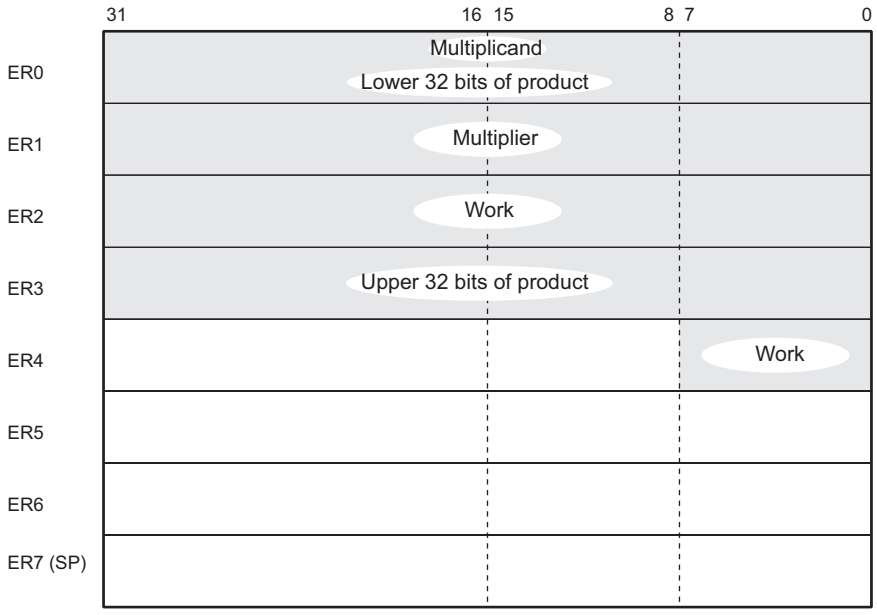
H8/300H Tiny Series

Contents

1. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Multiplicand (signed, 32 bits)	ER0	4
	Multiplier (signed, 32 bits)	ER1	4
Output	Upper 32 bits of the product (signed, 64 bits)	ER3	4
	Lower 32 bits of the product (signed, 64 bits)	ER0	4

2. Changes to Internal Registers and Flag Changes



I	UI	H	U	N	Z	V	C
–	–	↕	–	↕	↕	↕	↕

– : No change
↕ : Varies
0 : Fixed to 0
1 : Fixed to 1

3. Programming Specifications

Program memory (bytes)
66
Data memory (bytes)
0
Stack (bytes)
0
Number of cycles
156
Re-entrant
Yes
Relocatable
Yes
Interrupts during execution
Yes

4. Note

The number of cycles in the programming specifications is the value for calculation of H'80000000 × H'7FFFFFFF.

5. Description

5.1 Description of Functions

1. The arguments are as follows.
   ER0: Set the multiplicand (signed, 32 bits) as an input argument. The lower 32 bits of the product (signed, 64 bits) are set here as an output argument.
   ER1: Set the multiplier (signed, 32 bits) as an input argument.
   ER3: The upper 32 bits of the product (signed 64 bits) are set here as an output argument.
2. The following figure illustrates the execution of the MULS subroutine. When the input arguments are set as shown, the product is placed in ER3 and ER0.

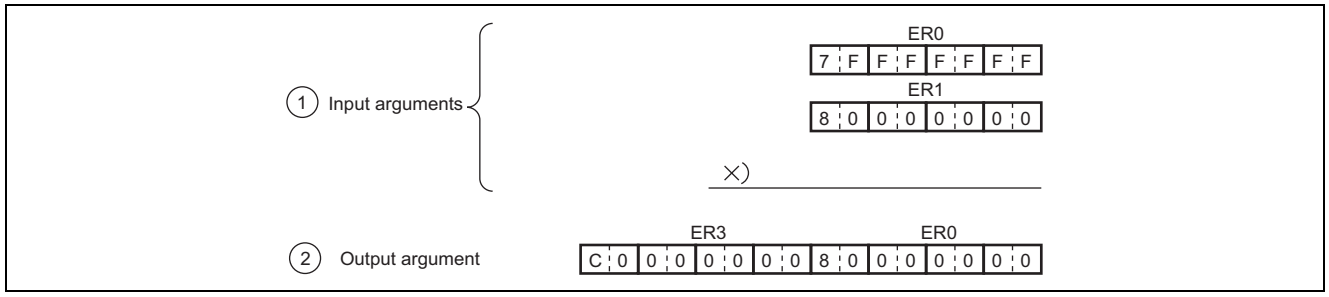


Figure 1 Example of MULS Execution

5.2 Usage Notes

Since the results of multiplication are placed in the same registers as are used to set the multiplicand and multiplier, the multiplicand and multiplier are lost through execution of MULS. When you will still require the multiplicand and multiplier, save them elsewhere in memory beforehand.

5.3 Description of Data Memory

No data memory is used by MULS.

5.4 Example of Usage

After setting the multiplicand and multiplier, call the MULS subroutine.

```
WORK1   . RES. L 1          ..... Reservation of the data memory area for setting of the multiplicand (signed, 32 bits) by the user
                                  program.
WORK2   . RES. L 1          ..... Reservation of the data memory area for setting of the multiplier (signed, 32 bits) by the user
                                  program.
          .
          .
          .
        MOV. L @WORK1, ER0  ..... Sets, as an input argument, the multiplicand (signed, 32 bits) specified by the user program.

        MOV. L @WORK2, ER1  ..... Sets, as an input argument, the multiplier (signed, 32 bits) specified by the user program.

        JSR    @MULS        ..... Subroutine call of MULS.
```

5.5 Principles of Operation

1. Negative multiplicands and multipliers are converted to positive.
2. The subroutine then finds partial products ((1), (2), (3), and (4) in the figure) and obtains the final result of multiplication ((5) in the figure) by summing the partial products. The partial products are found by using the instruction for the signed multiplication (MULXU.W) of two 16-bit binary numbers.
3. The product is converted to a negative number if the sign flag is 1, as is shown in table 1.

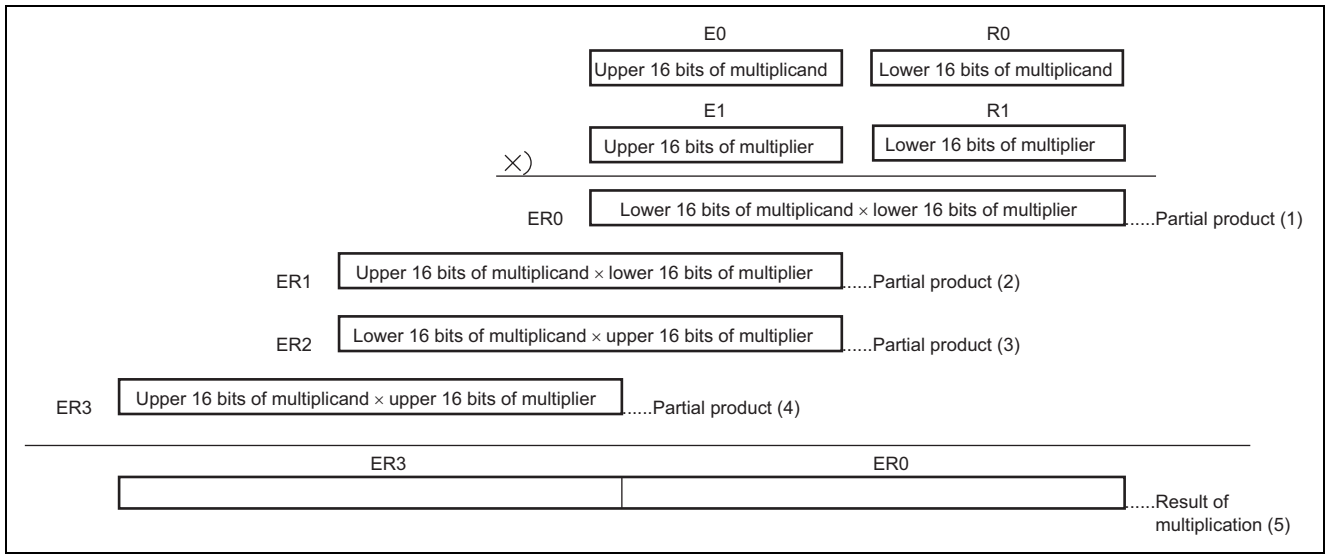
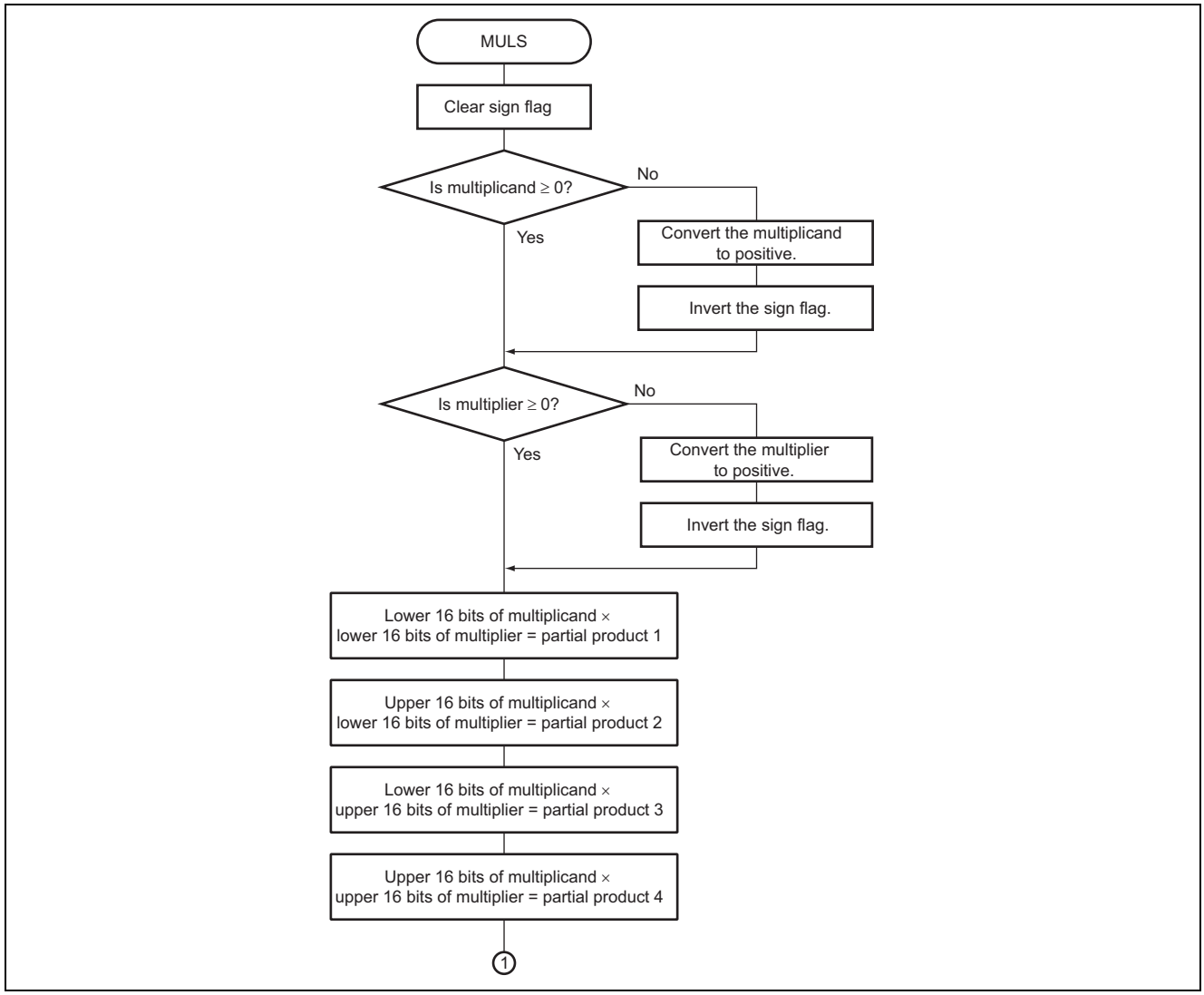


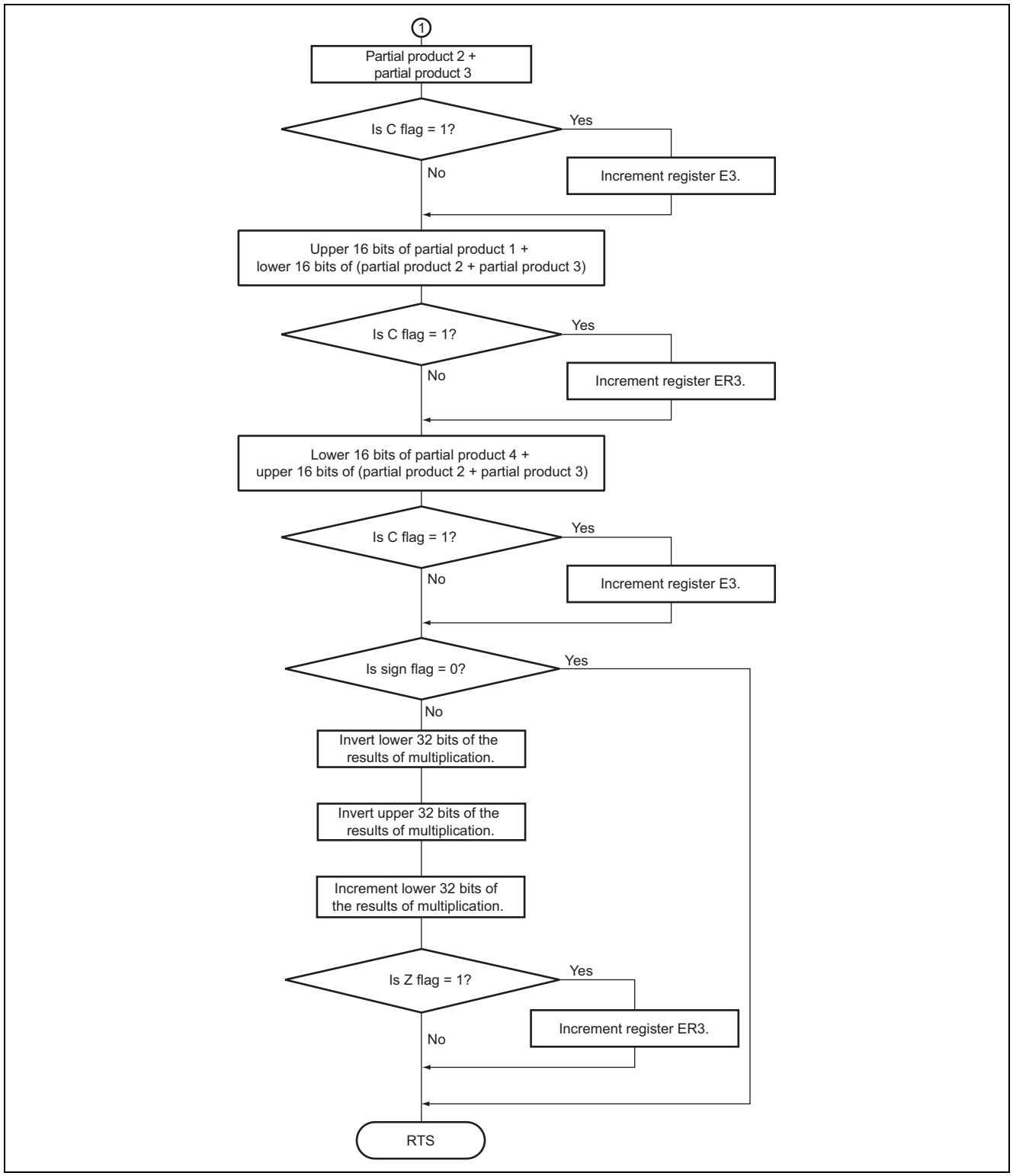
Figure 2 Multiplication

Table 1 Sign of Multiplication Result and the Sign Flag

Multiplicand	Multiplier	Product	Sign Flag
Positive	Positive	Positive	0
	Negative	Negative	1
Negative	Positive	Negative	1
	Negative	Positive	0

6. Flowchart


MULS
Clear sign flag
Is multiplicand ≥ 0?
No
Yes
Convert the multiplicand to positive.
Invert the sign flag.
Is multiplier ≥ 0?
No
Yes
Convert the multiplier to positive.
Invert the sign flag.
Lower 16 bits of multiplicand × lower 16 bits of multiplier = partial product 1
Upper 16 bits of multiplicand × lower 16 bits of multiplier = partial product 2
Lower 16 bits of multiplicand × upper 16 bits of multiplier = partial product 3
Upper 16 bits of multiplicand × upper 16 bits of multiplier = partial product 4
1


1
Partial product 2 + partial product 3
Is C flag = 1?
Yes
Increment register E3.
No
Upper 16 bits of partial product 1 + lower 16 bits of (partial product 2 + partial product 3)
Is C flag = 1?
Yes
Increment register ER3.
No
Lower 16 bits of partial product 4 + upper 16 bits of (partial product 2 + partial product 3)
Is C flag = 1?
Yes
Increment register E3.
No
Is sign flag = 0?
Yes
No
Invert lower 32 bits of the results of multiplication.
Invert upper 32 bits of the results of multiplication.
Increment lower 32 bits of the results of multiplication.
Is Z flag = 1?
Yes
Increment register ER3.
No
RTS

7. Program Listing

```
1                                       1     ;*********************************************************************
2                                       2     ;*                                                                   *
3                                       3     ;*         NAME     :    32 BIT SIGNED MULTIPLICATION   (MULS)       *
4                                       4     ;*                                                                   *
5                                       5     ;*********************************************************************
6                                       6     ;*                                                                   *
7                                       7     ;*         ENTRY    :   ER0              (MULTIPLICAND)             *
8                                       8     ;*                       ER1              (MULTIPLIER)               *
9                                       9     ;*         RETURNS  :   ER3              (UPPER 32 BIT PRODUCT)     *
10                                      10    ;*                       ER0              (LOWER 32 BIT PRODUCT)     *
11                                      11    ;*                                                                   *
12                                      12    ;*********************************************************************
13                                      13    ;
14                                      14              .CPU          300HA
15  001000                              15              .SECTION A,CODE,LOCATE=H'001000
16          00001000                    16    MULS      .EQU          $               ;Entry point
17  001000  727C                        17              BCLR          #7,R4L          ;Clear flag
18  001002  0F80                        18              MOV.L         ER0,ER0         ;
19  001004  58A00004                    19              BPL           MULS1           ;
20  001008  17B0                        20              NEG.L         ER0             ;If minus then change to plus
21  00100A  717C                        21              BNOT          #7,R4L          ;Change flag
22  00100C  0F91                        22    MULS1     MOV.L         ER1,ER1         ;
23  00100E  58A00004                    23              BPL           MULS2           ;
24  001012  17B1                        24              NEG.L         ER1             ;If minus then change to plus
25  001014  717C                        25              BNOT          #7,R4L          ;Change flag
26  001016  0D02                        26    MULS2     MOV.W         R0,R2           ;
27  001018  0D83                        27              MOV.W         E0,R3           ;
28  00101A  0D9B                        28              MOV.W         E1,E3           ;
29  00101C  5210                        29              MULXU.W       R1,ER0          ;Lower 16 bit * lower 16 bit -> ER0
30  00101E  5231                        30              MULXU.W       R3,ER1          ;Lower 16 bit * upper 16 bit -> ER1
31  001020  52B2                        31              MULXU.W       E3,ER2          ;Upper 16 bit * lower 16 bit -> ER2
32  001022  52B3                        32              MULXU.W       E3,ER3          ;Upper 16 bit * upper 16 bit -> ER3
33  001024  0AA1                        33              ADD.L         ER2,ER1         ;
34  001026  58400002                    34              BCC           MULS3           ;
35  00102A  0B5B                        35              INC.W         #1,E3           ;
36  00102C  0918                        36    MULS3     ADD.W         R1,E0           ;
37  00102E  58400002                    37              BCC           MULS4           ;
38  001032  0B73                        38              INC.L         #1,ER3          ;
39  001034  0993                        39    MULS4     ADD.W         E1,R3           ;
40  001036  58400002                    40              BCC           MULS5           ;
41  00103A  0B5B                        41              INC.W         #1,E3           ;
42  00103C  737C                        42    MULS5     BTST          #7,R4L          ;
43  00103E  587000C                     43              BEQ           MULS6           ;
44  001042  1730                        44              NOT.L         ER0             ;
45  001044  1733                        45              NOT.L         ER3             ;
46  001046  0B70                        46              INC.L         #1,ER0          ;
47  001048  58600002                    47              BNE           MULS6           ;
48  00104C  0B73                        48              INC.L         #1,ER3          ;
49  00104E  5470                        49    MULS6     RTS                           ;
50                                      50              .END
***** TOTAL     ERRORS       0
***** TOTAL     WARNINGS     0
```

Note: The program listing included in this application note assumes compilation under the option for the advanced mode of H8/300H CPU. If you use this sample program with an H8/300H Tiny Series product, make the following change to the program code:
.CPU 300HA → .CPU 300HN

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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