SH7670 Group

DMAC Dual Address Mode

R01AN0304EJ0101
Rev. 1.01
Oct. 15, 2010

Summary

This application note provides an example of DMA transfer by means of the dual address mode of the direct memory access controller (DMAC) of the SH7670.

Target Device

SH7670 MCU

Contents

1. Introduction

1.1 Specifications

- DMA transfer from the on-chip RAM to external SDRAM is performed on DMAC channel 0 in dual address mode.
- Auto-request mode is used to request the DMAC to transfer five sets of 32-bit data (total 20 bytes).

1.2 Module Used

- Direct memory access controller (DMAC channel 0)

1.3 Applicable Conditions

MCU	SH7670
Operating Frequency	Internal clock: 200 MHz Bus clock: 66.6 MHz Peripheral clock: 33.3 MHz
Integrated Development Environment	Renesas Electronics High-performance Embedded Workshop Ver.4.03.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.01 Release 01
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7670 Group Example of Initialization
- SH7670 Group Using the DMAC to Transfer Data between Memory Areas
- SH7670 Group Using the DMAC to Transfer Data to On-chip Peripheral Modules

2. Description of the Sample Application

This sample program employs the direct memory access controller (DMAC) to perform DMA transfer from the on-chip RAM to external SDRAM in dual address mode.

2.1 Operational Overview of Module Used

In dual address mode, both the transfer source and destination are accessed (selected) by an address. The transfer source and destination can be located externally or internally. DMA transfer requires two bus cycles because data are read from the transfer source in a data read cycle and written to the transfer destination in a data write cycle. After the read cycle, the data for transfer are temporarily stored in the DMAC. For example in transfer between external memories, data are read to the DMAC from one region of external memory in a data read cycle, after which data are written to the other region of external memory in a data write cycle.

The flow of data in dual address mode is illustrated in figure 1. A block diagram of the DMAC is shown in figure 2. The settings of the DMAC are listed in table 1.

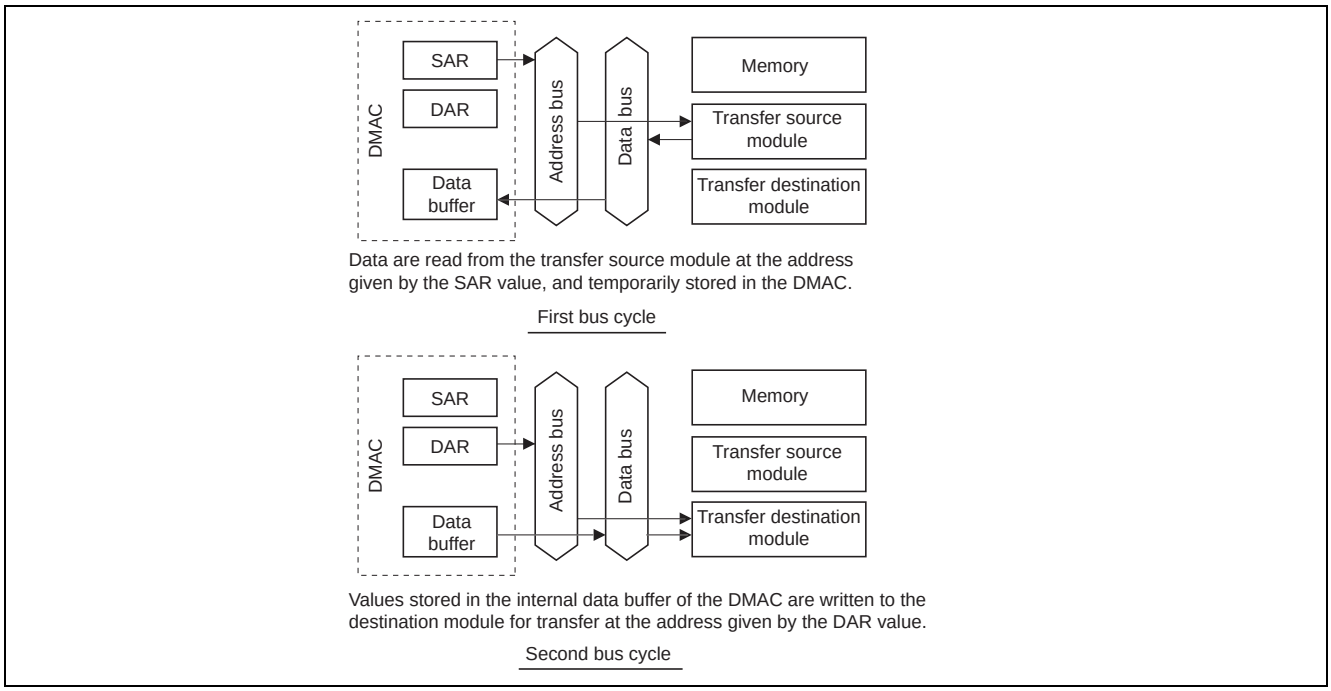
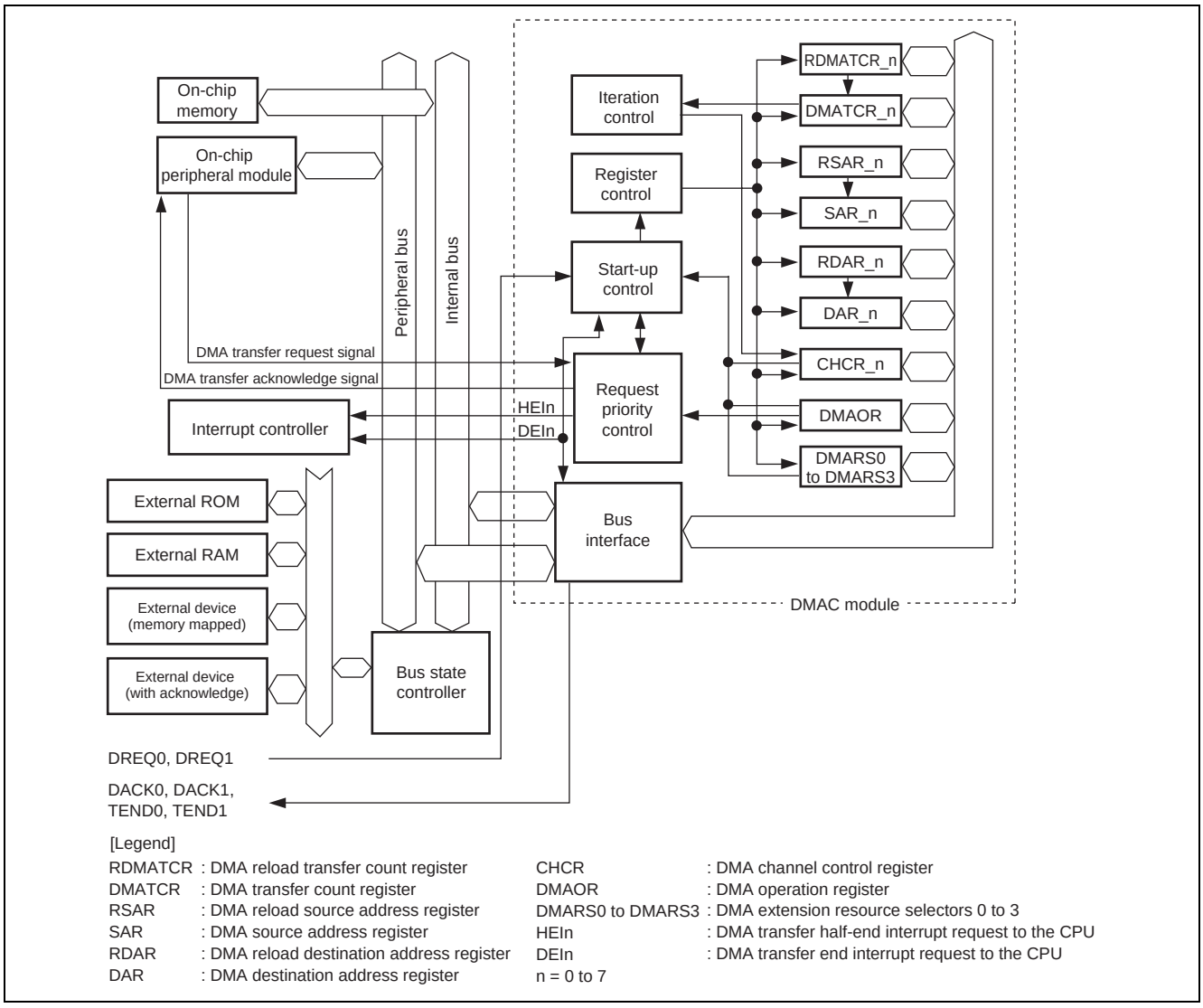


Figure 1 Flow of Data in Dual Address Mode

Table 1 Settings of DMAC

Item	Description
Address mode	Dual address
Transfer request	Auto request (transfer requests are made by software)
Number of unit transfers	5 (20 bytes of data in total are transferred)
Bus mode	Burst mode
Transfer source address	On-chip RAM (automatic incrementation according to the data size after each transfer)
Transfer destination address	SDRAM (H'2C00 1000) in the CS3 space (automatic incrementation according to the data size after each transfer)
Transfer data size	Longword (32 bits)
Interrupt	Transfer end interrupt enabled

Note: For details on the DMAC, refer to the section on the direct memory access controller (DMAC) in the *SH7670 Group Hardware Manual* (REJ09B0437).



[Legend]

RDMATCR	: DMA reload transfer count register	CHCR	: DMA channel control register
DMATCR	: DMA transfer count register	DMAOR	: DMA operation register
RSAR	: DMA reload source address register	DMARS0 to DMARS3	: DMA extension resource selectors 0 to 3
SAR	: DMA source address register	HEIn	: DMA transfer half-end interrupt request to the CPU
RDAR	: DMA reload destination address register	DEIn	: DMA transfer end interrupt request to the CPU
DAR	: DMA destination address register	n = 0 to 7	

Figure 2 Block Diagram of the DMAC

2.2 Procedure for Setting the Module Used

This section describes the procedure for specifying initial settings for operating the DMAC in dual address mode. Auto-request mode is used for requesting transfer. A flowchart of the DMAC initialization is shown in figure 3. For details on registers, refer to the *SH7670 Group Hardware Manual* (REJ09B0437).

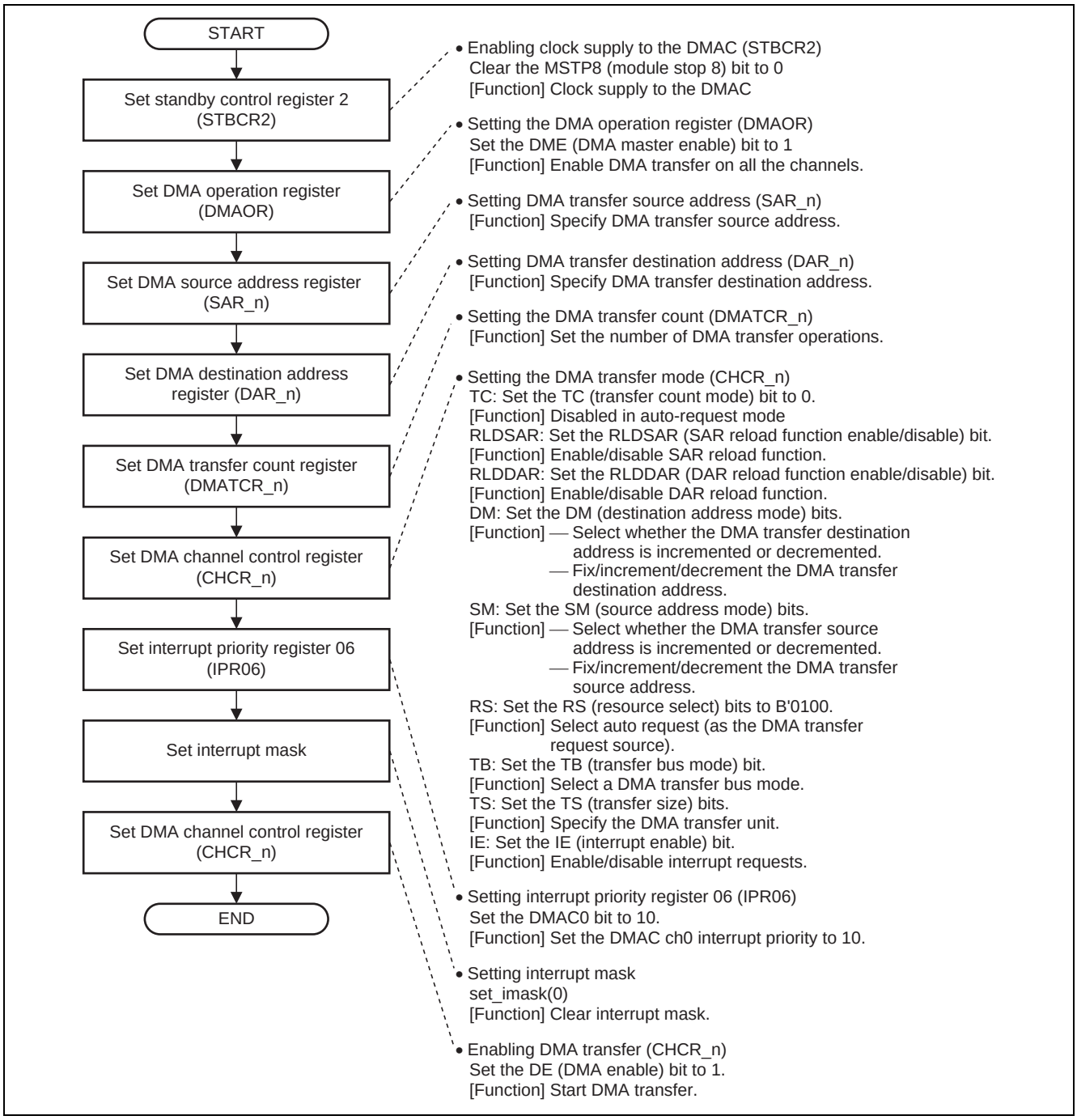


Figure 3 Example of Flow for Initialization of the DMAC

2.3 Operation of the Sample Program

The principle of operation in this sample task is illustrated in figure 4 and described in table 2.

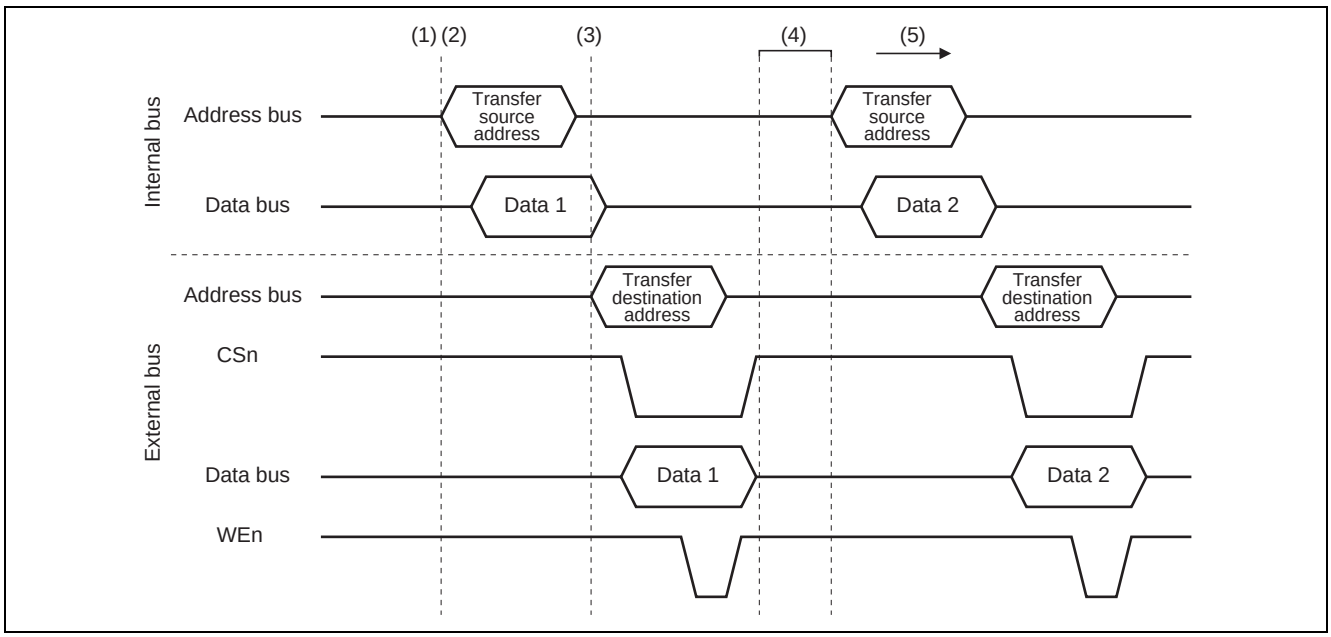


Figure 4 Operation in Dual Address Mode

Table 2 Processing

	Software Processing	Hardware Processing
(1)	Setting the DE bit in CHCR_0 to 1 after all the other settings have been specified. (DMAC0 starts operation)	Output of the transfer source address to the internal address bus
(2)	—	Output of data from the on-chip RAM to the internal data bus
(3)	—	Output of CSn and WEn signals, address, and data to the external bus
(4)	—	Incrementing of SAR_0 and DAR_0
(5)	—	Repeating until DMATCR_0 becomes 0

2.4 Notes on Using the Sample Program

In this sample program, addresses where the source and destination areas for transfer start are specified as absolute addresses for clarity. Ensure that sections used by the user program do not overlap with the source and destination regions that start from the absolute addresses.

2.5 Procedure for Processing by the Sample Program

In the sample program, DMA transfer of 20-byte data from the on-chip RAM to external SDRAM is performed, after which transfer end interrupt processing is performed to disable DMA transfer.

The register settings for the sample program are listed in table 3. Also, the flow of processing by the sample program is shown in figure 5.

Table 3 Register Settings for Sample Program

Register Name	Address	Setting	Description
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP8 = 0: DMAC operates
DMA channel control register_0 (CHCR_0)	H'FFFE 100C	H'0000 5474	TC = 0: Ineffective in auto-request mode RLDSAR = 0: Disables the SAR reload function RLDDAR = 0: Disables the DAR reload function DM = B'01: Increments the destination address SM = B'01: Increment the source address RS = B'0100: Auto request TB = 1: Burst mode TS = B'10: Longword transfer IE = 1: Enable interrupt requests
		H'0000 5475	DE = 1: Enable DMA transfer
		H'0000 5470	IE = 0: Disables interrupt requests TE = 0: Clears the transfer end flag DE = 0: Disables DMA transfer
DMA source address register_0 (SAR_0)	H'FFFE 1000	Address of transfer source data	Sets start address of transfer source in an on-chip RAM area.
DMA destination address register_0 (DAR_0)	H'FFFE 1004	H'2C00 1000	Sets start address of transfer destination in an external memory area*.
DMA transfer count register_0 (DMATCR_0)	H'FFFE 1008	H'05	Number of unit transfers: 5
DMA operation register (DMAOR)	H'FFFE 1200	H'0001	DME = 1: Enables DMA transfer on all channels
DMA extension resource selector0 (DMARS0)	H'FFFE 1300	H'0000	Not used for auto request

Note: * Addresses in external memory areas differ with the target board.

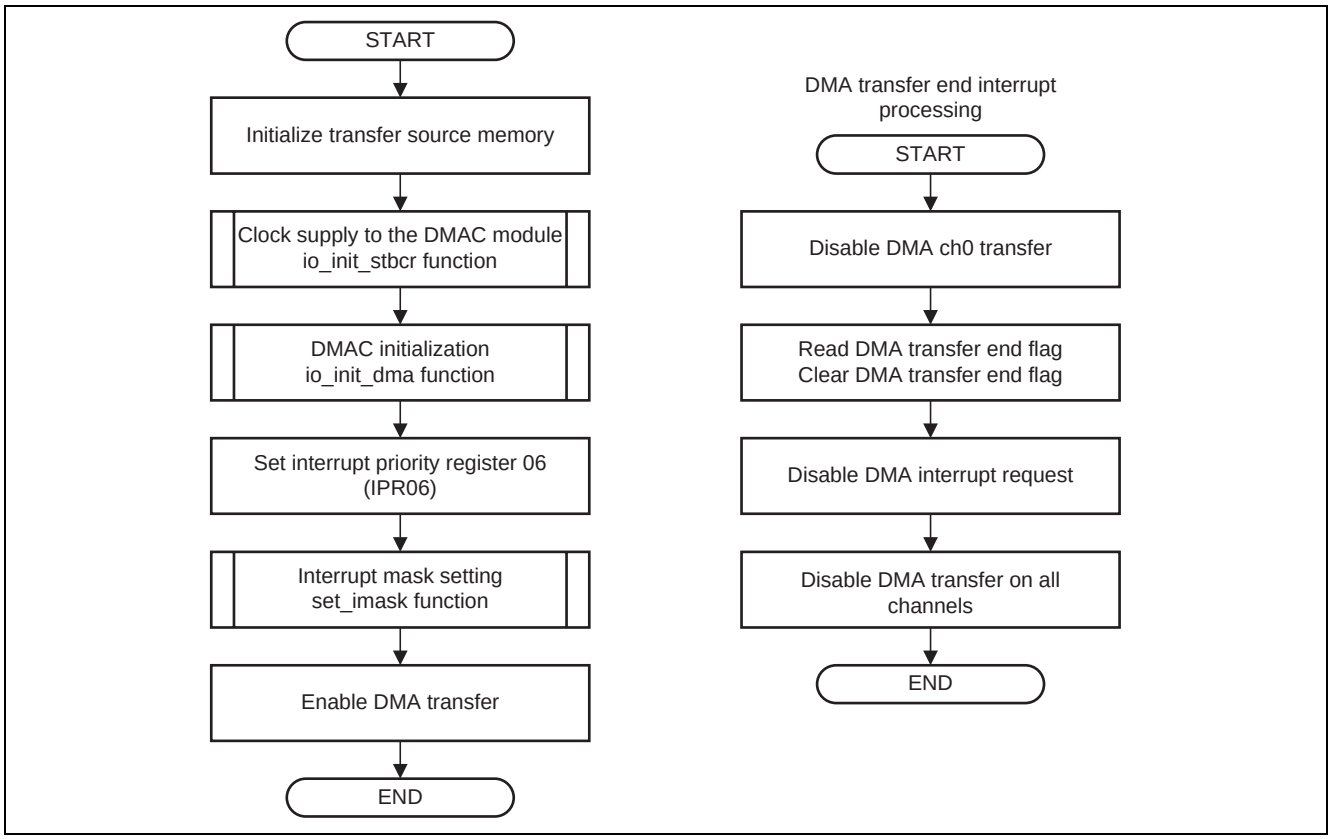


Figure 5 Flow of Processing by the Sample Program

3. Sample Program Listing

3.1 Sample program list "main.c" (1)

```
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27  ***********************************************************************
28  * Copyright (C) 2008(2010) Renesas Electronics Corporation. All rights reserved.
29  *""FILE COMMENT""*********** Technical reference data *************************
30  *   System Name : SH7671 Sample Program
31  *   File Name   : main.c
32  *   Abstract    : Sample program for DMAC in dual address mode
33  *   Version     : 1.00.01
34  *   Device      : SH7671
35  *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36  *               : C/C++ compiler package for the SuperH RISC engine family
37  *               :                               (Ver.9.01 Release01).
38  *   OS          : None
39  *   H/W Platform: M3A-HS71(CPU board)
40  *   Description :
41  ***********************************************************************
42  *   History     : Apr.24,2008 ver.1.00.00
43  *               : Oct.08,2010 ver.1.00.01 Changed the company name and device name
44  *""FILE COMMENT END""*****************************************************/
45  #include <machine.h>
46  #include "iodefine.h"              /* SH7670 iodefine  */
47
48  /* ==== prototype declaration ==== */
49  void main(void);
50  void io_init_stbcr(void);
51  void io_init_dma(unsigned long sar, unsigned long dar, unsigned long num);
52
```

3.2 Sample program list "main.c" (2)

```
53     /* ==== symbol definition ==== */
54     #define NUM 5
55     #define SDRAM_ADDR 0x2c001000ul     /* DMA source address (SDRAM) */
56
57     /* ==== RAM allocation variable declaration ==== */
58     unsigned long Data[NUM];
59
60     /*""FUNC COMMENT""*****************************************************************
61      * Outline      : Sample program main
62      *-------------------------------------------------------------------------------
63      * Include      : #include "iodefine.h"
64      *-------------------------------------------------------------------------------
65      * Declaration  : void main(void);
66      *-------------------------------------------------------------------------------
67      * Function     : Sample program main
68      *-------------------------------------------------------------------------------
69      * Argument     : void
70      *-------------------------------------------------------------------------------
71      * Return Value : none
72      *-------------------------------------------------------------------------------
73      * Notice       :
74      *""FUNC COMMENT END""*************************************************************/
75     void main(void)
76     {
77         /* ==== Transfer data set ==== */
78         Data[0] = 0x11111111ul;
79         Data[1] = 0x22222222ul;
80         Data[2] = 0x33333333ul;
81         Data[3] = 0x44444444ul;
82         Data[4] = 0x55555555ul;
83
84         /* ==== Setting of power down mode ==== */
85         io_init_stbcr();
86
87         /* ==== Setting of DMAC ==== */
88         io_init_dma((unsigned long)&Data[0], SDRAM_ADDR, NUM);
89
90         /* ==== interrupt priority register ==== */
91         INTC.IPR06.BIT._DMAC0 = 10u;
92
93         /* ==== clear the interrupt mask ==== */
94         set_imask(0);
95
96         /* ==== DMA transfer start ==== */
97         DMAC.CHCR0.BIT.DE = 1ul;
98
99         while(1){
100            /* loop */
101        }
102    }
103
```

3.3 Sample program list "main.c" (3)

```
104    /*""FUNC COMMENT""*****************************************************************
105     * Outline      : Existing moduel standby mode
106     *-------------------------------------------------------------------------------
107     * Include      : #include "iodefine.h"
108     *-------------------------------------------------------------------------------
109     * Declaration  : void io_init_stbcr(void);
110     *-------------------------------------------------------------------------------
111     * Function     : Existing module standby mode
112     *-------------------------------------------------------------------------------
113     * Argument     : void
114     *-------------------------------------------------------------------------------
115     * Return Value : none
116     *-------------------------------------------------------------------------------
117     * Notice       :
118     *""FUNC COMMENT END""*************************************************************/
119    void io_init_stbcr(void)
120    {
121        /* ==== Setting of power down mode ==== */
122        CPG.STBCR2.BIT.MSTP8 = 0u;      /* Clear the DMAC module standby mode */
123    }
124
125    /*""FUNC COMMENT""*****************************************************************
126     * Outline      : DMAC setting
127     *-------------------------------------------------------------------------------
128     * Include      : #include "iodefine.h"
129     *-------------------------------------------------------------------------------
130     * Declaration  : void io_init_dma(unsigned long sar, unsigned long dar,
131     *              :                  unsigned long num);
132     *-------------------------------------------------------------------------------
133     * Function     : DMAC setting
134     *-------------------------------------------------------------------------------
135     * Argument     : unsigned long sar ; transfer source address
136     *              : unsigned long dar ; transfer destination address
137     *              : unsigned long num ; number of unit transfers
138     *-------------------------------------------------------------------------------
139     * Return Value : none
140     *-------------------------------------------------------------------------------
141     * Notice       :
142     *""FUNC COMMENT END""*************************************************************/
```

3.4 Sample program list "main.c" (4)

```
143    void io_init_dma(unsigned long sar, unsigned long dar, unsigned long num)
144    {
145
146        /* ==== Setting of DMAC ==== */
147        /* ---- DMA operation register (DMAOR) ---- */
148        DMAC.DMAOR.BIT.DME = 1u;            /* DMA master enable */
149
150        /* ---- DMA source address registers (SAR) ---- */
151        DMAC.SAR0 = sar;                    /* DMA source address */
152        /* ---- DMA Destination Address Registers (DAR) ---- */
153        DMAC.DAR0 = dar;                    /* DMA destination address */
154        /* ---- DMA transfer count registers (DMATCR) ---- */
155        DMAC.DMATCR0 = num;                 /* DMA transfer count */
156
157        /* ---- DMA channel control registers (CHCR) ---- */
158        DMAC.CHCR0.LONG = 0x00005474ul;
159                /*
160                   bit31    : TC : 0 ---------------------  Disabled in auto-request mode
161                   bit30    : reserve 0
162                   bit29    : RLDSAR OFF : 0 -------------  SAR reload function is disabled.
163                   bit28    : RLDDAR OFF : 0 -------------  DAR reload function is disabled.
164                   bit27-24 : reserve 0
165                   bit23    : DO over run 0 : 0 ----------  Not in use
166                   bit22    : TL TEND low active : 0 -----  Not in use
167                   bit21    : reserve 0
168                   bit20    : TEMASK : TE set mask : 0 ---  When the TE bit is set, DMA
       transfer is halted
169                   bit19    : HE : 0 ---------------------  Not in use
170                   bit18    : HIE : 0 --------------------  Not in use
171                   bit17    : AM : 0 ---------------------  Not in use
172                   bit16    : AL : 0 ---------------------  Not in use
173                   bit15-14 : DM1:0 DM0:1 ----------------  Destination address is incremented.
174                   bit13-12 : SM1:0 SM0:1 ----------------  Source address is incremented.
175                   bit11-8  : RS : auto request : B'0100 -  Auto request
176                   bit7     : DL : DREQ level : 0 --------  Not in use
177                   bit6     : DS : DREQ select : 1 -------  Falling edge is detected.
178                   bit5     : TB : cycle : 1 -------------  Burst mode
179                   bit4-3   : TS : transfer size : B'10 --  Transfer in units of longword
180                   bit2     : IE : interrupt enable : 1 --  An interrupt request is enabled.
181                   bit1     : TE : transfer end ----------  The TE flag is cleared.
182                   bit0     : DE : DMA enable bit : 0 ----  DMA transfer is disabled.
183                */
184
185    }
186
```

3.5 Sample program list "main.c" (5)

```
187    /*""FUNC COMMENT""*****************************************************************
188     * Outline      : DMA transfer end interrupt
189     *-------------------------------------------------------------------------------
190     * Include      : #include "iodefine.h"
191     *-------------------------------------------------------------------------------
192     * Declaration  : void io_int_dma(void);
193     *-------------------------------------------------------------------------------
194     * Function     : 1. Disabling DMA transfer
195     *              : 2. Clearing the transfer end flag
196     *              : 3. Disabling interrupt requests
197     *              : 4. Disabling DMA transfer on all channels
198     *              : 5. Dummy reading
199     *-------------------------------------------------------------------------------
200     * Argument     : void
201     *-------------------------------------------------------------------------------
202     * Return Value : none
203     *-------------------------------------------------------------------------------
204     * Notice       :
205     *""FUNC COMMENT END""*************************************************************/
206    void io_int_dma(void)
207    {
208        volatile unsigned long dummy;
209
210        DMAC.CHCR0.BIT.DE = 0x00ul;         /* Clear the DE bit */
211
212        DMAC.CHCR0.BIT.TE = 0x00ul;         /* Clear the TE bit */
213
214        DMAC.CHCR0.BIT.IE = 0x00ul;         /* Clear the IE bit */
215
216        DMAC.DMAOR.BIT.DME = 0x00u;         /* DMA master disable */
217
218        dummy = DMAC.CHCR0.BIT.TE;
219    }
220
221    /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7670 Group Hardware Manual Rev. 2.00
  The latest version of the hardware user's manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Nov.19.08	—	First edition issued
1.01	Oct.15.10	—	Changed the sample program (AC Switching Characteristics are removed)

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   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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