SH7263/SH7203 Group

I^2C Bus Interface 3

Dummy Clock Transmission in Communication Failure

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Abstract

In I^2C communications, the slave device may fix the SDA pin to “L” due to a noise and others, which disturbs communications. For recovery, inputting clock to the slave using the measure other than I^2C communication is required.

This application note gives information on how to input clock to the slave using the clocked synchronous serial format of the I^2C bus interface 3 (hereinafter called IIC3).

Products

SH7263/SH7203 (hereinafter called as “SH7263”)

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Operate the SH7263 in IIC3 master mode. Connect the EEPROM to the slave, then perform a 10-byte data read. When a hang-up is caused to the IIC3 by EEPROM bus occupation, transmit a dummy clock to recover from the failure and restart the data read.

When an 8-bit dummy clock is input to the EEPROM that is occupying the bus, the EEPROM will transit to the state that received the NACK from the master device, and releases the bus. In the sample code, the same process is followed; an 8-bit clock is transmitted as a dummy clock.

For the dummy clock transmission, use the IIC3 clocked synchronous serial format since the PB6/SDA pin on the SH7263 cannot be set to the output port.

Table 1.1 shows the peripheral function and its application. Figure 1.1 shows an example of the flow till a bus occupation failure is caused by the slave.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
I²C bus interface 3	• I²C bus format Access to the EEPROM • Clocked synchronous serial format Dummy clock transmission

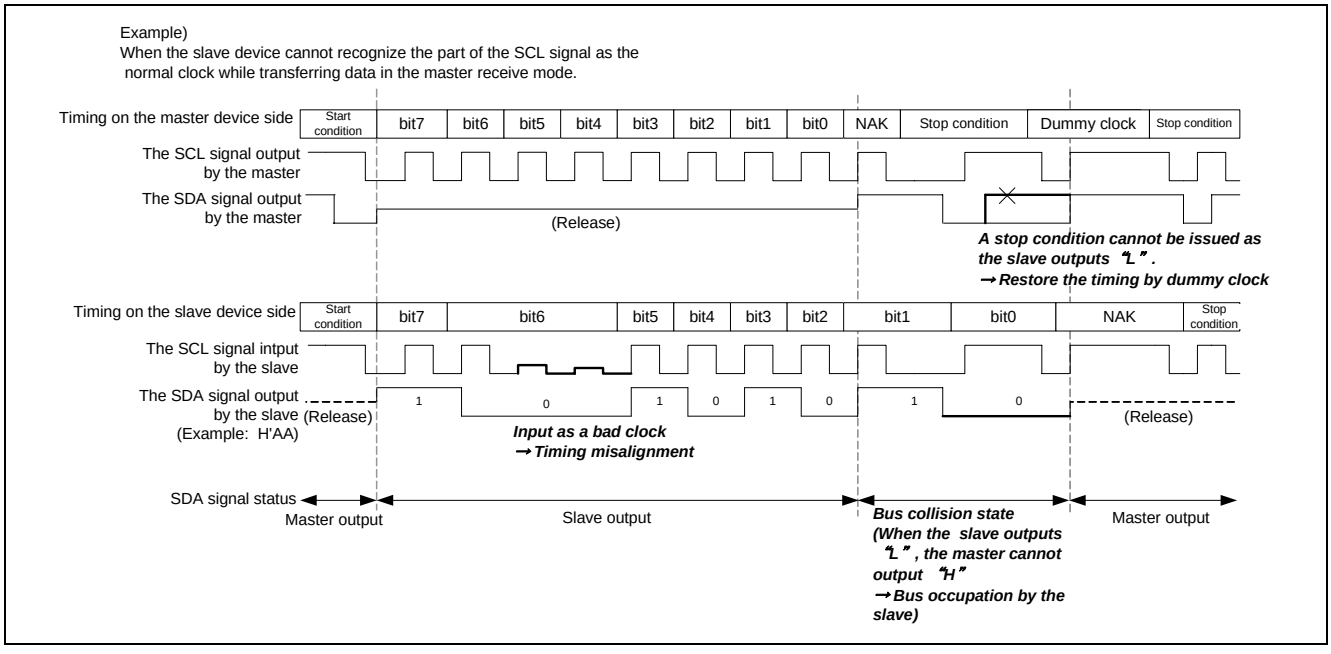

Figure 1.1 Flow till Bus Occupation Failure Occurred by the Slave (Example)

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH7263
Device used	Renesas Electronics Corporation EEPROM Model: R1EX24128ASA00A
Operating frequency	• CPU internal clock (Iϕ): 200MHz • Internal clock (Bϕ): 66.66MHz • Peripheral clock (Pϕ): 33.33MHz
Operating voltage	• Source power (I/O): 3.3V • Source power (internal): 1.2V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.03.00
C compiler	Renesas Electronics Corporation SuperH RISC engine FamilyC/C++ Compiler Package Ver.9.01 Release01
	Complier option -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Sample code version	2.00

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- SH7263/SH7203Group Reception by the I2C Bus Interface 3 Module in Single-Master Operation (EEPROM Reading) (document No.: REJ06B0838)

4. Peripheral Functions

This section gives the precautions for the IIC3 and the supplemental information on the receive setting for the clocked synchronous serial format used in the sample code. For the basic information, refer to the SH7263 Group Hardware Manual.

4.1 Clocked Synchronous Serial Format

Figure 4.1 shows the setting for the clocked synchronous serial format in master receive mode.

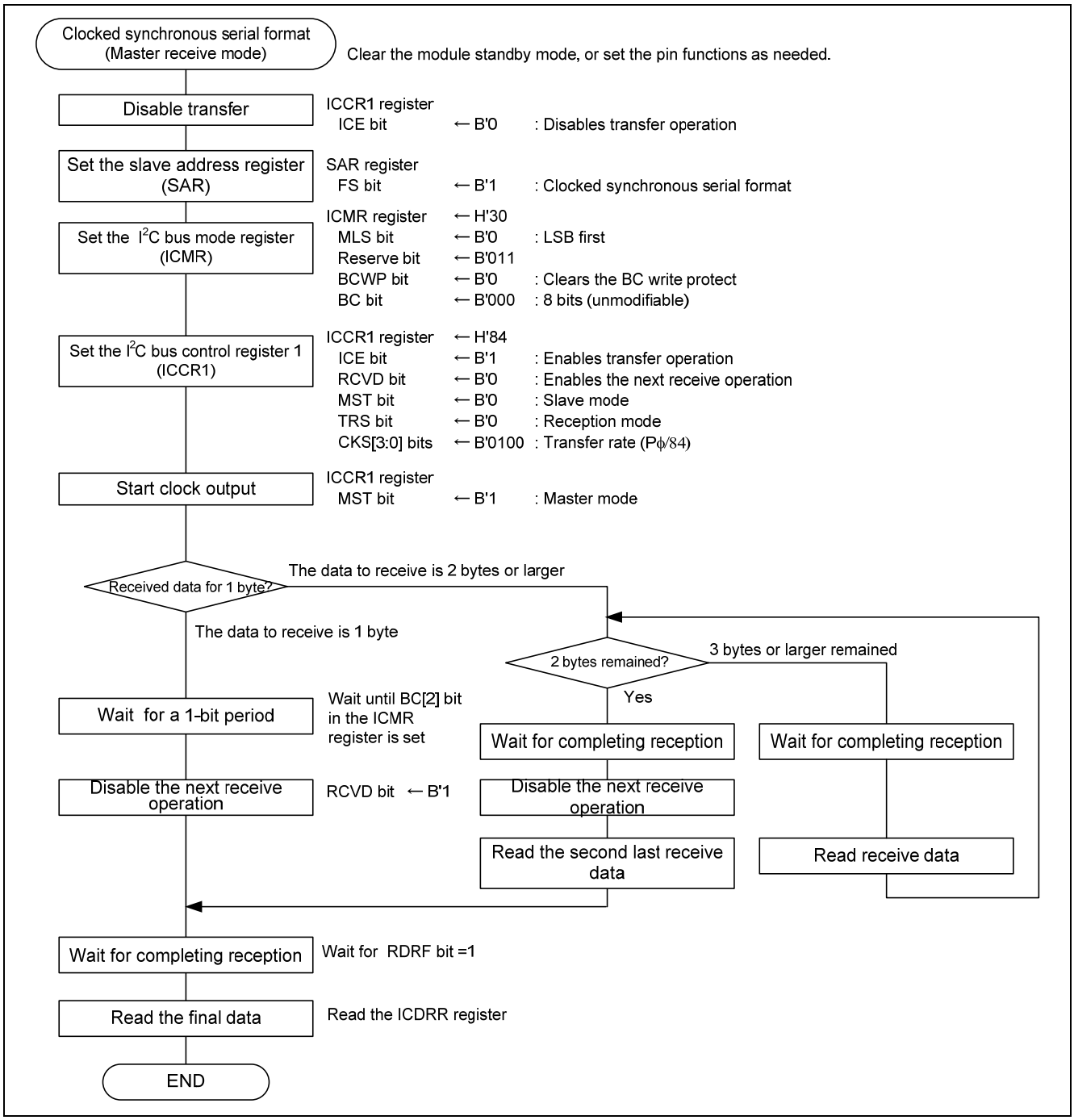

Figure 4.1 Setting Master Receive Mode in Clocked Synchronous Serial Format (Example)

4.2 Note on Master Receive Mode

Reading the I²C bus receive data register (ICDRR) around the falling edge of the 8th clock may fail to fetch the receive data.

In addition, when the receive disable bit (RCVD) in the I²C bus controller register is set to 1 around the falling edge of the 8th clock and the receive buffer is full, a stop condition may not be issued. Use either 1 or 2 below against the situations above.

1. In master receive mode, read the ICDRR before the rising edge of the 8th clock.
2. In master receive mode, set the RCVD bit to so that transfer proceeds in byte unit.

In the sample program, the RCVD is set to 1 and communication is performed in byte unit.

4.3 Note on Setting ACKBT in Master Receive Mode

In master receive mode operation, set ACKBT bit before the falling edge of the 8th SCL cycle of the final data on consecutive data transfer. Otherwise, an overrun may occur on the slave transmit device.

In the sample program, the RCVD is set to 1 and the communication is performed in byte unit, which does not apply to the above described case.

4.4 Note on Issuing A Stop Condition or Re-transmitting A Start Condition in Master Receive Mode

When the timing for issuing a stop condition or a retransmit start condition overlaps with the timing of the fall of the 9th clock of SCL, an extra one-clock SCL will be output after the 9th clock. Issue a stop condition or retransmit start condition after confirming the fall of the 9th clock of the SCL.

The following is how to confirm the fall of the 9th clock.

- After reading that the RDRF bit (receive data register full flag) in the ICSR register becomes 1, read the SCLO bit (SCL monitor flag) in the ICCR2 register becomes 0 (the SCL pin is “L”).

For the details on this item, refer to Renesas Technical Update (No.: TN-MC*-A020A/E).

4.5 Note on Using the IICRST

While the I²C bus is operating writing 0 to the ICE bit in the ICCR1 register or writing 1 to the IICRST bit in the ICCR2 register leads the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register undefined.

For the details on this item, refer to Renesas Technical Update (No.: TN-MC*-A022A/E).

4.6 Note on Issuing A Stop Condition in Master Transmit Mode

When issuing a stop condition in master transmit mode with the ACKE bit =1 in the I²C bus interrupt enable register (ICIER), the stop condition may not be output normally depending on the timing of issuance.

For the details on this item, refer to Renesas Technical Update (No.: TN-MC*-A023A/E).

5. Hardware

5.1 Used Pins and the Pin Functions

Table 5.1 lists the pins used and the pin functions.

Table 5.1 Used Pins and Pin Functions

Pin name	Input/output	Function
PB6/SCL3	Output	Clock output in the I²C communications
PB7/SDA3	Output/Input	Data input/output in the I²C communications

5.2 Hardware Configuration

Figure 5.1 shows the configuration diagram of SH7263 connecting the EEPROM.

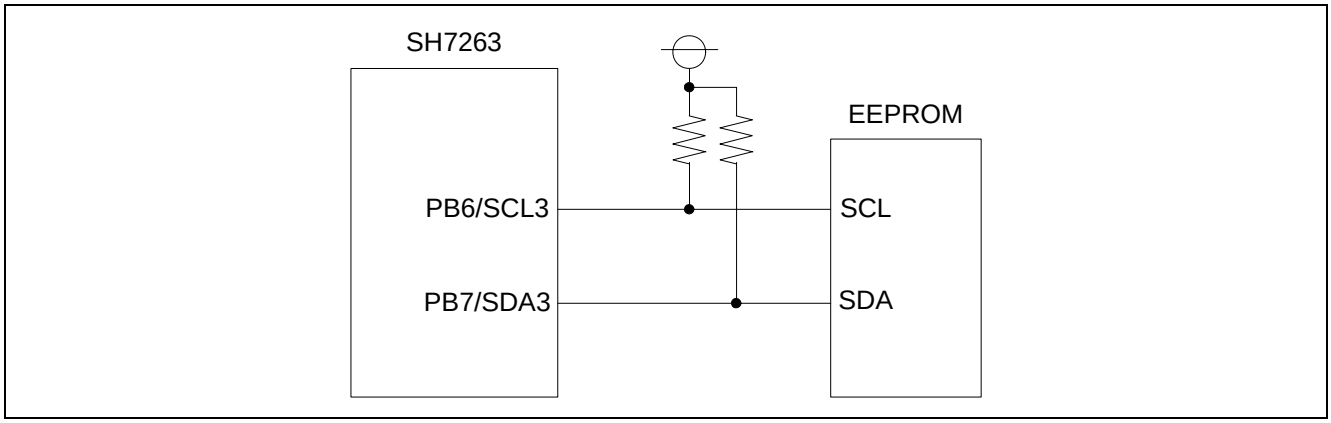

Figure 5.1 Configuration Diagram

6. Software

6.1 Operation Overview

In the sample code, IIC3 is set to master mode to execute the sequential read to the EEPROM for 10 bytes. For data transmission and reception, the I²C bus format is used. When the I²C communication is disturbed by the bus occupation in the slave device, switch the IIC3 to the clocked synchronous format to transmit a dummy clock until the bus is released. After the bus is released, the sequential read is carried out again using the I²C bus format.

6.1.1 Sequential Read Operation

Figure 6.1 shows the EEPROM sequential read.

For the device code and the device address, refer to the EEPROM data sheet. In the sample code, "B'1010" is employed as the device code, and "B'000" as the device address.

The memory address indicates the start address for reading the EEPROM. The address is incremented on the EEPROM side each time the data is read.

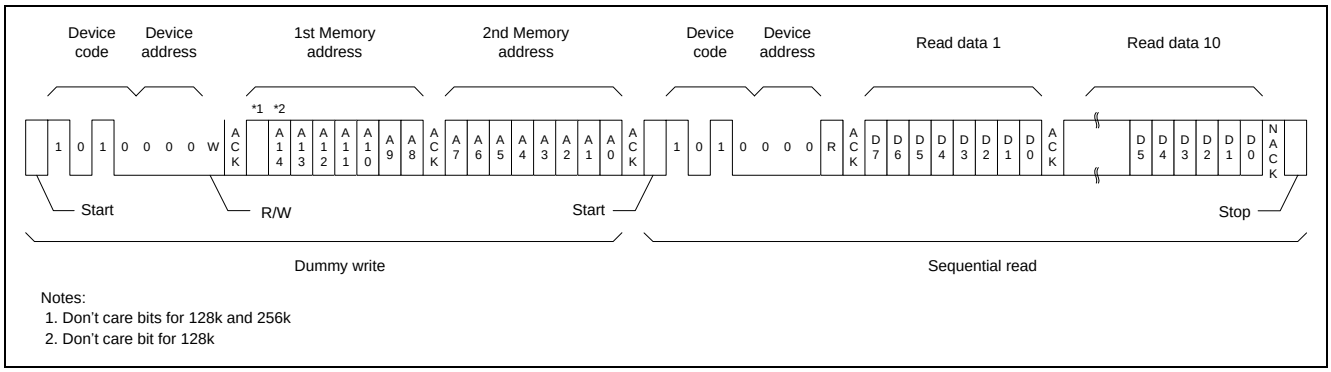

Figure 6.1 EEPROM Sequential Read

6.1.2 Detection of Bus Occupation

In the sample code, the bus occupation by the slave device is monitored during the I²C communications. The bus occupation is determined after a certain period of standby for a cancellation in the following two events.

- Wait for completing transmission in master transmit mode (wait for the TEND bit setting).
- Wait for completing an issuance of a stop condition in master transmit mode or master receive mode (wait for the STOP bit setting).

6.1.3 Procedure of Bus Cancellation

Use the master receive mode in the clocked synchronous serial format. Set the MST bit and the master receive mode, and the clock is transmitted automatically. When the slave device releases the bus, the SDA pin becomes H. When detecting that the SDA pin becomes H, stop the clock. For details on the procedure, refer to Figure 6.9 Function for Recovery from Bus Occupation State.

In the sample code, the sequential read is restarted after issuing a stop condition. For the recovery measure, refer to the specification of the slave device.

6.2 File Composition

Table 6.1 lists the file used in the sample code. Files generated by the integrated development environment should not be listed in this table.

Table 6.1 File Composition

File Name	Outline	Remarks
main.c	Main processing function EEPROM operation function IIC3 control function	

6.3 Constants

Table 6.2 lists the constants used in the sample code.

Table 6.2 Constants in the Sample Code

Constant Name	Setting Value	Description
EEPROM_MEM_ADDR	0x0000	Start address of the EEPROM
DEVICE_CODE	0xA0	Device code of the EEPROM
DEVICE_ADDR	0x00	Device address of the EEPROM
IIC_DATA_WR	0x00	Data write code
IIC_DATA_RD	0x01	Data read code
IIC3_DATA	10	Data transfer size in bytes
E_OK	0	Normal end
E_ERR_ACK	-1	NAK reception error
E_ERR_BUS	-2	Detects bus occupation failures
E_ERR_FATAL	-3	Detects fatal errors

6.4 Variables

Table 6.3 lists the global variable used in the sample code.

Table 6.3 Global Variables

Form	Constant	Description	Functions used
unsigned char	ReadData[IIC3_DATA]	Storage area for read data	main

6.5 Functions

Table 6.4 lists the functions used in the sample code.

Table 6.4 Functions

Function	Description
main	Main processing
io_iic3_init	Initializes the IIC3 module
io_iic3_eeprom_read	Reads data from the EEPROM
io_iic3_data_receive	Master receive mode
io_iic3_address_send	Transmits the slave device address
io_iic3_data_send	Transmits data for one byte
io_iic3_mst_send_end	Issues a stop condition
io_iic3_bus_recovery	Recovers from the bus occupation state

6.6 Function Specifications

The following tables list the function specifications in the sample code.

main

Outline	Main processing
Header	None
Declaration	void main(void);
Description	Initializes the IIC3 and reads data for 10 bytes from the EEPROM. In case that the bus occupation failure occurs, issues a dummy clock to recover from the failure. Repeats data read till the processing ends normally.
Argument	None
Returned value	None

io_iic3_init

Outline	Initializes the IIC3 module
Header	None
Declaration	void io_iic3_init(void)
Description	Initializes the IIC3 channel 3.
Argument	None
Returned value	None

io_iic3_eeprom_read

Outline	Reads data from the EEPROM
Header	None
Declaration	int io_iic3_eeprom_read(unsigned char d_code, unsigned char d_adr, unsigned short r_adr, unsigned int r_size, unsigned char *r_buf)
Description	Reads data for *r_size* byte from the EEPROM specified by the device code *d_code* and the device address *d_adr*. Stores the read data to the area specified by *r_bur*. The memory address for the EEPROM is specified by *tr_adr*.
Argument	unsigned char d_code : Device code unsigned char d_adr : Device address unsigned short r_adr : Address at read destination unsigned int r_size : Byte count to read unsigned char *r_buf : Storage address for the read data
Returned value	E_OK : Normal end E_ERR_ACK: NAK reception error E_ERR_BUS: Detects a bus occupation failure

io_iic3_data_receive

Outline	Master receive mode
Header	None
Declaration	int io_iic3_data_receive(unsigned char *r_buf, unsigned int r_size)
Description	Sets to master receive mode, receives for the byte counts specified by *r_size*, and stores the received data to *r_buf*. After receiving the specified byte counts, switches the mode to slave receive mode.
Argument	unsigned int r_size : Storage for the read data unsigned char *r_buf : Data size for the read data
Returned value	E_OK : Normal end E_ERR_BUS: Detects a bus occupation failure

io_iic3_address_send

Outline	Transmits the slave device address
Header	None
Declaration	int io_iic3_address_send(unsigned char *data)
Description	Transmits the one-byte slave device address and 2-byte memory address specified by *data*.
Argument	unsigned char *data : Address for transmit data
Returned value	E_OK : Normal end E_ERR_ACK: NAK reception error E_ERR_BUS: Detects a bus occupation failure

io_iic3_data_send

Outline	Transmits data for one byte
Header	None
Declaration	int io_iic3_data_send(unsigned char data)
Description	Transmits data on the procedure below. 1. Waits for ICDRT empty 2. Sets the transmit data 3. Confirms transmission completed 4. Confirms ACK response
Argument	unsigned char data : Transmit data
Returned value	E_OK : Normal end E_ERR_ACK: NAK reception error E_ERR_BUS: Detects a bus occupation failure

io_iic3_mst_send_end

Outline	Issues a stop condition
Header	None
Declaration	int io_iic3_mst_send_end(void)
Description	Issues a stop condition, and switches to the slave receive mode.
Argument	None
Returned value	E_OK : Normal end E_ERR_ACK: NAK reception error E_ERR_BUS: Detects a bus occupation failure

io_iic3_bus_recovery

Outline	Recovers from the bus occupation state
Header	None
Declaration	int io_iic3_bus_recovery(void)
Description	Transmits the 8-bit dummy clock in the master receive mode with the clocked synchronous serial format. After transmitting the dummy clock, and if the SDA pin H is not detected, returns an error.
Argument	None
Returned value	E_OK : Normal end E_ERR_FATAL: Fatal error

6.7 Flowchart

This section describes the processing procedure of the major functions used in the sample code. The words in boldface in the figures indicate the processing related to the bus occupation failure and recovery from the failure.

6.7.1 Main Function

Figure 6.2 shows the procedure of the main function.

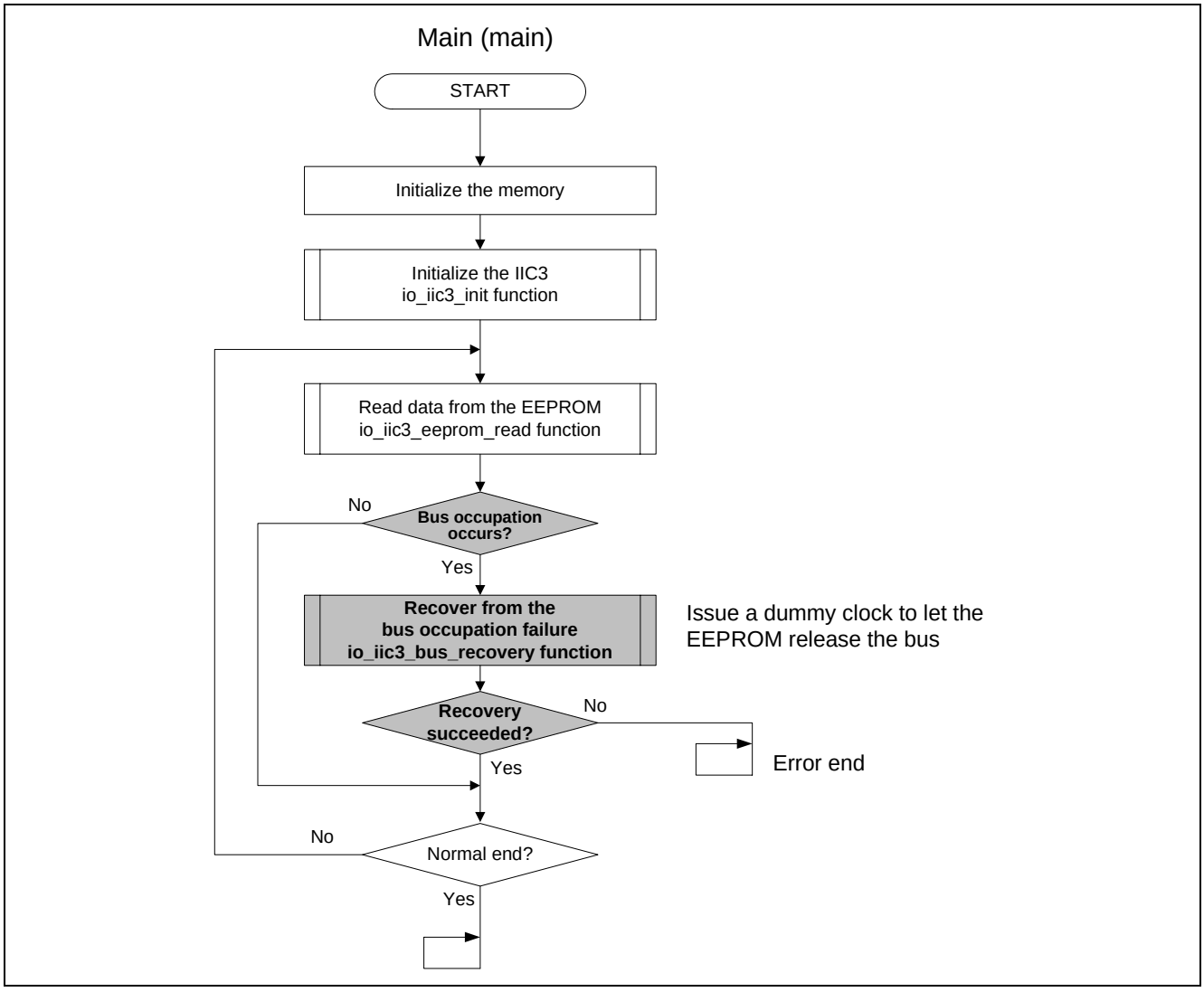

Figure 6.2 Main Function

6.7.2 IIC3 Module Initialization

Figure 6.3 shows the procedure of the function for initializing the IIC3 module.

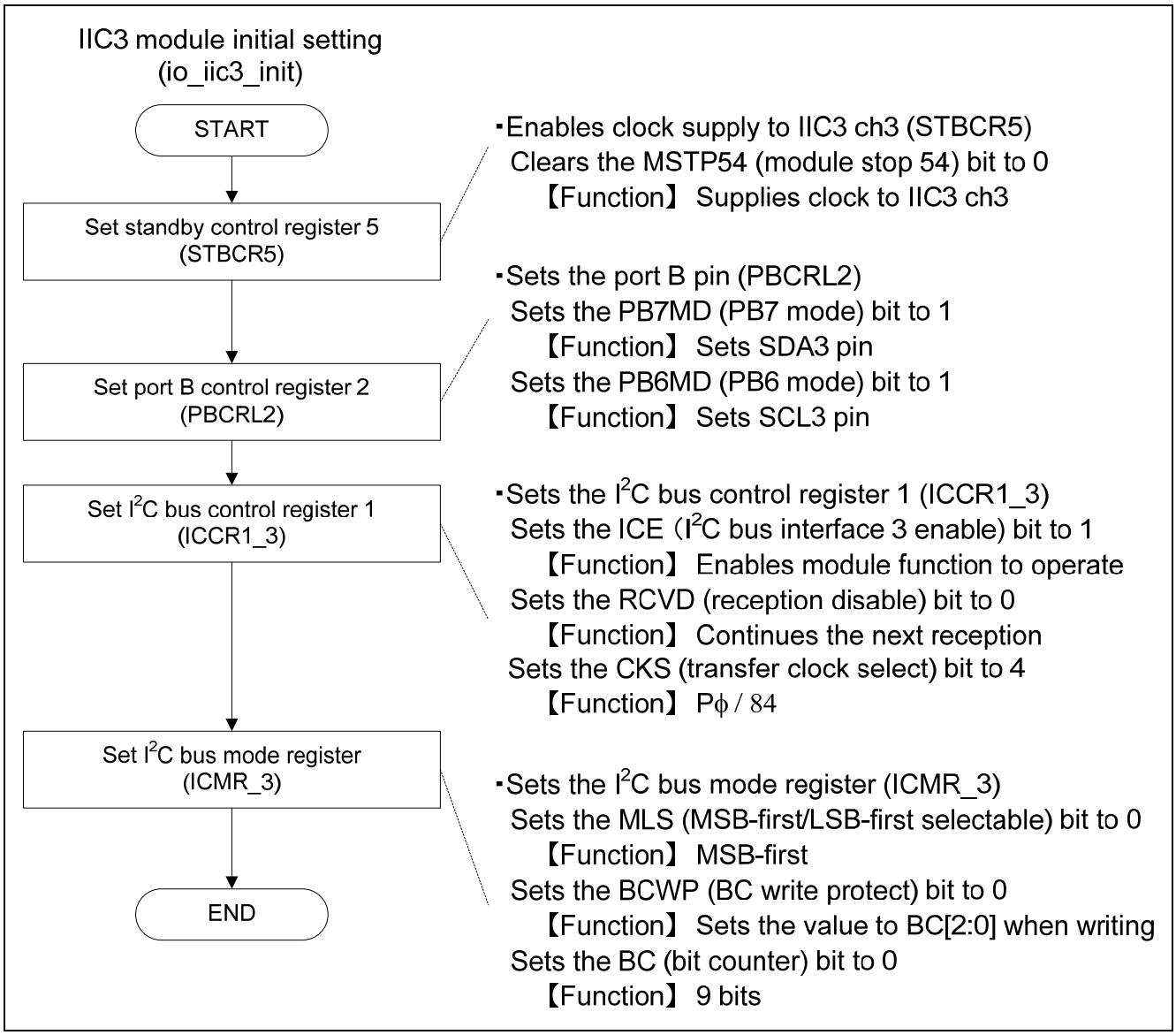

Figure 6.3 IIC3 Module Initialization

6.7.3 Function for Data Read from the EEPROM

Figure 6.4 shows the procedure of the function for data read from the EEPROM.

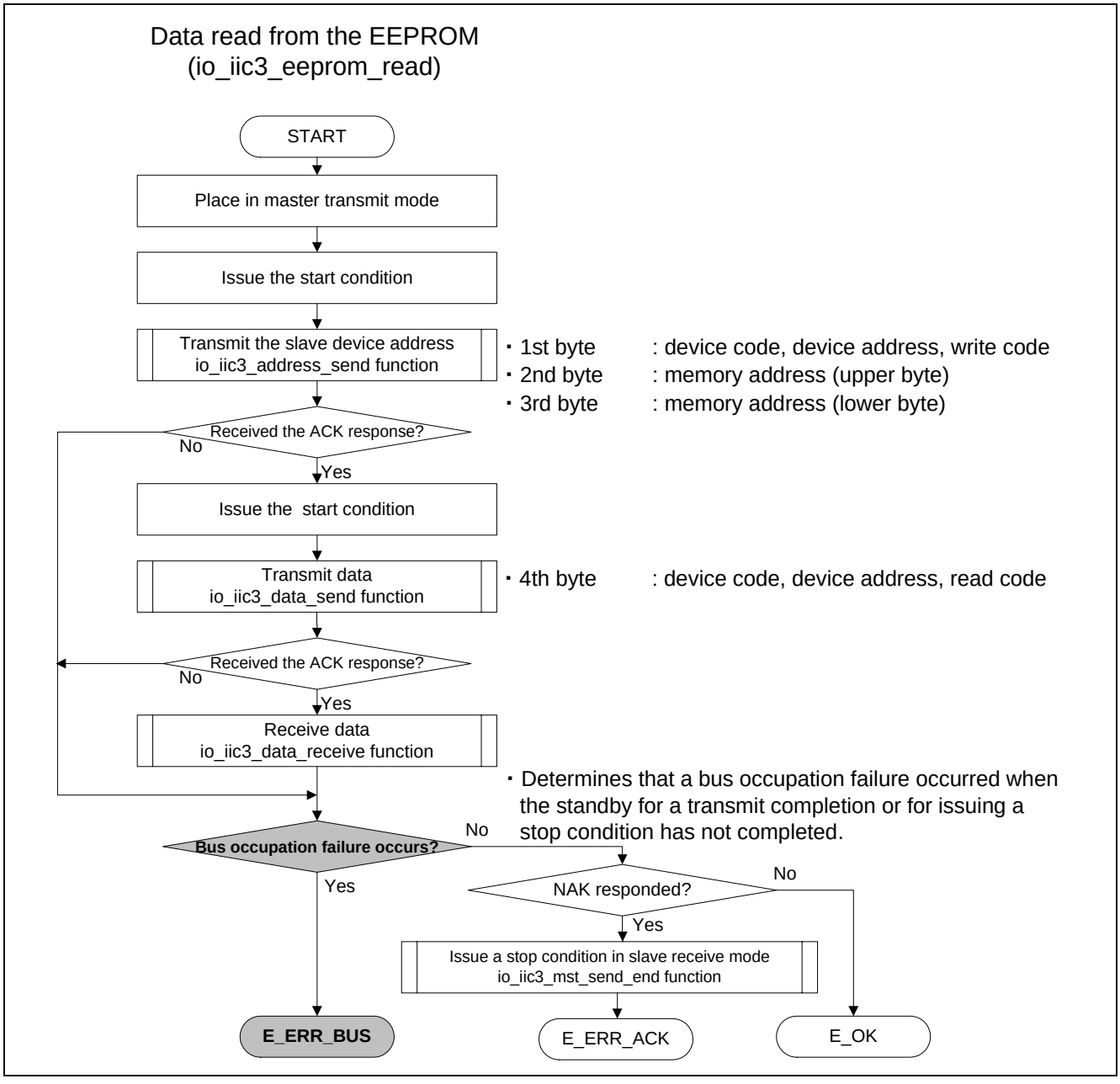

Figure 6.4 Function for Data Read from EEPROM

6.7.4 Function for Data Read

Figure 6.5 and Figure 6.6 show the procedure of the function for data read.

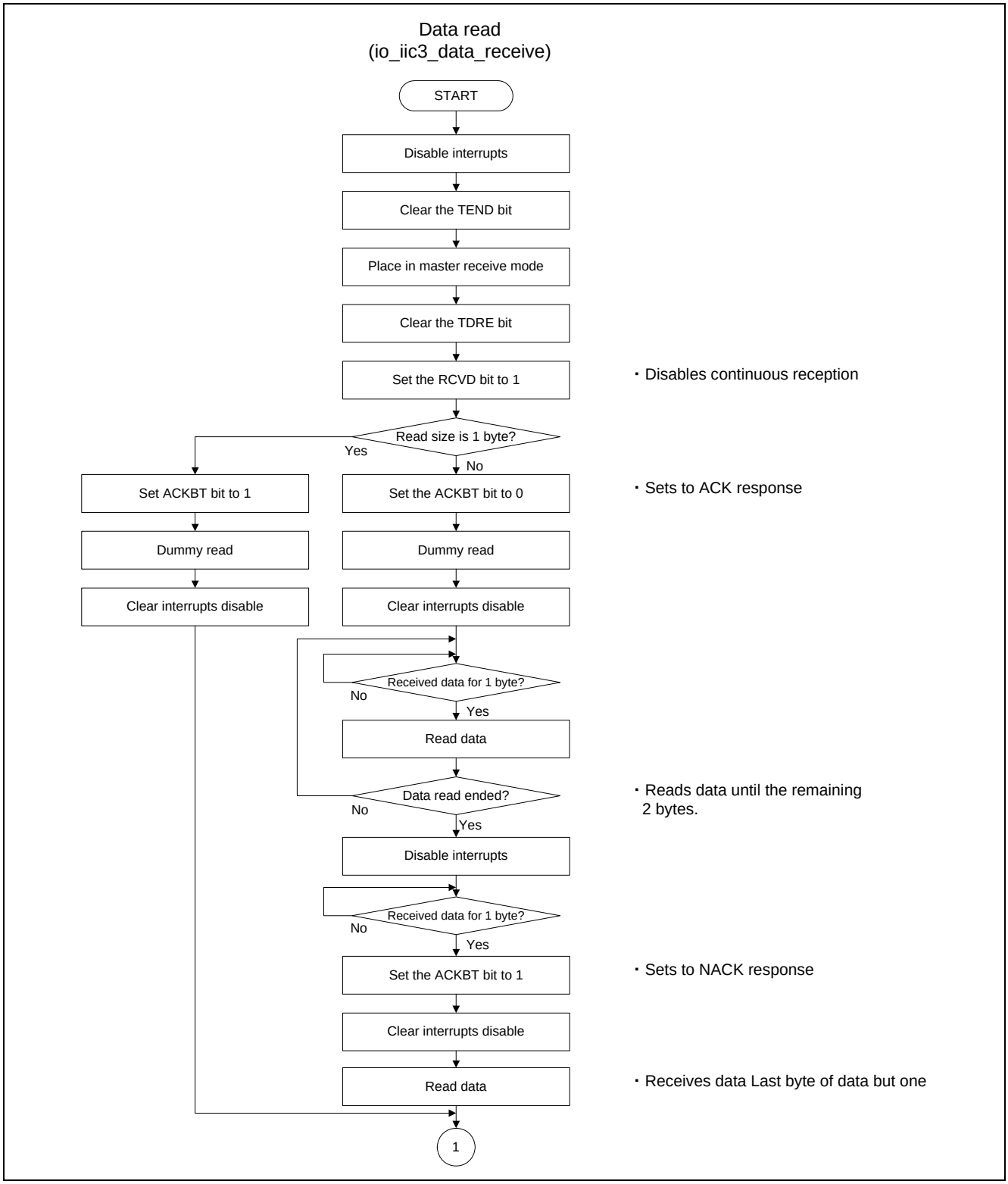

Figure 6.5 Function for Data Read

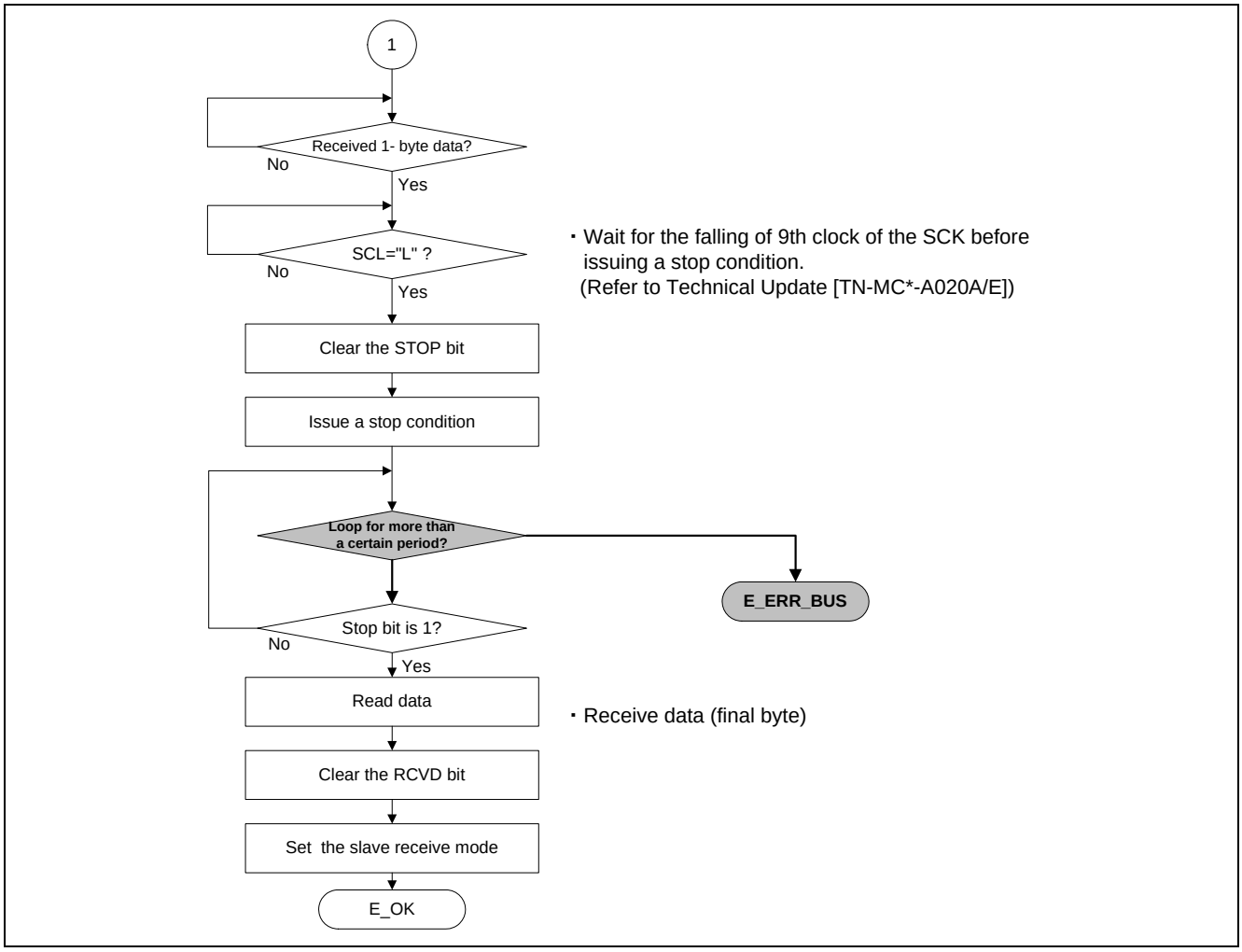

Figure 6.6 Function for Data Read

6.7.5 Function for Transmitting Slave Device Address

Figure 6.7 shows the procedure of the function for transmitting the slave device address.

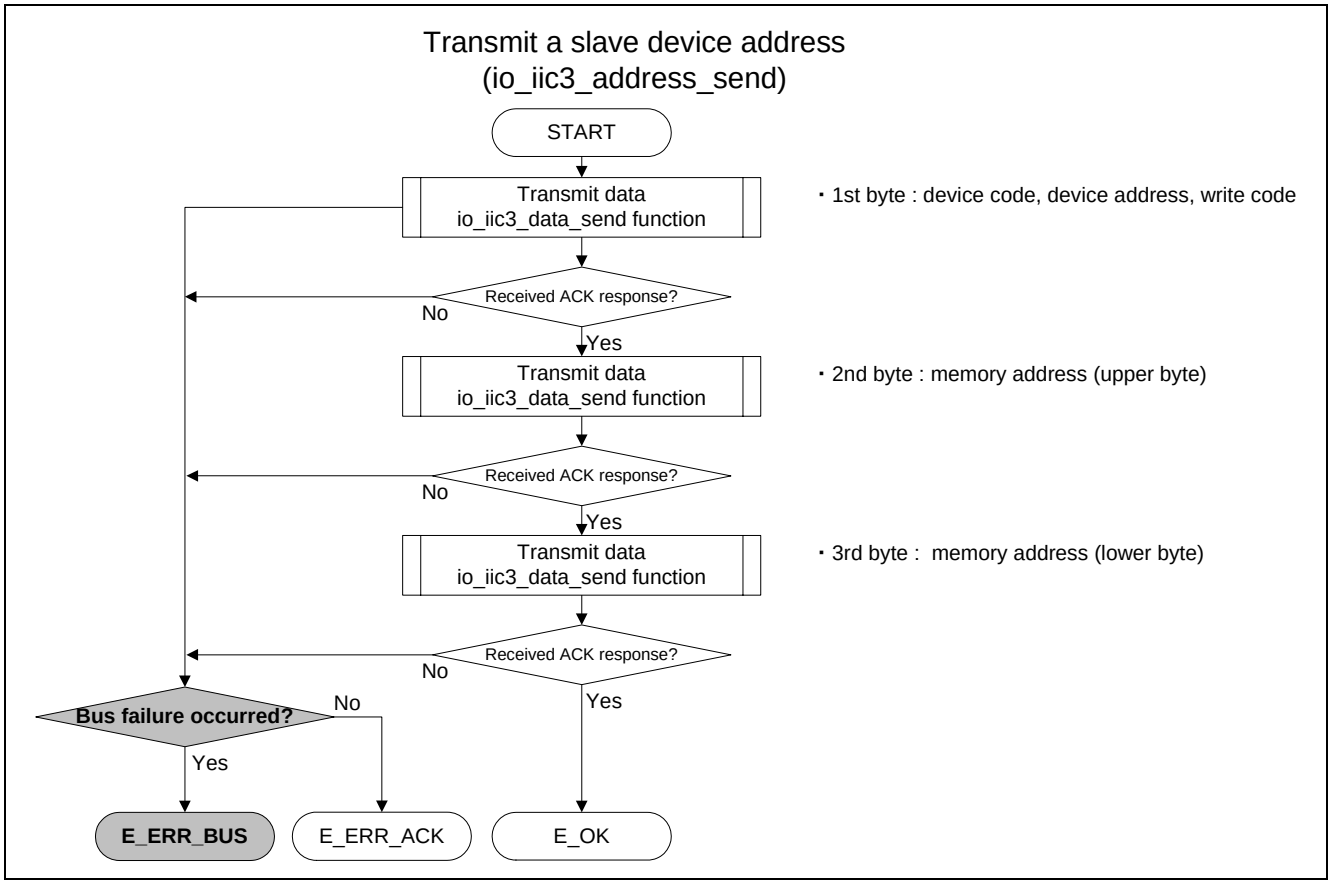

Figure 6.7 Function for Slave Device Address Transmission

6.7.6 Function for Data Transmission

Figure 6.8 shows the procedure of the functions for data transmission.

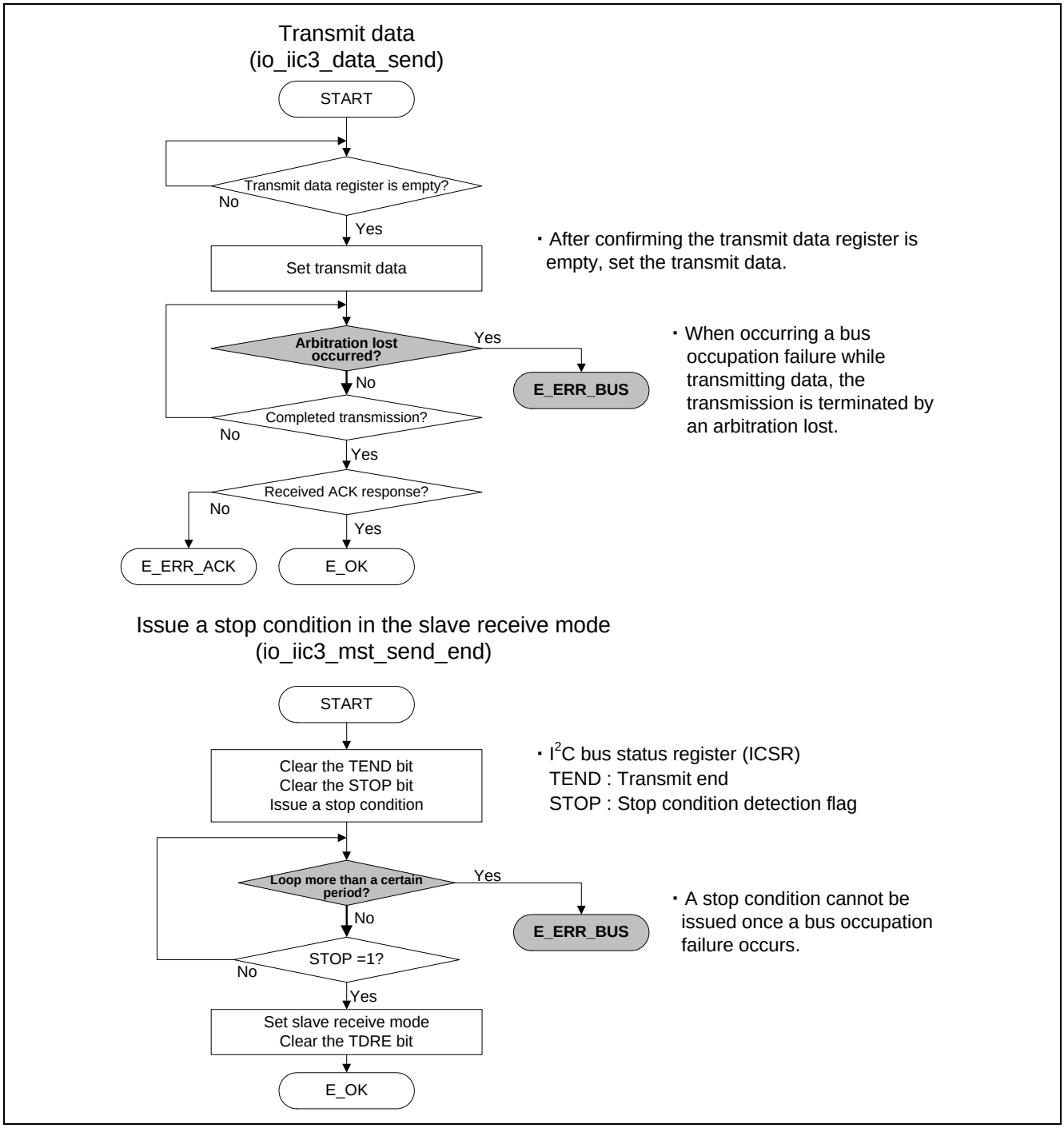

Figure 6.8 Functions for Data Transmission

6.7.7 Function for Recovery from Bus Occupation State

Figure 6.9 shows the procedure of the function for recovering from the bus occupation state.

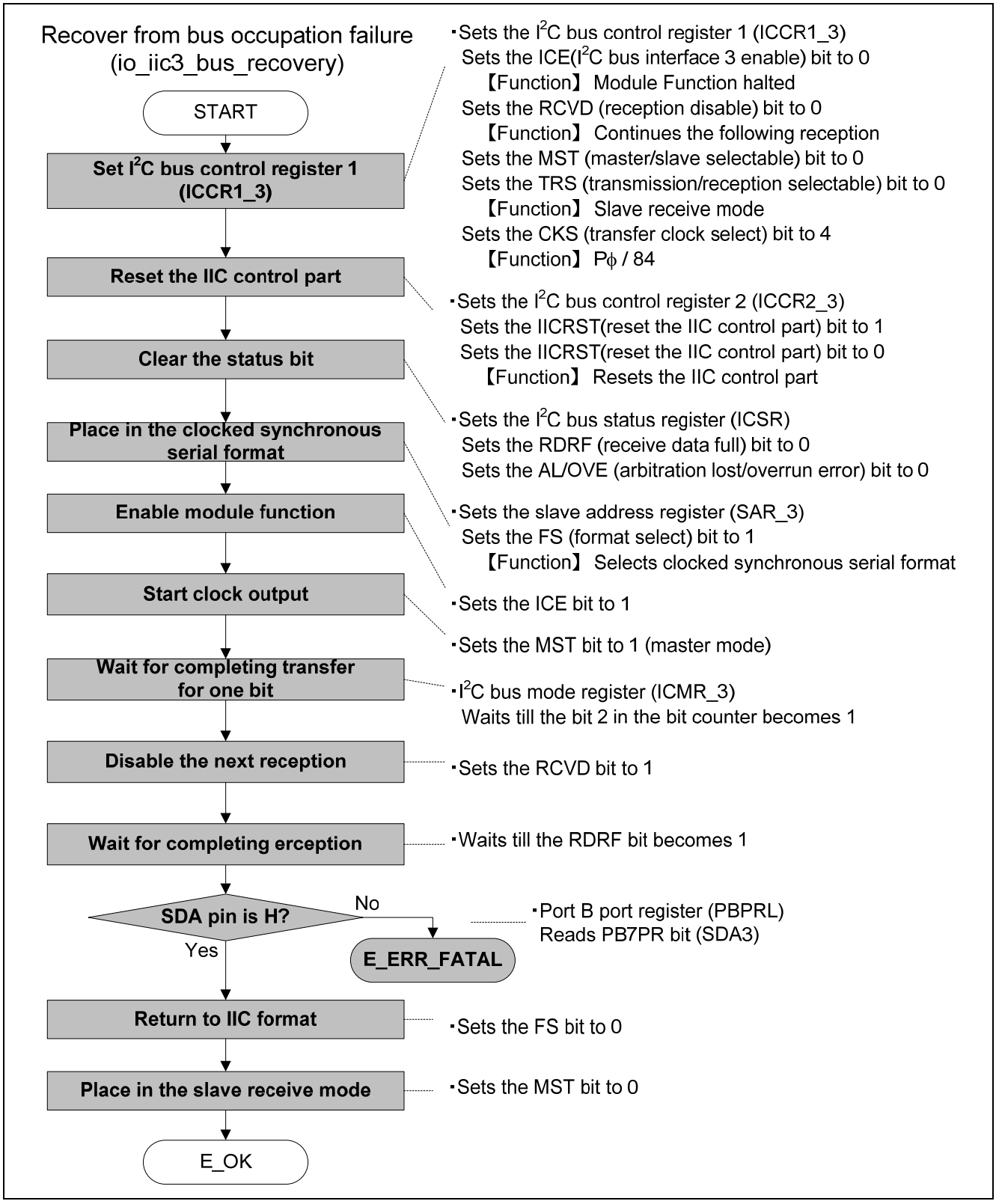

Figure 6.9 Function for Recovery from Bus Occupation State

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

Hardware Manual
SH7263 Group Hardware Manual Rev.3.00
SH7203 Group Hardware Manual Rev.3.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Development Tool Manual
SuperH C/C++ Compiler Package V.9.04 User's Manual Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

SuperH Family E10A-USB Emulator User's Manual Rev. 9.00
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Revision History	SH7263/SH7203 Group Application Note for IIC Bus Interface3 Dummy Clock Transmission in Communication Failure

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 23, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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