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H8/300L Super Low Power (SLP) 系列

外围功能的说明

内容

说明 H8/38024F 单片机的外围功能。

要点

本应用说明叙述在使用 H8/38024F 单片机的外围功能时应该注意的重要事项。
在本应用说明中叙述的外围功能，主要面向单片机的 SCI 和 LCD。

动作确认器件

H8/38024F

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1. SCI 接口

H8/38024F 单片机的串行通信接口只有一个 SCI3，运行在异步或者同步模式。支持全双工通信，内置能选择所需的位速率的波特率发生器，能选择内部或者外部时钟作为接收/发送时钟源，能使用 6 种中断。

另外，支持多处理器通信功能，能在多个处理器间传送串行数据。

本应用说明不叙述各种 SCI 寄存器的概要、设定和存取方法，而集中叙述在使用 SCI3 时需要注意和探讨的事项（时序问题等）。

1.1 异步模式

在异步模式下，与每个字符同步传送串行数据。通过 UART 或 ACIA 等标准异步通信 LSI 的接收器 / 发送器进行串行数据的传送。能选择 16 种传送格式。

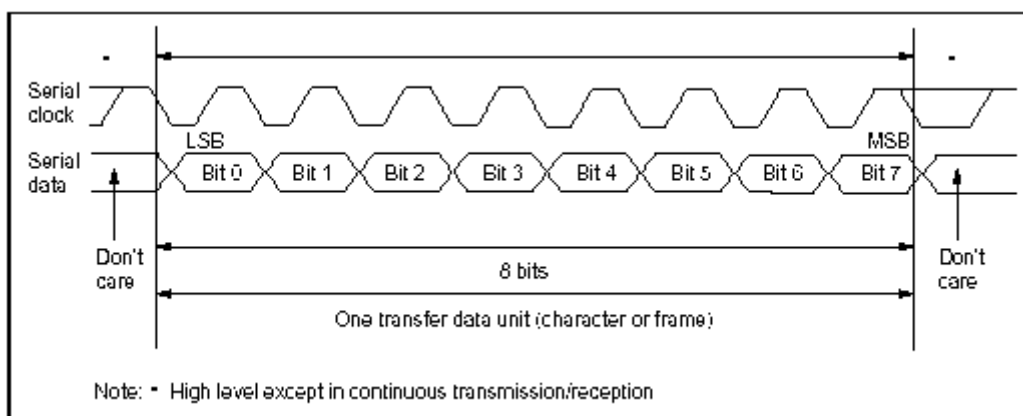
数据长	7、8、5 位
停止位长	1 位或者 2 位
奇偶校验	偶数校验、奇数校验、或者无奇偶校验
多处理器位	1 或者 0
接收错误的检测	奇偶校验、溢出、帧错误
中止的检测	在帧错误时，直接读 RXD ₃₂ 管脚的电平，检测中止

1.2 同步模式

在同步模式下，与时钟同步传送串行数据，能和具有同步通信功能的其他 LSI 进行串行数据的传送。此模式适用于高速串行通信。

数据长	8 位
接收错误的检测	溢出错误

同步通信在串行时钟的下降沿和下一个下降沿之间输出通信线上的数据，并在串行时钟的上升沿确定数据。请参照下图：



1 个传送数据从 LSB 开始，以 MSB 结束。在输出 MSB 后，通信线保持 MSB 的值。在同步模式的数据接收中，SCI3 在串行时钟的上升沿锁存接收数据。数据传送格式为 8 位固定的数据长，不能附加奇偶校验位和多处理器位。

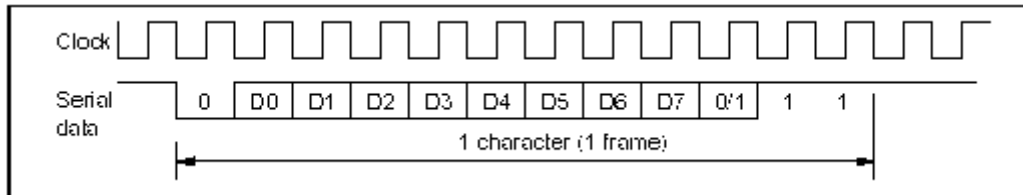
1.3 时钟

1.3.1 异步模式

能选择波特率发生器生成的内部时钟或者输入到 SCK32 管脚的外部时钟作为 SCI3 发送 / 接收时钟。在选择时钟源时，设定硬件手册中记载的寄存器。

将外部时钟输入到 SCK32 管脚时，时钟频率必须设定为位速率的 16 倍。

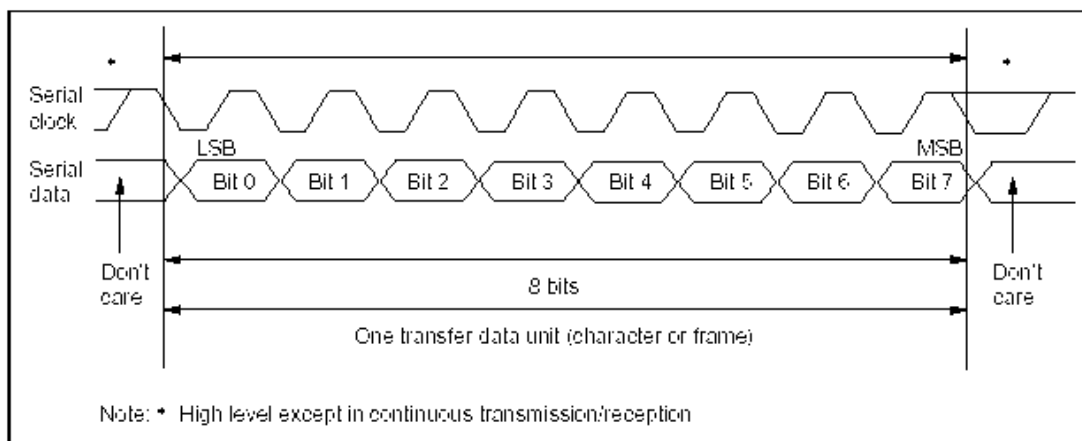
通过内部时钟进行 SCI3 运行时，能从 SCK32 管脚输出时钟。此时，输出时钟频率等于位速率，该相位在发送/接收数据的各位中央时钟上升。请参照以下的异步模式图：



1.3.2 同步模式

能选择波特率发生器生成的内部时钟或者输入到 SCK32 管脚的外部时钟中作为 SCI3 发送/接收时钟。

通过内部时钟进行 SCI3 运行时，能从 SCK32 管脚输出时钟。在发送或者接收 1 个字符中输出 8 个脉冲的串行时钟。当 SCI3 既不发送也不接收时，时钟固定为高电平。请参照下图：

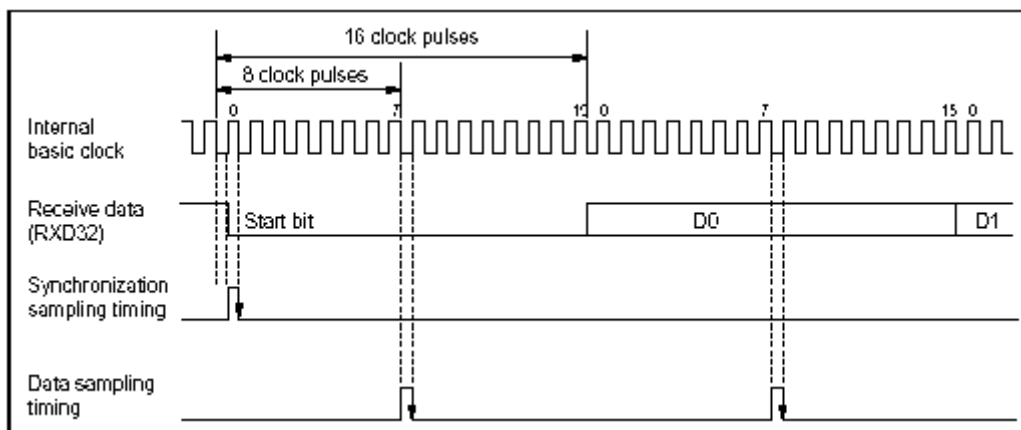


在异步模式使用外部时钟的情况下，必须注意不要在运行中（包含初始化）停止时钟。在同步模式使用外部时钟的情况下，不要在包含初始化的运行中供给时钟。

1.4 中断

SCI3 有发送结束、发送数据空、接收数据满和 3 种接收错误中断（溢出错误、帧错误、奇偶校验错误）共 6 种中断，这些中断被分配了相同的向量地址。关于中断的允许/禁止，请参照单片机的硬件手册。

最后，在此应该说明的要点是异步模式的接收数据的采样时序和接收数据的容限。在异步模式下，SCI3 通过频率为 16 倍传送率的基本时钟运行。在接收数据时，SCI3 以基本时钟为准，采样起始位的下降沿，取得内部同步。在基本时钟的第 8 个上升沿将接收数据取到内部。如下图所示：



2. LCD 接口

在此说明使用 H8/38024F 单片机的 LCD 功能连接 LCD 显示屏时的注意事项，不说明各种寄存器的设定方法。

H8/38024F 单片机内置段型 LCD 控制电路、LCD 驱动器和电源供给电路，能直接驱动 LCD 显示屏。LCD 驱动器/控制器的特点如下所示：

- 显示能力

Duty Cycle	Internal Driver
Static	32 seg
1/2	32 seg
1/3	32 seg
1/4	32 seg

- LCD RAM 容量 [128 位 = 8 位 x 16 字节]
- LCD RAM 的字存取
- 能并联
- 能在待机以外的全部运行模式进行显示
- 能选择 11 种帧频
- 通过内部电源分压电阻供给 LCD 驱动功率
- 能选择 A 或者 B 波形

2.1 帧频

LCD 帧频是底板和段输出变化的速度，能由 LCD 周期/2 * 底板数求出。帧频的范围是 25 到 250Hz，但是最一般的是 50 到 150Hz。如果频率高，消耗功率就增加；如果频率低，LCD 显示屏的图像就不清晰。下表总结了帧频的几种选择方法：

Bit 3	Bit 2	Bit 1	Bit 0	Operating Clock	Frame Frequency ^{*2}	
					$\phi = 2 \text{ MHz}$	$\phi = 250 \text{ kHz}^{*1}$
0	*	0	0	ϕw	128 Hz ^{*3} (initial value)	
0	*	0	1	$\phi w/2$	64 Hz ^{*3}	
0	*	1	*	$\phi w/4$	32 Hz ^{*3}	
1	0	0	0	$\phi/2$	—	244 Hz
1	0	0	1	$\phi/4$	977 Hz	122 Hz
1	0	1	0	$\phi/8$	488 Hz	61 Hz
1	0	1	1	$\phi/16$	244 Hz	30.5 Hz
1	1	0	0	$\phi/32$	122 Hz	—
1	1	0	1	$\phi/64$	61 Hz	—
1	1	1	0	$\phi/128$	30.5 Hz	—
1	1	1	1	$\phi/256$	—	—

*: Don't care

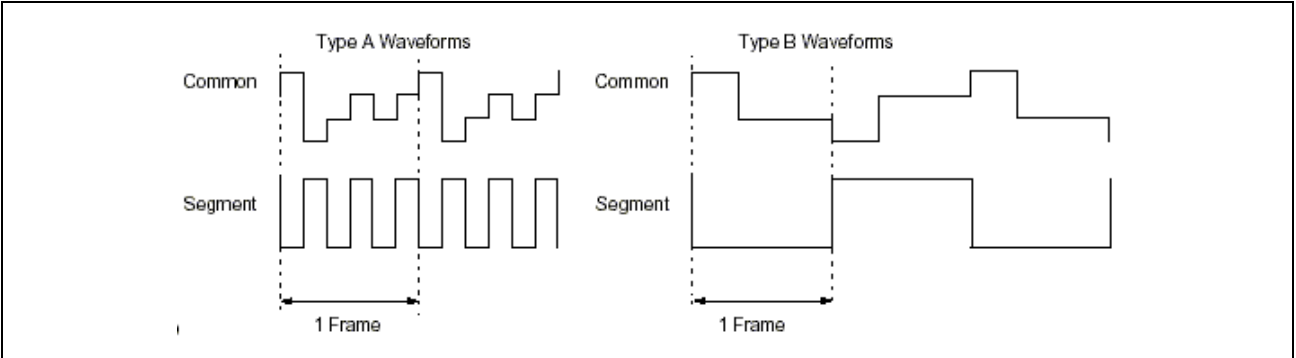
Notes: *1 This is the frame frequency in active (medium-speed, $\phi csc/16$) mode when $\phi = 2 \text{ MHz}$.

*2 When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.

*3 This is the frame frequency when $\phi w = 32.768 \text{ kHz}$.

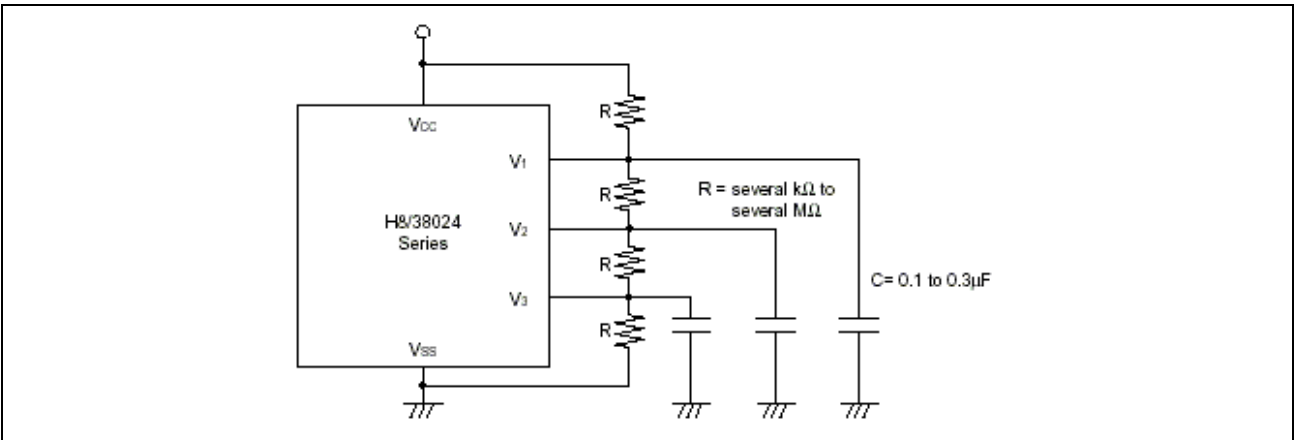
2.2 驱动波形

驱动 LCD 显示屏的波形有 A 型和 B 型 2 种。在给像素加载电压时，LCD 驱动器必须保持各像素的端到端的电压为 $0V_{DC}$ 。A 型的波形为：在 1 帧内保持 $0V_{DC}$ ，B 型的波形为：在 2 帧内保持 $0V_{DC}$ 。各类型的波形如下图所示：



2.3 LCD 驱动电源的升压

在使用大型 LCD 显示屏时，有时内部的电源供给能力不足。如果在使用 V_{CC} 作为电源时电源不足，就必须降低电源阻抗。为了实现这一功能，将 $0.1\mu F \sim 0.3\mu F$ 的旁路电容连接到 $V_1 \sim V_3$ 的引脚，或者在外部附加分压电阻。外部分压电阻的连接如下图所示：



2.4 低功耗模式的 LCD 控制器/驱动器的运行

H8/38024 系列的 LCD 控制器/驱动器也能在低功耗模式下运行。

必须注意：由于在子激活模式、时钟模式和子睡眠模式下系统时钟振荡器停止，所以当还没有选择内部子时钟时，不供给时钟且停止显示。此时，由于电流可能直接供给 LCD 显示屏，所以必须选择子时钟。由于在激活（中速）模式下提供系统时钟，为了使帧频不变，需要更改帧频的设置。关于帧频的选择，请参照本应用说明的 2.1 章。

Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
Clock	ϕ	Runs	Runs	Runs	Stops	Stops	Stops	Stops	Stops ^{*4}
	ϕw	Runs	Runs	Runs	Runs	Runs	Runs	Stops ^{*1}	Stops ^{*4}
Display operation	ACT = 0	Stops	Stops	Stops	Stops	Stops	Stops	Stops ^{*2}	Stops
	ACT = 1	Stops	Functions	Functions	Functions ^{*3}	Functions ^{*3}	Functions ^{*3}	Stops ^{*2}	Stops

Notes: *1 The subclock oscillator does not stop, but clock supply is halted.

*2 The LCD drive power supply is turned off regardless of the setting of the PSW bit.

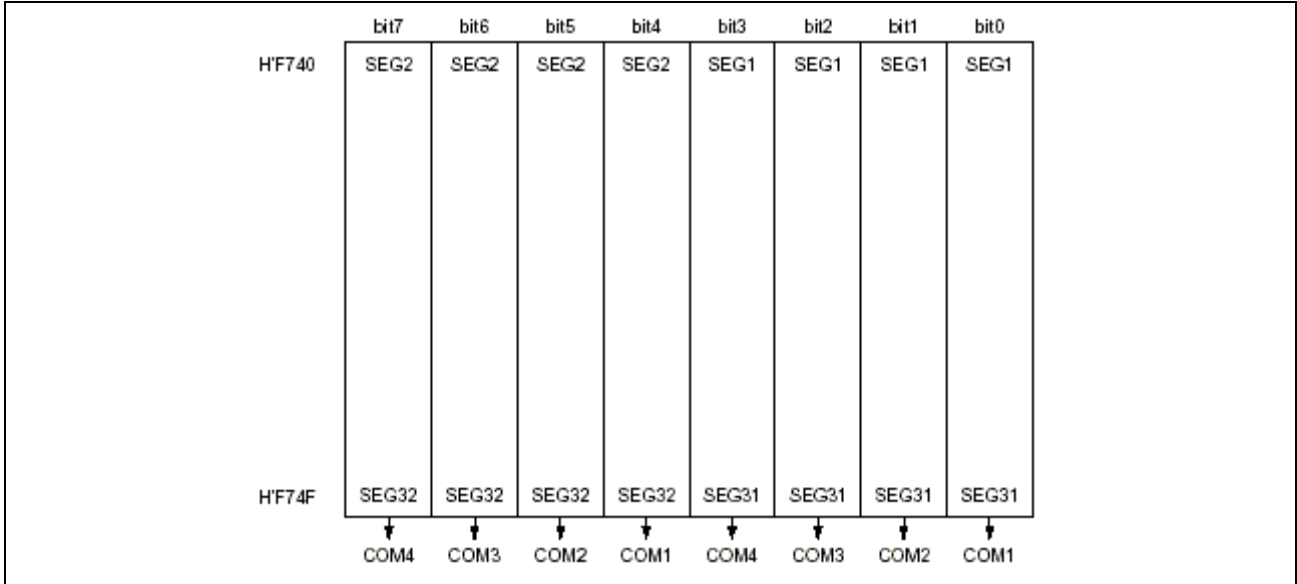
*3 Display operation is performed only if ϕw , $\phi w/2$, or $\phi w/4$ is selected as the operating clock.

*4 The clock supplied to the LCD stops.

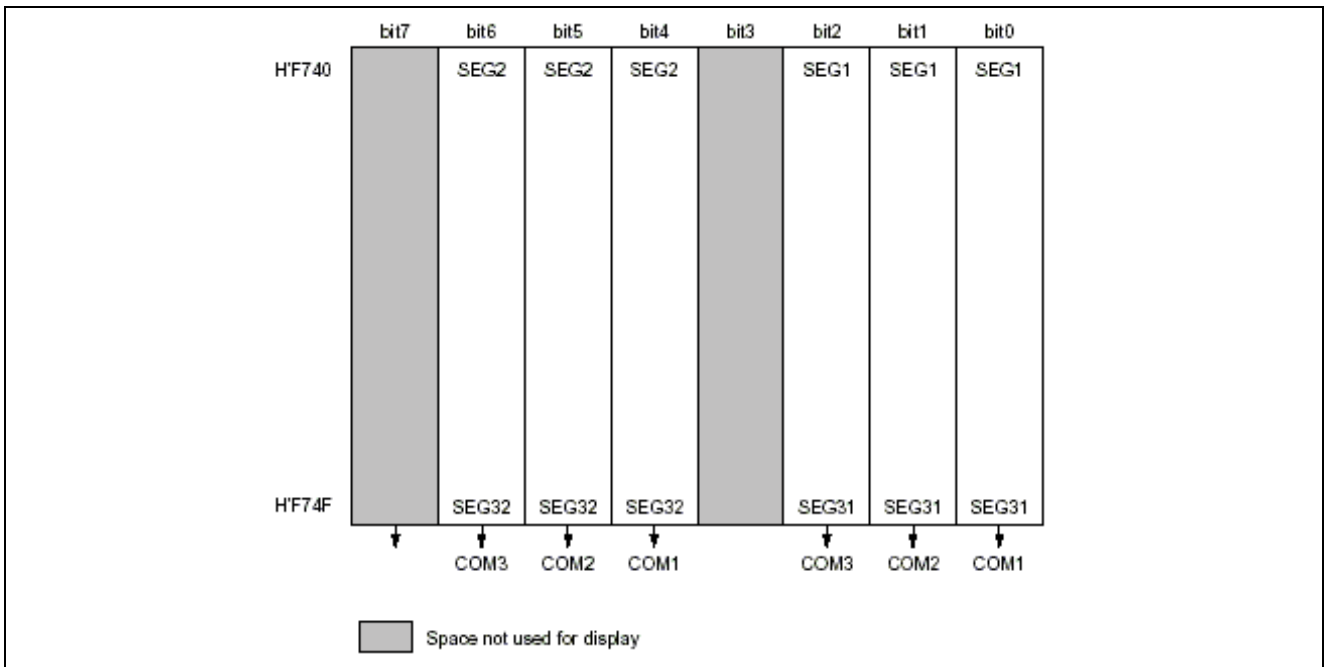
2.5 LCD RAM 和占空比的关系

LCD RAM 和显示段的关系因占空比而不同。在设定了显示所需的寄存器后，使用和通常 RAM 存取的相同指令将数据写到对应占空比的部分。其次，如果将显示为 ON，就自动开始显示。设定 RAM 时，能使用字或者字节存取指令。

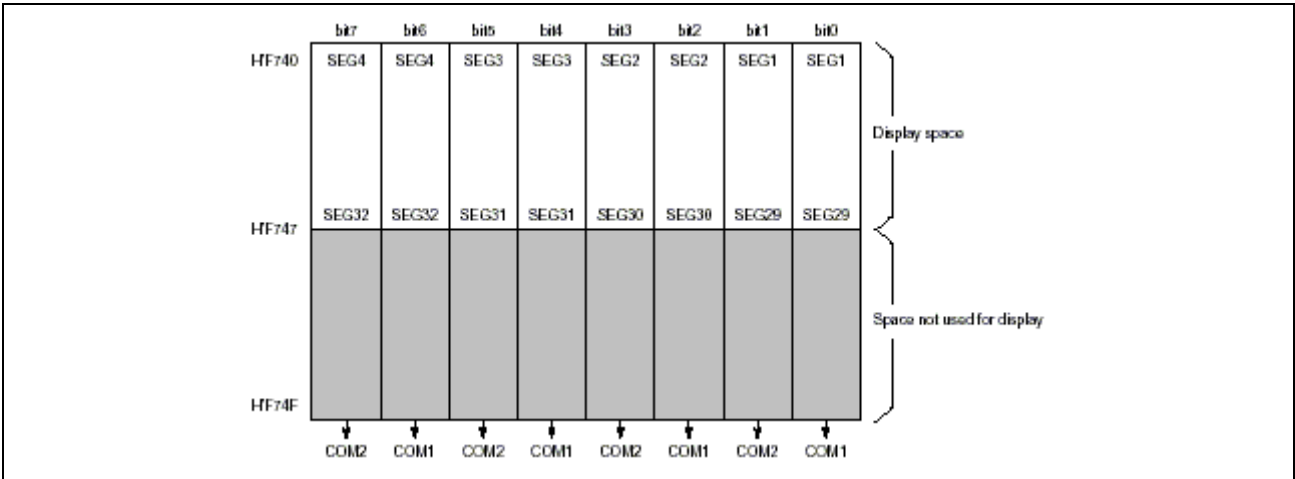
LCD RAM 和支持的各种占空比的关系如下图所示：



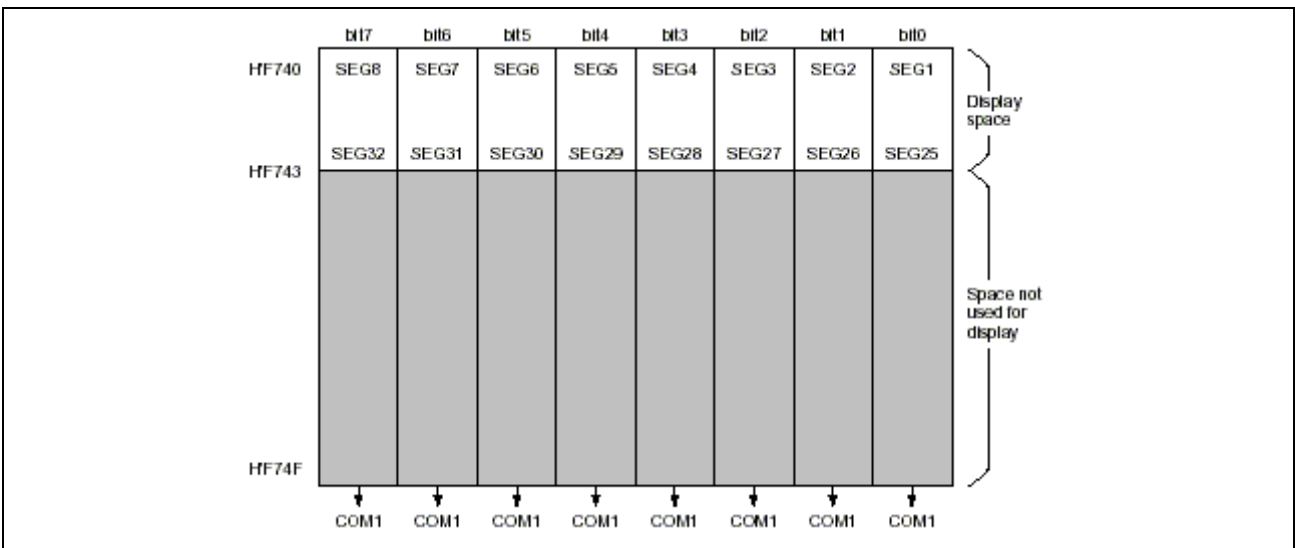
1/4 占空比周期的 LCD RAM 映像



1/3 占空比周期的 LCD RAM 映像



1/2 占空比周期的 LCD RAM 映像



静态模式的 LCD RAM 映像

2.6 电特性

LCD 控制器/驱动器的电特性因掩模版和 F-ZTAT 版而不同。为了正确地运行，系统设计员必须注意此不同点。另外，必须调查 LCD 厂家提供的 LCD 显示屏的电气规格，确认 LCD 控制器/驱动器是否适合 LCD 显示屏。

掩模版和 F-ZTAT 版的值如下所示：

2.6.1 掩模版和 Z-TAT 版

$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}^{*3}$
 (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values			Reference Figure
				Min	Typ	Max	
Segment driver drop voltage	V_{DS}	SEG ₁ to SEG ₃₂	$I_D = 2 \mu\text{A}$ $V_1 = 2.7 \text{ V to } 5.5 \text{ V}$	—	—	0.6	V *1
Common driver drop voltage	V_{DC}	COM ₁ to COM ₄	$I_D = 2 \mu\text{A}$ $V_1 = 2.7 \text{ V to } 5.5 \text{ V}$	—	—	0.3	V *1
LCD power supply split-resistance	R_{LCD}		Between V_1 and V_{SS}	0.5	3.0	9.0	MΩ
Liquid crystal display voltage	V_{LCD}	V_1		2.2	—	5.5	V *2

Notes: *1 The voltage drop from power supply pins V_1 , V_2 , V_3 , and V_{SS} to each segment pin or common pin.

*2 When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$.

*3 The guaranteed temperature as an electrical characteristic for Die products is 75°C.

2.6.2 F-ZTAT 版

$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}^{*3}$
 (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values			Reference Figure
				Min	Typ	Max	
Segment driver drop voltage	V_{DS}	SEG ₁ to SEG ₃₂	$I_D = 2 \mu\text{A}$ $V_1 = 2.7 \text{ V to } 3.6 \text{ V}$	—	—	0.6	V *1
Common driver drop voltage	V_{DC}	COM ₁ to COM ₄	$I_D = 2 \mu\text{A}$ $V_1 = 2.7 \text{ V to } 3.6 \text{ V}$	—	—	0.3	V *1
LCD power supply split-resistance	R_{LCD}		Between V_1 and V_{SS}	0.5	3.0	9.0	MΩ
Liquid crystal display voltage	V_{LCD}	V_1		2.2	—	3.6	V *2

Notes: *1 The voltage drop from power supply pins V_1 , V_2 , V_3 , and V_{SS} to each segment pin or common pin.

*2 When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$.

*3 The guaranteed temperature as an electrical characteristic for Die products is 75°C.

3. 参考文献

1. H8/38024 Series, H8/38024F-ZTAT™ Hardware Manual
2. www.embedded.com
3. www.ednmag.com

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