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Renesas Electronics Corporation

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SH7144/45 Group

RAM Monitoring Using DMAC

1. Specifications

Using the SH7145's SCI in asynchronous mode, a RAM reference address (4-byte data) transmitted from the console is received, and the contents of that address are fetched from RAM and transmitted to the console via the SCI, as shown in figure 1.

The transfer protocol settings used are 19200 bps, 8-bit data, one stop bit, and no parity.

For data transfer from RDR to RAM, DMAC direct addressing mode is used, and RDR receive data is stored in RAM, as shown in figure 2.

For data transfer from RAM to TDR, DMAC indirect addressing mode is used and the following operations are executed, as shown in figure 3.

1. Data stored in RAM is stored in a temporary buffer in the DMAC, and data is fetched from RAM using this as the address.
2. Fetched data is transferred sequentially to TDR one byte at a time.

The DMAC transfer conditions are as shown in tables 2.11 and 2.12.

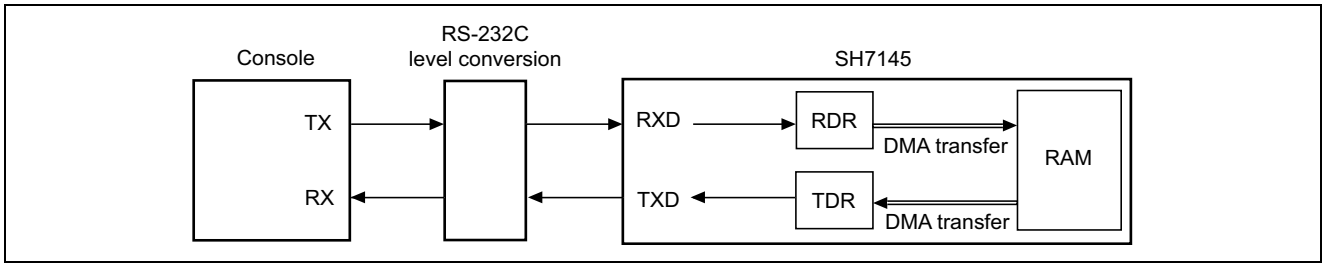


Figure 1 Block Diagram of SCI Transfer of Data in RAM by SH7145

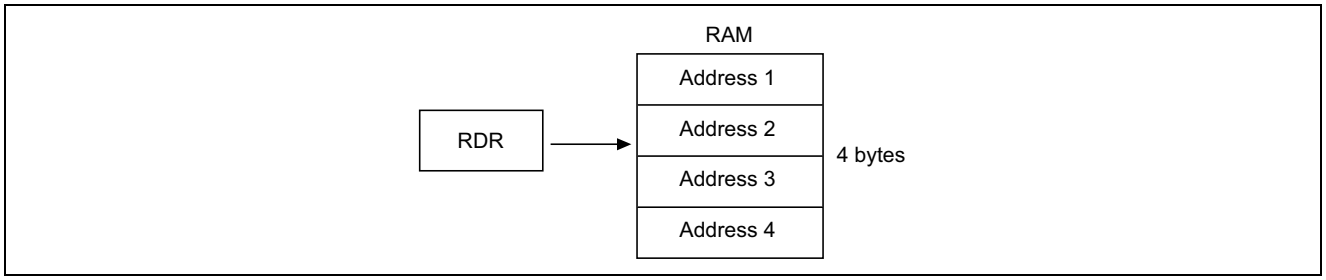


Figure 2 Data Transfer Using DMAC (Transfer Source Direct Addressing)

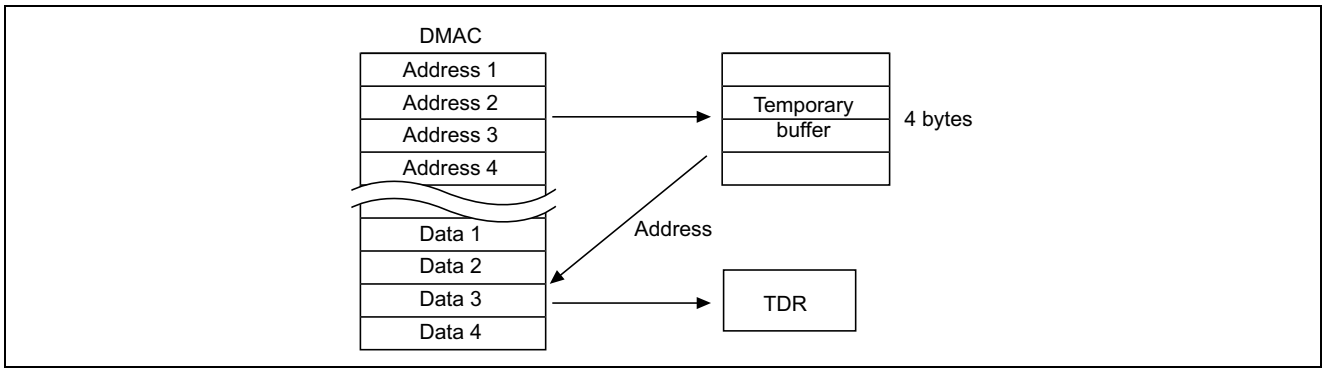


Figure 3 Data Transfer Using DMAC (Transfer Source Indirect Addressing)

Table 1 DMAC Transfer Conditions for SCI Reception (RDR → RAM)

Condition	Description
DMAC channel	Channel 0
Transfer source	On-chip SCI channel 0
Transfer destination	On-chip RAM
Number of transfers	4
Transfer source address	Fixed
Transfer destination address	Incremented
Transfer request source	SCI channel 0
Bus mode	Cycle-steal
Transfer unit	Byte

Table 2 DMAC Transfer Conditions for SCI Reception (RAM → TDR)

Condition	Description
DMAC channel	Channel 3
Transfer source	On-chip RAM
Transfer destination	On-chip SCI channel 0
Number of transfers	1
Transfer source address	Incremented
Transfer destination address	Fixed
Transfer request source	SCI channel 0
Bus mode	Cycle-steal
Transfer unit	Byte

2. Functions Used

In this sample task, RAM monitoring is performed using the SCI and DMAC.

Figure 4 shows a block diagram of SCI transmission circuits. In this task, console data transmission is performed using the following SCI functions.

- A function that performs data communication asynchronously, with synchronization performed character by character (asynchronous mode)
- A function that generates an interrupt on completion of transmission (TEI interrupt)

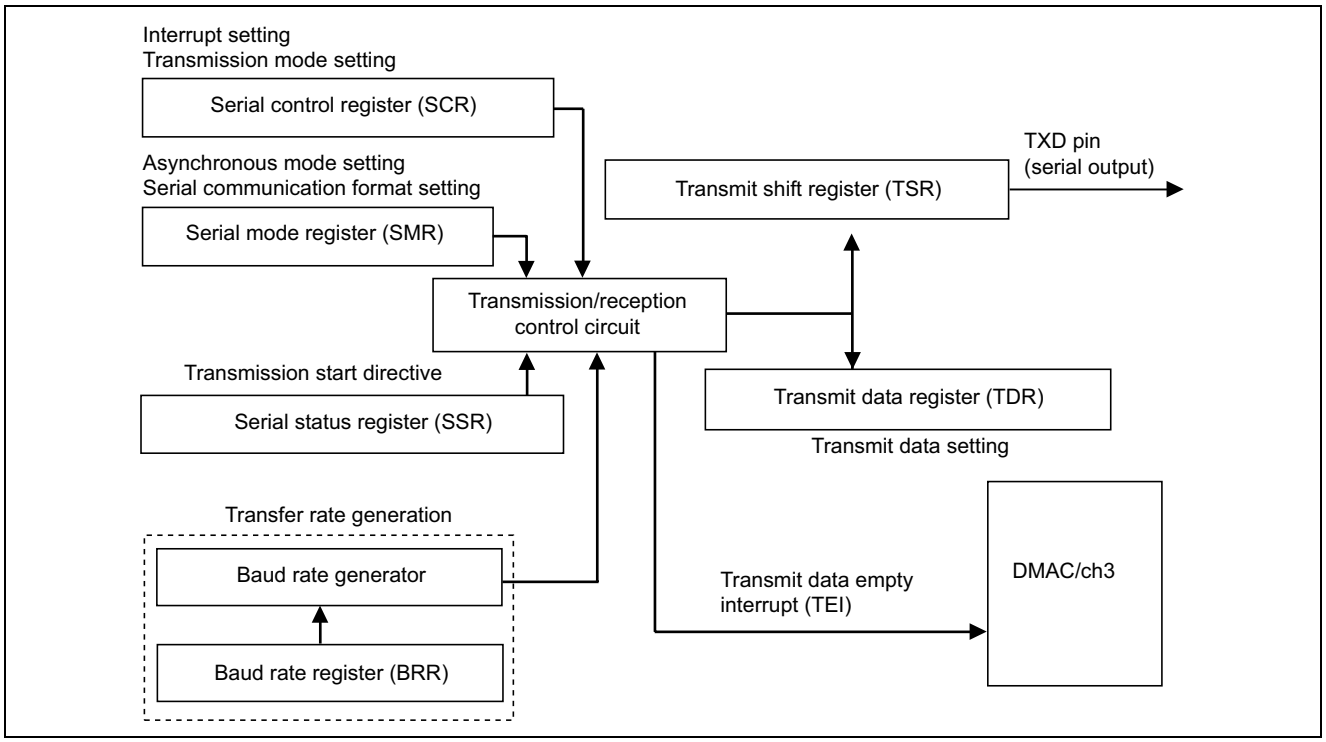


Figure 4 SCI Transmission Block Diagram

Figure 5 shows a block diagram of SCI reception circuits. In this sample task, data is received from the console using the following SCI functions.

- A function that performs data communication asynchronously, with synchronization performed character by character (asynchronous mode)
- A function that generates an interrupt on completion of reception (RXI interrupt)

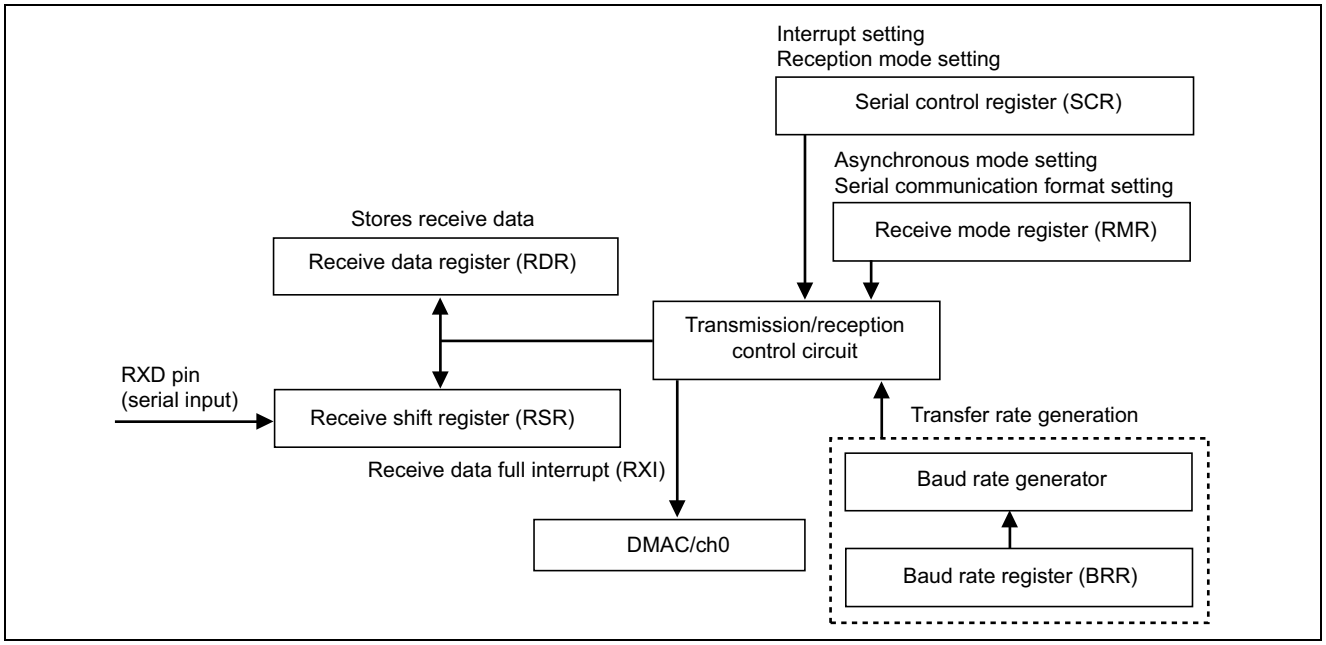


Figure 5 SCI Reception Block Diagram

Figure 6 shows a block diagram of DMAC/ch0 used in this sample task. In this sample task, block transfer is performed using the following DMAC/ch0 functions.

- A function that performs direct transfer of address data for both the transfer source and transfer destination when the DMAC is activated (direct address transfer mode)
- A function that activates the DMAC by means of the SCI

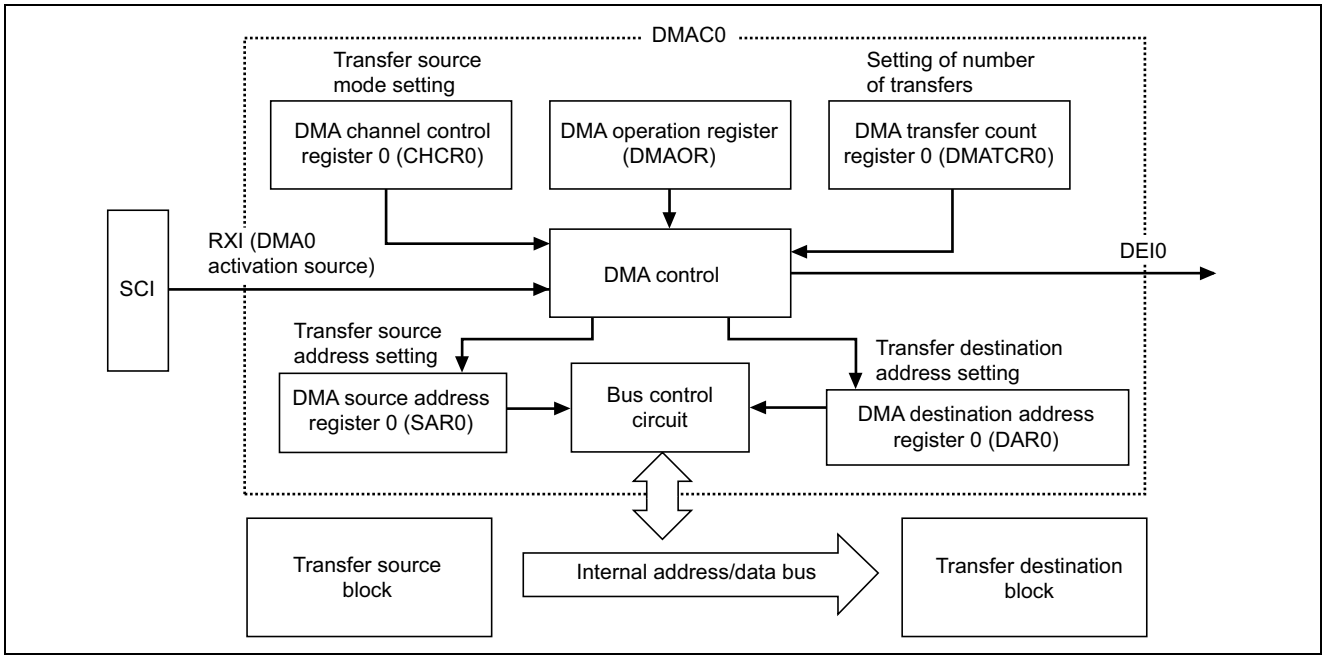


Figure 6 Block Diagram of DMAC/ch0

Figure 7 shows a block diagram of DMAC/ch3 used in this sample task. In this sample task, block transfer is performed using the following DMAC/ch3 functions.

- A function that transfers data stored in a transfer source register when the DMAC is activated (indirect address transfer mode)
- A function that activates the DMAC by means of the SCI

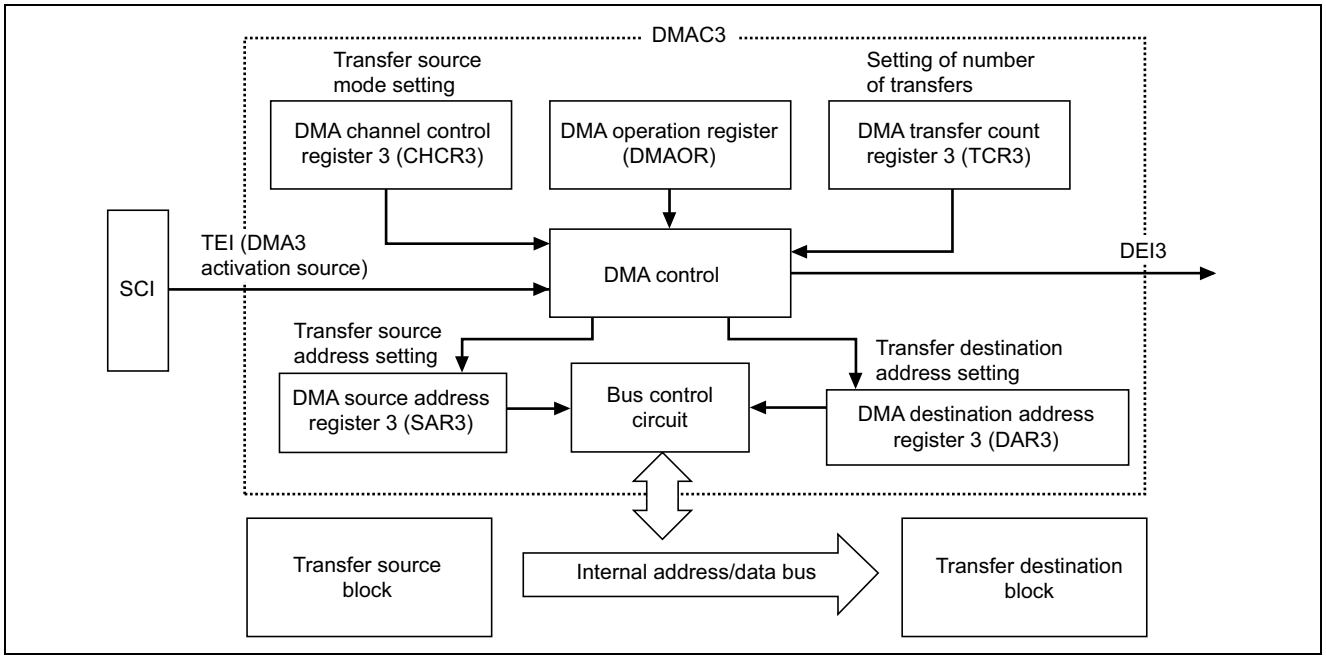


Figure 7 Block Diagram of DMAC/ch3

Table 3 shows the function assignments used in this sample task. Data transmission/reception is performed via the SCI by assigning DMAC and SCI functions as shown in the table.

Table 3 Function Assignments

Pin or Register Name	Function Assignment
SAR0	Transfer source address setting
SAR3	
DAR0	Transfer destination address setting
DAR3	
TCR0	Setting of number of transfers
TCR3	
CHCR0	Setting of DMAC operating mode, transfer method, etc.
CHCR3	
DMAOR	DMAC executing channel priority level setting
RXD	Data reception pin
TXD	Data transmission pin
SMR	SCI transmission format setting
SCR	SCI interrupt enabling/disabling setting
SSR	Interrupt status setting
RDR	Stores receive data from console
TDR	Used to transfer transmit data to console
BRR	Transfer rate setting

3. Principles of Operation

Figure 8 illustrates the principles of operation of this sample task. Data transmission/reception is performed via the SCI by SH7145 hardware and software processing as shown in the figure.

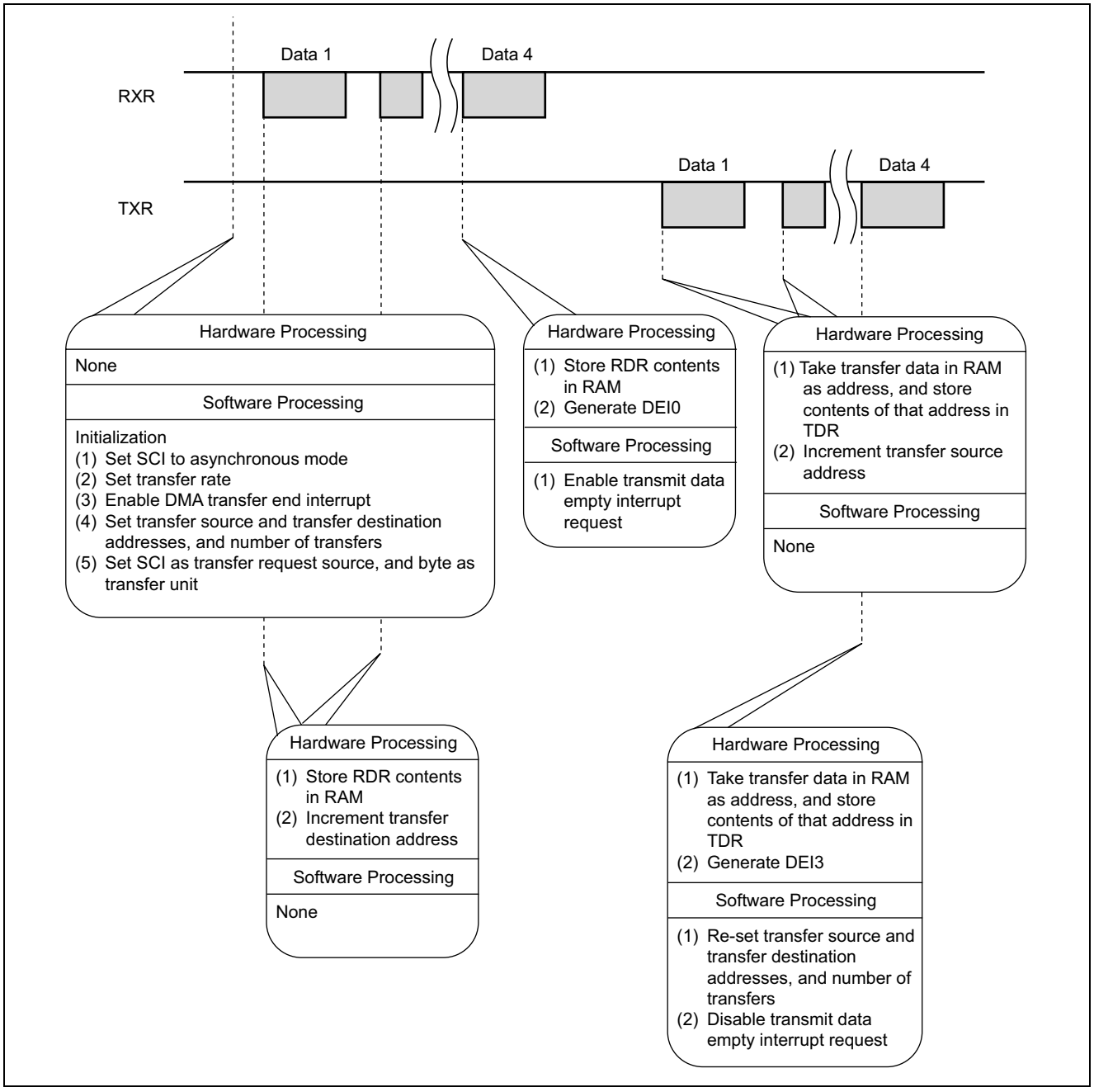


Figure 8 Principles of Operation of Data Transfer by SCI

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	rammon	Performs SCI and DMAC initialization
Receive data transfer	dma_rdr	Initiated by DEI0. Enables transmit data empty interrupt request
Transmit data transfer	dma_tdr	Initiated by DEI3. Re-sets transfer source and transfer destination addresses, and number of transfers. Disables transmit data empty interrupt request

(2) Arguments

Label or Register Name	Function	Data Length	Module	Input/Output
dat.addr0	Stores RAM reference address	Longword	Main routine	Input
data0	Stores reference data ("H")	Byte	Main routine	Output

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_STBY.MSTCR1	SCI and DMAC module standby mode clearing	H'FFFF861C	H'f03d
P_DMAC0.SAR0	Used to set RDR address	H'FFFF86C0	&P_SCI1.RDR_1
P_DMAC0.DAR0	Used to set transfer destination RAM start address	H'FFFF86C4	&dat.addr0
P_DMAC0.DMATCR0	Sets 4 as number of transfers	H'FFFF86C8	H'04
P_DMAC0.CHCR0	Setting of DMAC operating mode, transfer method, etc.	H'FFFF86CC	H'00004f05
P_DMAC3.SAR3	Used to set transfer source RAM start address	H'FFFF86F0	&dat.addr0
P_DMAC3.DAR3	Used to set TDR address	H'FFFF86F4	&P_SCI1.TDR_1
P_DMAC3.DMATCR3	Sets 1 as number of transfers	H'FFFF86F8	H'01
P_DMAC3.CHCR3	Setting of DMAC operating mode, transfer method, etc.	H'FFFF86FC	H'00101e04
P_DMAC.DMAOR	Setting of DMAC executing channel priority level	H'FFFF86B0	H'0001
P_PORTA.PAIORL	Sets SCI ch1 input/output pin	H'FFFF8386	H'0010
P_PORTA.PACRL2	Sets pin multiplexing to SCI0	H'FFFF838E	H'0140
P_INTC.IPRC	Sets 14/15 as DMAC ch0/3 interrupt priority levels	H'FFFF834C	H'e00f
P_INTC.IPRF	Sets 10 as SCI/ch1 interrupt priority level	H'FFFF8352	H'000a
P_SCI1.SMR_1	Sets SCI to asynchronous mode	H'FFFF81B0	H'00
P_SCI1.SCR_1	Enables transmission/reception interrupts, transmission/reception operation	H'FFFF81B2	H'50
P_SCI1.BRR_1	Sets transfer rate (19200 bits/s)	H'FFFF81B1	H'40

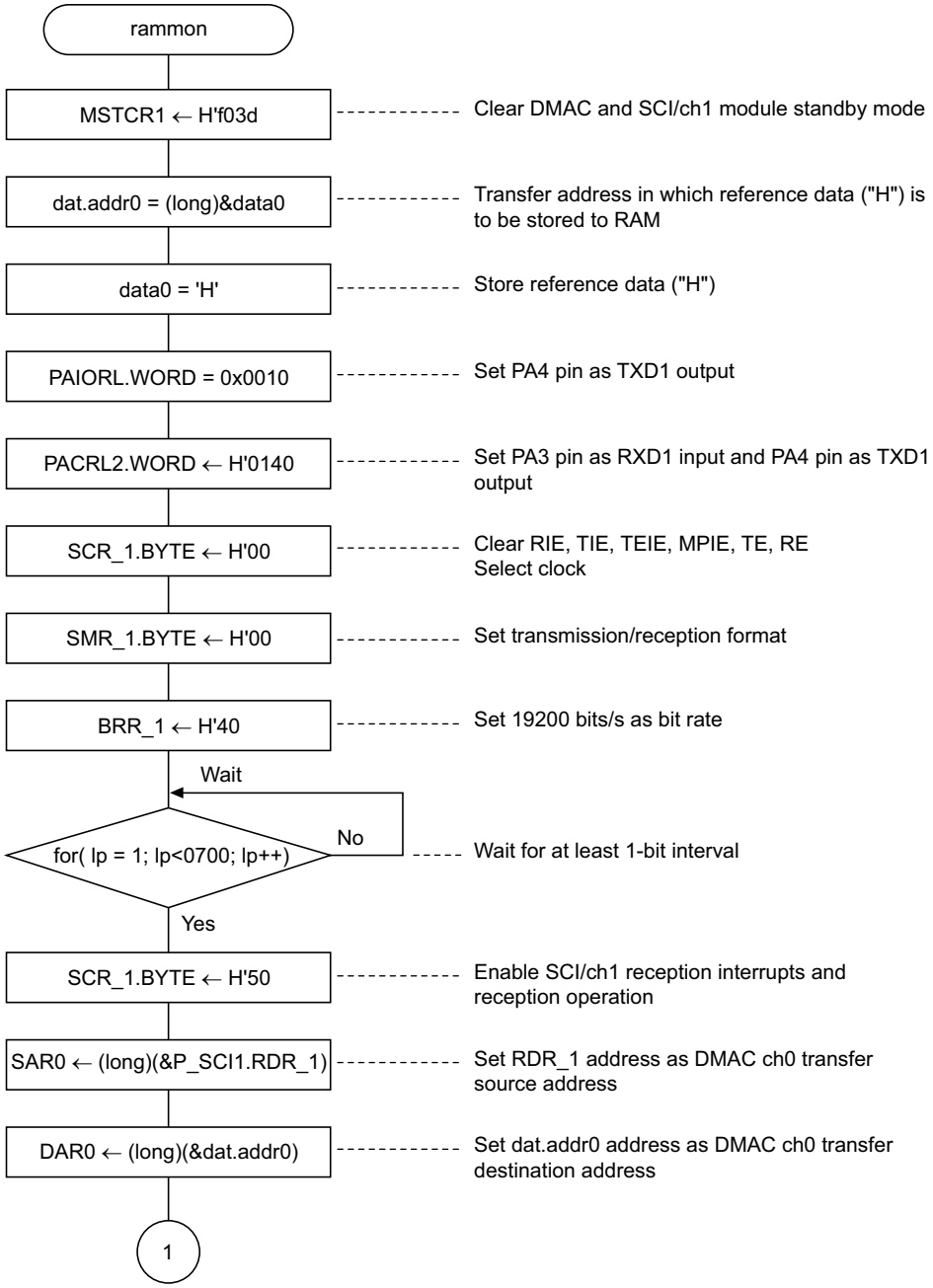
(4) RAM Used

This task does not use any RAM apart from the arguments.

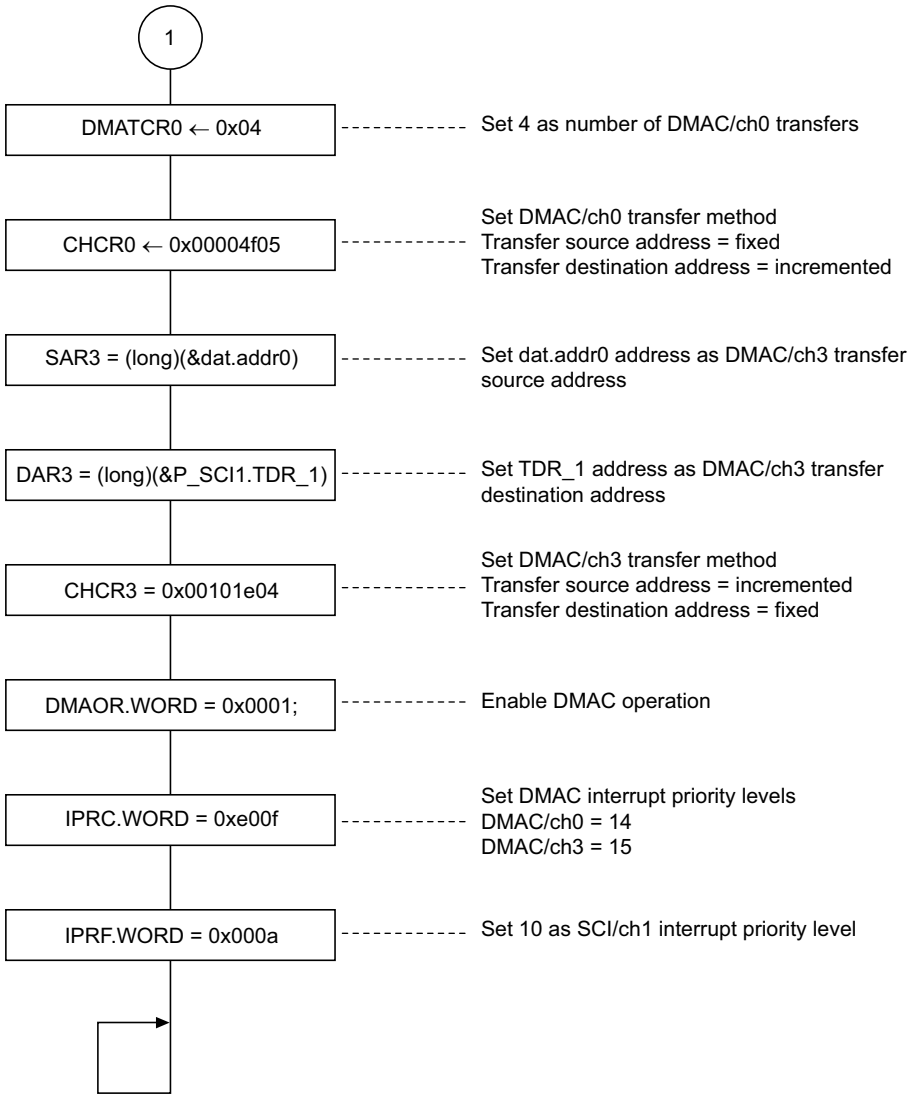
Note: SH7145 header file names are used for register label names.

5. Flowcharts

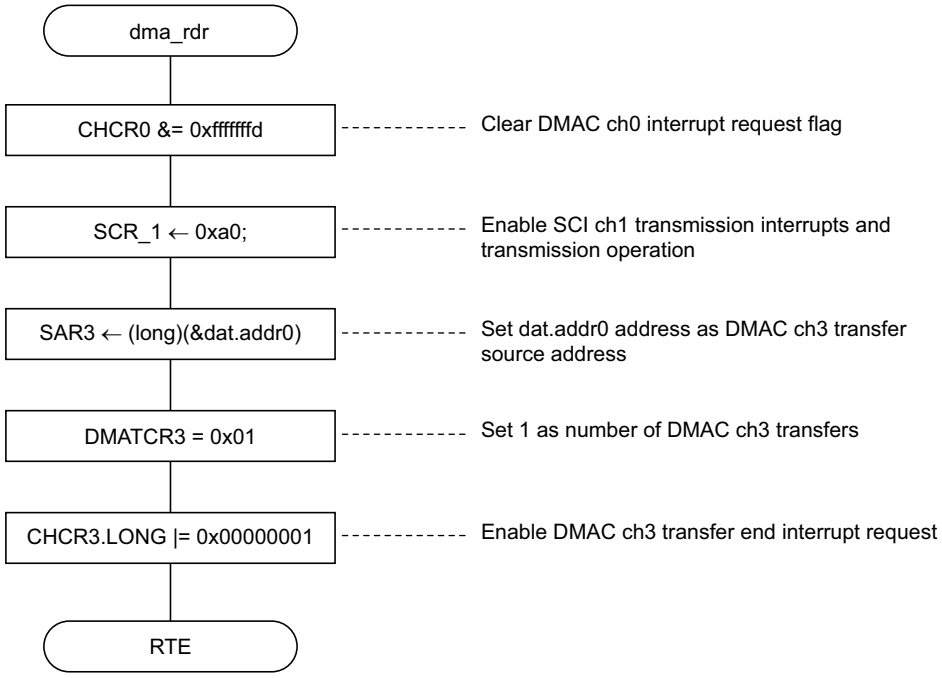
(1) Main routine



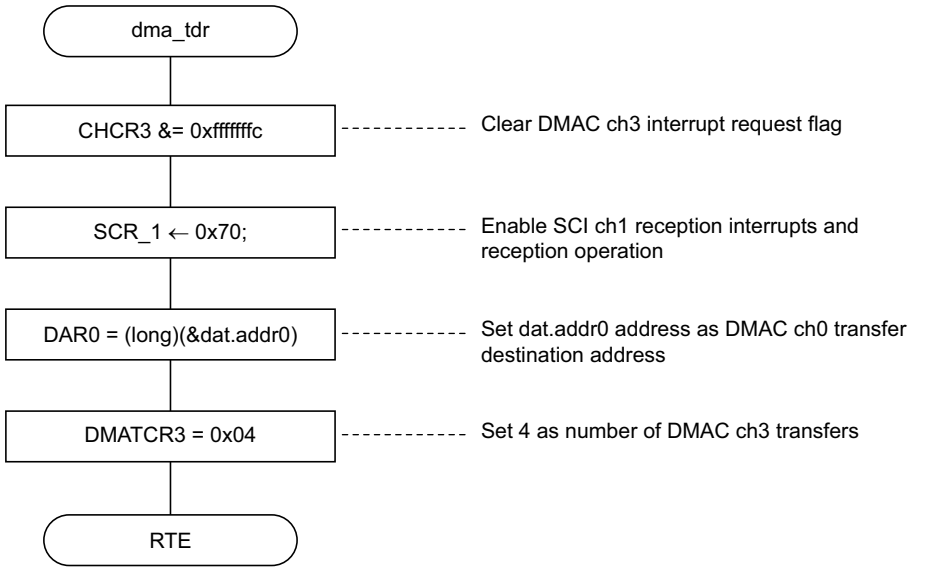
(2) Main routine (cont)



(3) Receive data transfer



(4) Transmit data transfer



6. Program Listing

```
/************************************************************************/
/*                                INCLUDE FILE                          */
/************************************************************************/
#include<machine.h>
#include "iodefine_7145F.h"
/************************************************************************/
/*                              PROTOTYPE                               */
/************************************************************************/
void rammon(void);
#pragma interrupt(dma_rdr,dma_tdr)
/************************************************************************/
/*                              RAM ALLOCATION                          */
/************************************************************************/
#define data0 (*(volatile unsigned char *)0xffffe000)
volatile struct addr
{
     long addr0;
};
#define dat (*(struct addr *)0xffffe010)
/************************************************************************/
/*                            MAIN PROGRAM                              */
/************************************************************************/
void rammon(void)
 {
  signed int lp;
  P_STBY.MSTCR1.WORD = 0xf03d;          /* DMAC, SCI ch1 module standby mode clear */

  dat.addr0 = (long)&data0;
  data0 = 'H';                          /* reference data = ”H” */
  P_PORTA.PAIORL.WORD = 0x0010;
  P_PORTA.PACRL2.WORD = 0X0140;

  P_SCI1.SCR_1.BYTE = 0x00;
  P_SCI1.SMR_1.BYTE = 0x00;             /* Pϕ/1 */
  P_SCI1.BRR_1 = 0x40;                  /* 19200bps */
  for( lp = 1; lp<0300; lp++);          /* for loop = 1bit */
  P_SCI1.SCR_1.BYTE = 0x50;
  P_DMAC0.SAR0 = (long)(&P_SCI1.RDR_1); /* DMAC ch0 source address */
  P_DMAC0.DAR0 = (long)(&dat.addr0);    /* DMAC ch0 destination address */
  P_DMAC0.DMATCR0 = 0x04;               /* DMAC ch0 transfer count =4 */
  P_DMAC0.CHCR0.LONG = 0x00004f05;
  P_DMAC3.SAR3 = (long)(&dat.addr0);    /* DMAC ch3 source address */
  P_DMAC3.DAR3 = (long)(&P_SCI1.TDR_1); /* DMAC ch0 destination address */
  P_DMAC3.CHCR3.LONG = 0x00101e04;
  P_DMAC.DMAOR.WORD = 0x0001;           /* Enable DMAC operation */
  P_INTC.IPRC.WORD = 0xe00f;            /* DMAC ch0 interrupt level =14 ch3
                                           interrupt level =15 */
  P_INTC.IPRF.WORD = 0x000a;            /* SCI ch1 interrupt level =10 */
  set_imask(0x0);
  while(1);                             /* Loop */
 }
```

```
void dma_rdr(void)                          /* DMAC ch1  innterrupt routine */
 {                                          /* DMAC ch1 data taransfer end */
  P_DMAC0.CHCR0.LONG &= 0xfffffffd;         /* Clear flag */
  P_SCI1.SCR_1.BYTE = 0xa0;                 /* Enable SCI ch1 transfer & transfer
                                               data empty interrupt */
  P_DMAC3.SAR3 = (long)(&dat.addr0);        /* DMAC ch3 source address */
  P_DMAC3.DMATCR3 = 0x01;                   /* DMAC ch3 transfer count =1 */
  P_DMAC3.CHCR3.LONG |= 0x00000001;         /* DMAC ch3 enable*/
 }

void dma_tdr(void)                          /* DMAC ch3 interrupt routine*/
 {                                          /* DMAC ch1 data transfer end*/
  P_DMAC3.CHCR3.LONG &= 0xfffffffc;         /* Clear flag */
  P_SCI1.SCR_1.BYTE = 0x70;                 /* Enable SCI ch1 receive data & receive
                                               data full interrupt */
  P_DMAC0.DAR0 = (long)(&dat.addr0);        /* DMAC ch0 destination address */
  P_DMAC0.DMATCR0 = 0x04;                   /* DMAC ch3 transfer count =4 */
 }
```

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