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SH7144/45 Group

PWM 4-Phase Output

1. Specifications

Using MTU PWM mode 1, 4-phase PWM output is performed based on a set duty cycle and period.

In PWM mode 1, an arbitrary period can be set for each channel. Two outputs are possible for each of ch0, ch3, and ch4, and one output for each of ch1 and ch2. Thus for ch0, ch3, and ch4, waveforms can be generated with a different high width within the same period.

A duty cycle of 0% to 100% can be set with a 1/65,535 resolution.

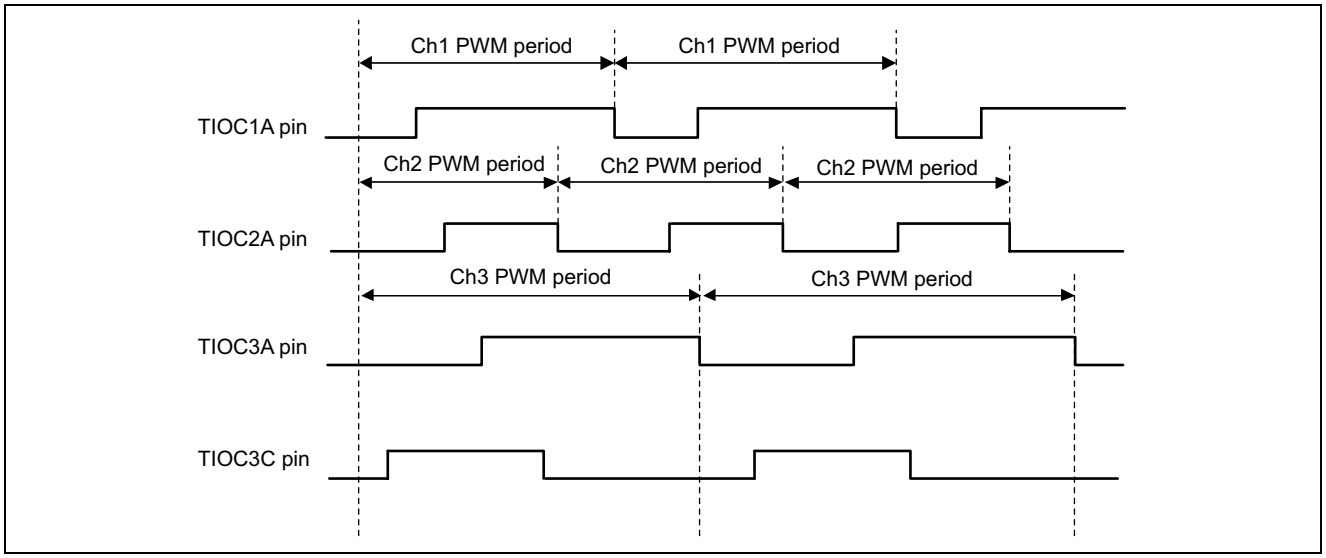


Figure 1 Example of PWM Output

2. Functions Used

In this sample task, 4-phase PWM output is performed using MTU ch1 to ch3.

In PWM mode 1, PWM output is generated with TGRA paired with TGRB, and TGRC paired with TGRD. By using ch0 to ch4, a maximum of 8-phase PWM output is possible.

Figure 2 shows a block diagram of the MTU as used in this sample task.

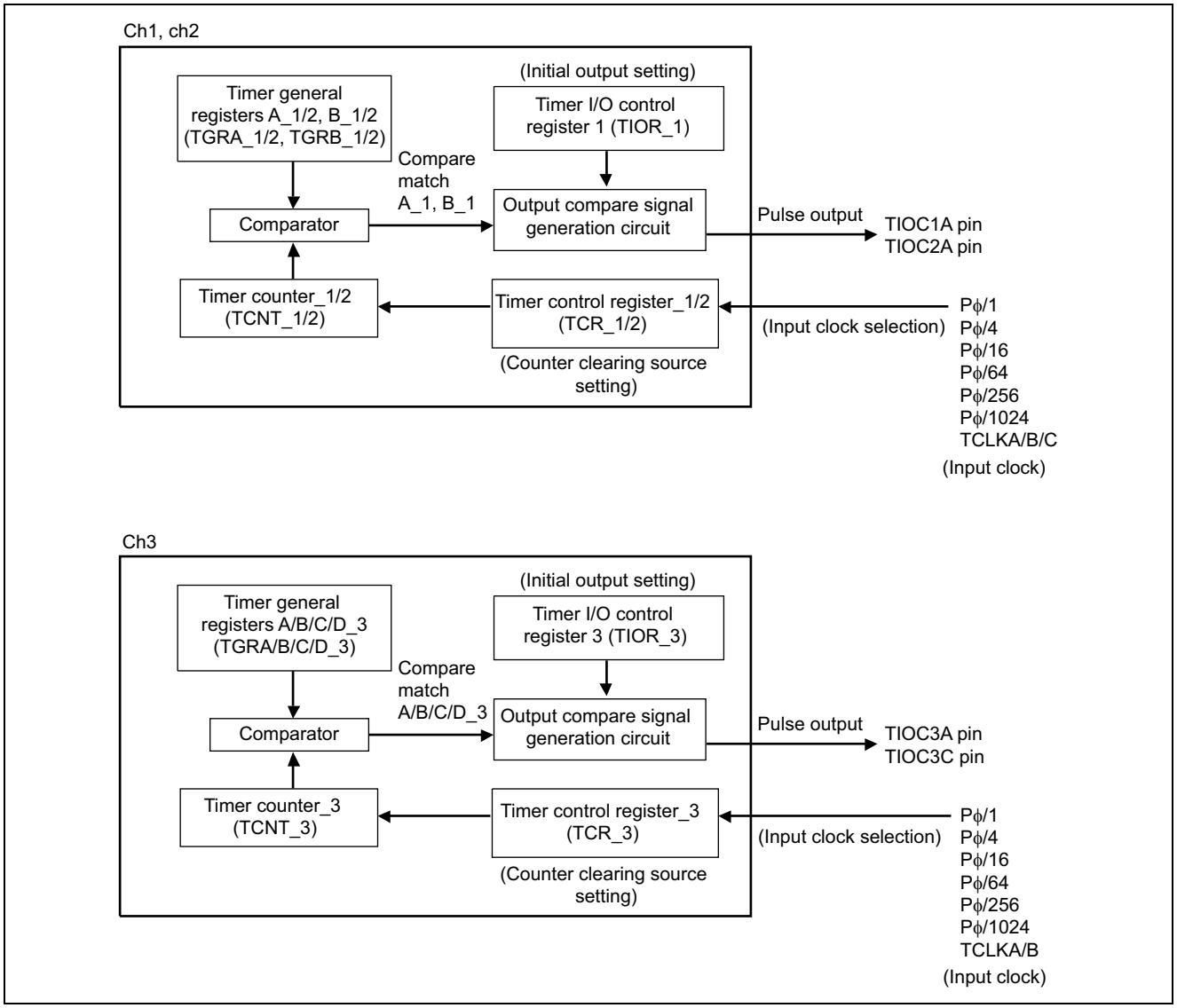


Figure 2 Block Diagram of MTU/ch1, ch2, ch3

Table 1 shows the function assignments used in this sample task. PWM pulses are output by assigning MTU functions as shown in the table.

Table 1 Function Assignments

Pin or Register Name	Function Assignment
TIOC1A TIOC2A TIOC3A TIOC3C	PWM pulse output pins
TCR_1 TCR_2 TCR_3	Selection of ch1 to ch3 timer counter clearing sources and input clocks
TMDR_1 TMDR_2 TMDR_3	Operation of ch1 to ch3 in PWM mode 1
TGRA_1 TGRA_2 TGRA_3	PWM period setting
TGRB_1 TGRB_2 TGRB_3 TGRC_3 TGRD_3	Duty cycle setting

3. Principles of Operation

Figure 3 illustrates the principles of operation of this sample task. Four-phase PWM output is performed from the ch1 to ch3 PWM output pins (TIOC1A, TIOC2A, TIOC3A/C) by SH7145 hardware and software processing as shown in the figure.

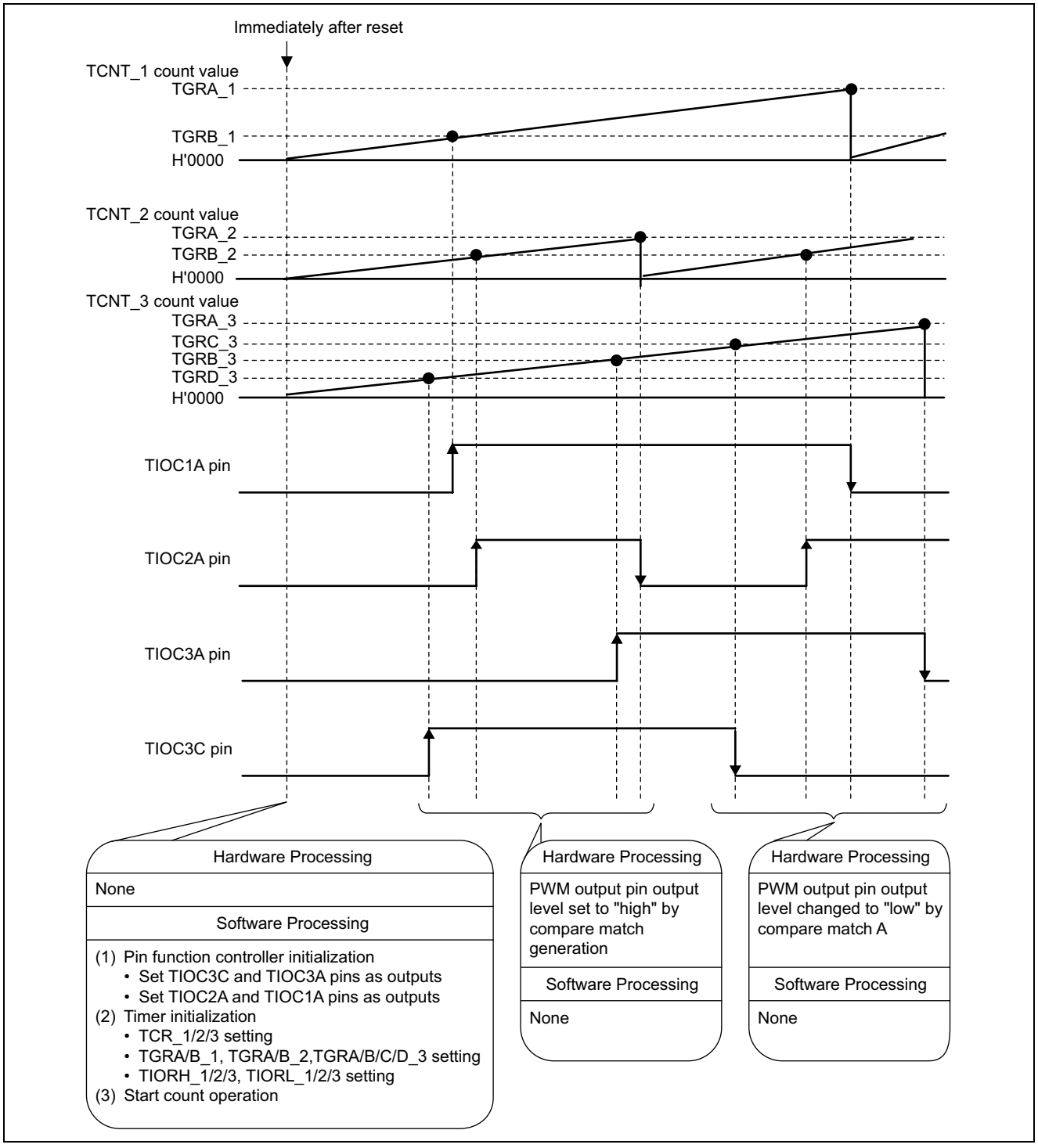


Figure 3 Principles of Operation of PWM Waveforms

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	pwm_1	PFC and PWM output setting

(2) Arguments

Label or Register Name	Function Assignment	Data Length	Module	Input/Output
pul_cyc1 pul_cyc2 pul_cyc3	Used to set timer value for pulse period Pulse period is calculated using following equation: Pulse period (ns) = timer value × ϕ period (25 ns at 40 MHz operation)	1 word	Main routine	Input
pul_duty1b pul_duty2b pul_duty3b pul_duty3c pul_duty3d	Used to set TIOC pin output waveform transition timing			

(3) Internal Registers Used

Register Name	Function Assignment	Address	Set Value
P_STBY.MSTCR2	MTU module standby mode clearing	H'FFFF861E	H'd0fd
P_MTU1.TCR_1 P_MTU2.TCR_2 P_MTU3.TCR_3	Timer counter clearing sources cleared by TGRA_1, TGRA_2, TGRA_3 compare matches Pϕ/16 selected as input clock	H'FFFF8280 H'FFFF82A0 H'FFFF8200	H'22 H'22 H'22
P_MTU1.TGRA_1	Channel 1 PWM period setting	H'FFFF8288	pul_cyc1
P_MTU1.TGRB_1	Used to set timer counter value causing high output from TIOC1A	H'FFFF828A	pul_duty1b
P_MTU2.TGRA_2	Channel 2 PWM period setting	H'FFFF82A8	pul_cyc2
P_MTU2.TGRB_2	Used to set timer counter value causing high output from TIOC2A	H'FFFF82AA	pul_duty2b
P_MTU34.TGRA_3	Channel 3 PWM period setting	H'FFFF8218	pul_cyc3
P_MTU34.TGRB_3	Used to set timer counter value causing high output from TIOC3A	H'FFFF821A	pul_duty3b
P_MTU34.TGRC_3	Used to set timer counter value causing low output from TIOC3C	H'FFFF8224	pul_duty3c
P_MTU34.TGRD_3	Used to set timer counter value causing high output from TIOC3C	H'FFFF8226	pul_duty3d
P_MTU1.TIOR_1	Sets TGRA_1 initial output 0, 0 output on output compare, TGRB_1 initial output 0, 1 output on output compare	H'FFFF8282	H'21
P_MTU2.TIOR_2	Sets TGRA_2 initial output 0, 0 output on output compare, TGRB_2 initial output 0, 1 output on output compare	H'FFFF82A2	H'21
P_MTU34.TIORH_3	Sets TGRA_3 initial output 0, 0 output on output compare, TGRB_3 initial output 0, 1 output on output compare	H'FFFF8204	H'21

Register Name	Function Assignment	Address	Set Value
P_MTU34.TIORL_3	Sets TGRC_3 initial output 0, 0 output on output compare, TGRD_3 initial output 0, 1 output on output compare	H'FFFF8205	H'21
P_MTU1.TMDR_1	Set PWM mode 1 as operating mode	H'FFFF8281	H'c2
P_MTU2.TMDR_2		H'FFFF82A1	H'c2
P_MTU34.TMDR_3		H'FFFF8202	H'c2

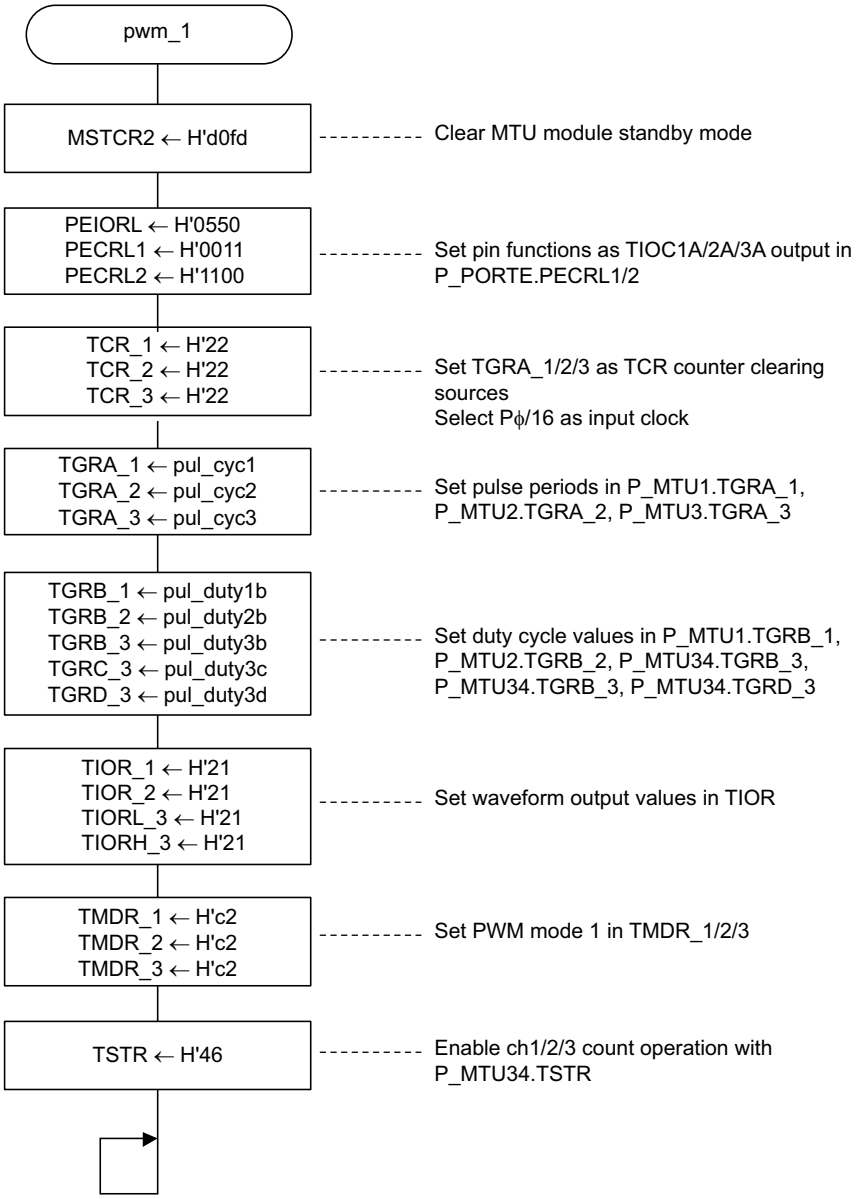
(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7145 header file names are used for register label names.

5. Flowcharts

(1) Main routine



6. Program Listing

```
/************************************************************************/
/*                                INCLUDE FILE                          */
/************************************************************************/
#include<machine.h>
#include"iodefine_7145F.h"
/************************************************************************/
/*                                PROTOTYPE                             */
/************************************************************************/
void pwm_1(void);
/************************************************************************/
/*                              RAM ALLOCATION                          */
/************************************************************************/
#define  pul_cyc1     (*(unsigned short  *)0xffffe000)
#define  pul_duty1b   (*(unsigned short  *)0xffffe002)
#define  pul_cyc2     (*(unsigned short  *)0xffffe004)
#define  pul_duty2b   (*(unsigned short  *)0xffffe006)
#define  pul_cyc3     (*(unsigned short  *)0xffffe008)
#define  pul_duty3b   (*(unsigned short  *)0xffffe00a)
#define  pul_duty3c   (*(unsigned short  *)0xffffe00c)
#define  pul_duty3d   (*(unsigned short  *)0xffffe00e)
/************************************************************************/
/*                             MAIN PROGRAM                             */
/************************************************************************/
void pwm_1(void)
 {
    P_STBY.MSTCR2.WORD = 0xd0fd;      /* Clear module standby mode */
    P_PORTE.PEIORL.WORD = 0x0550;     /* TIOC1A/2A/3A/3C = output */
    P_PORTE.PECRL1.WORD = 0x0011;
    P_PORTE.PECRL2.WORD = 0x1100;

    P_MTU1.TCR_1.BYTE = 0x22;         /* Counter1 clear by TGRA_1 */
    P_MTU2.TCR_2.BYTE = 0x22;         /* Counter2 clear by TGRA_2 */
    P_MTU34.TCR_3.BYTE = 0x22;        /* Counter3 clear by TGRA_3 */

    P_MTU1.TGRA_1 = pul_cyc1;         /* set TIOC1A period */
    P_MTU2.TGRA_2 = pul_cyc2;         /* set TIOC2A period */
    P_MTU34.TGRA_3 = pul_cyc3;        /* set TIOC3A period */
    P_MTU1.TGRB_1 = pul_duty1b;       /* set TIOC1A duty */
    P_MTU2.TGRB_2 = pul_duty2b;       /* set TIOC2A duty */
    P_MTU34.TGRB_3 = pul_duty3b;      /* set TIOC3A duty */
    P_MTU34.TGRC_3 = pul_duty3c;      /* set TIOC3C duty */
    P_MTU34.TGRD_3 = pul_duty3d;      /* set TIOC3C duty */
    P_MTU1.TIOR_1.BYTE = 0x21;        /* start"0",compare match"1"output*/
    P_MTU2.TIOR_2.BYTE = 0x21;        /* start"0",compare match"1"output*/
    P_MTU34.TIORL_3.BYTE = 0x21;      /* start"0",compare match"1"output*/
    P_MTU34.TIORH_3.BYTE = 0x21;      /* start"0",compare match"1"output*/
    P_MTU1.TMDR_1.BYTE = 0xc2;        /* PWM mode1 */
    P_MTU2.TMDR_2.BYTE = 0xc2;        /* PWM mode1 */
    P_MTU34.TMDR_3.BYTE = 0xc2;       /* PWM mode1 */

    P_MTU34.TSTR.BYTE = 0x46;         /* Timer counter start */
    while(1);
  }
```

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