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Renesas Electronics Corporation

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SH7046 Group

Externally Triggered Timer Waveform Cutoff

1. Specifications

Timer output waveform cutoff is performed by driving timer output waveforms to the high-impedance state in synchronization with the falling edge of an external signal, as shown in figure 1.

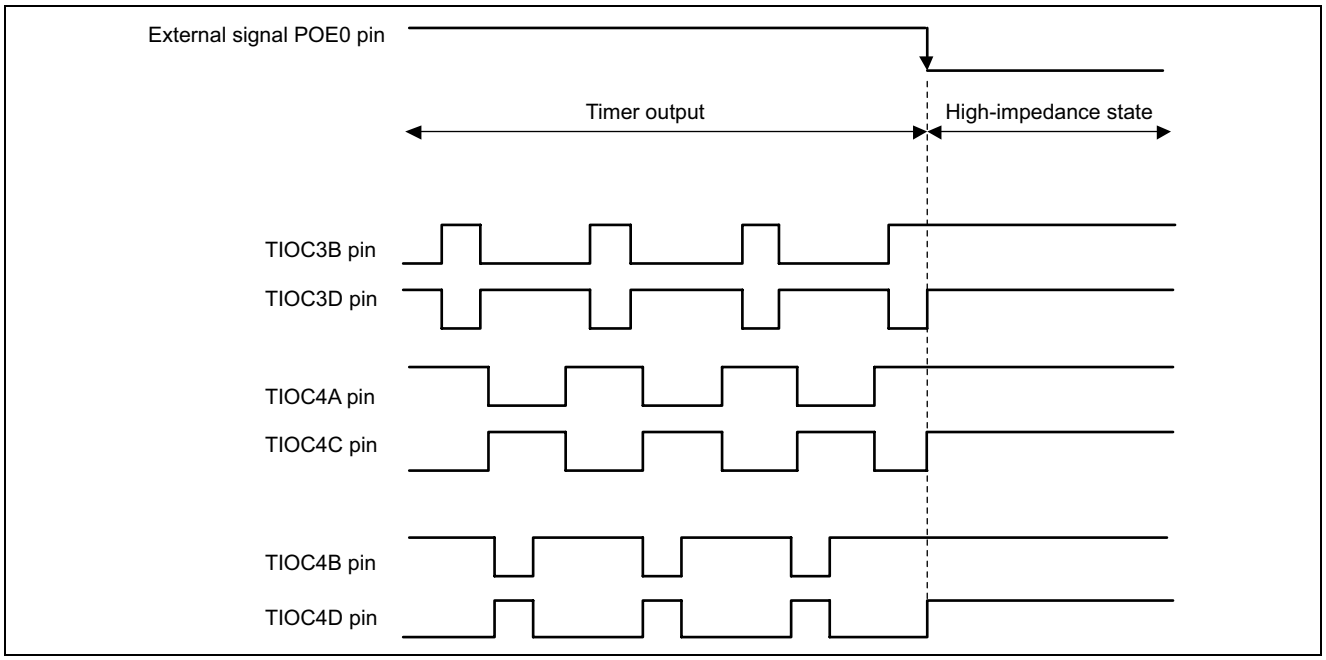


Figure 1 Example of Externally Triggered Waveform Cutoff

2. Functions Used

In this sample task, waveforms output by MTU ch3/4 (reset-synchronized PWM mode) are cut by being driven to the high-impedance state in synchronization with the falling edge of an external signal.

Figure 2 shows a block diagram of MTU/ch3 and ch4, and the POE.

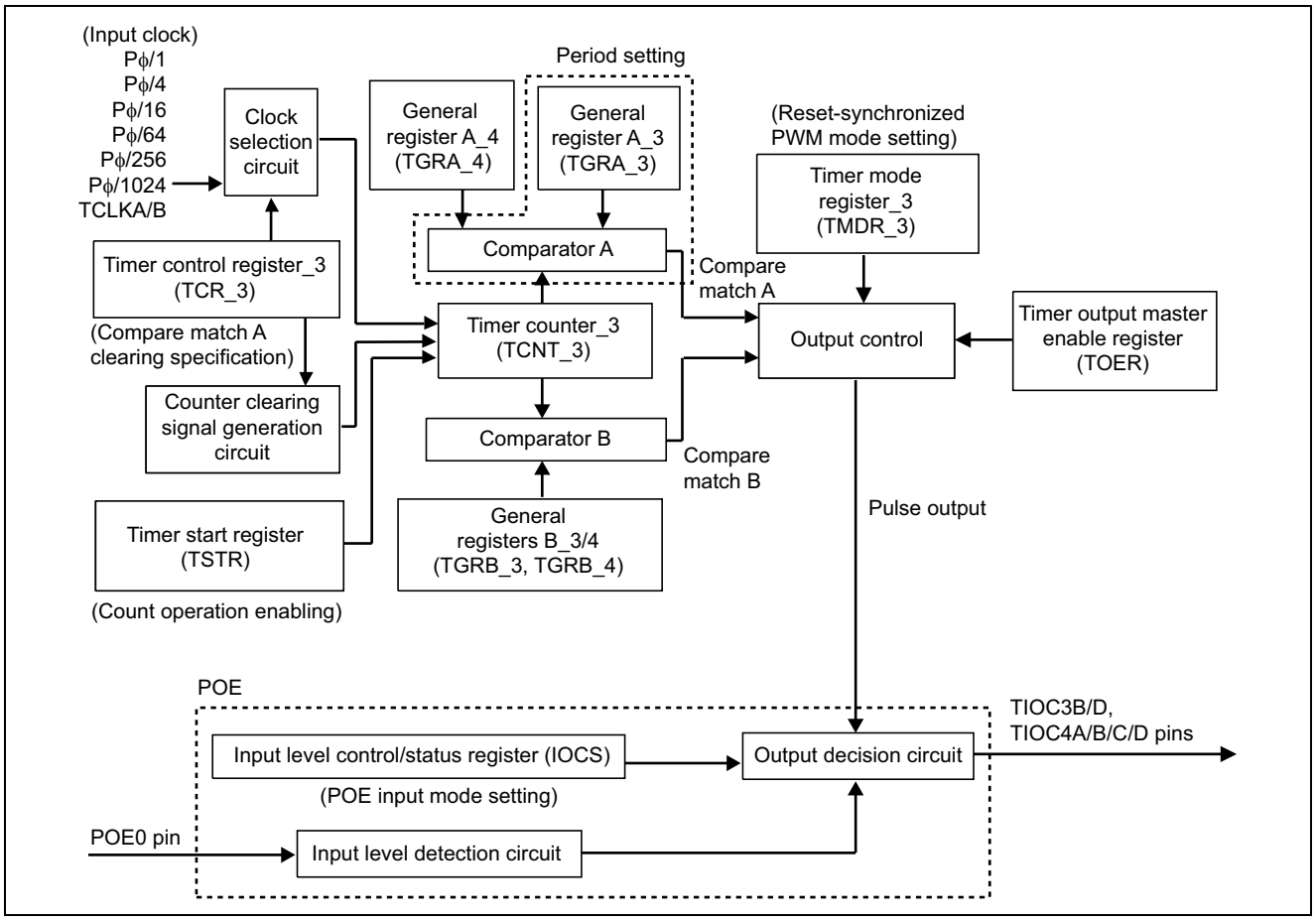


Figure 2 Block Diagram of MTU/ch3, ch4, and POE

Table 1 shows the function assignments used in this task. Waveform cutoff is performed by assigning MTU and POE functions as shown in the table.

Table 1 Function Assignments

Pin or Register Name	Function	Function Assignment
TIOC3B	Pins	Pulse output pins
TIOC3D		
TIOC4A		
TIOC4B		
TIOC4C		
TIOC4D		
POE0	Pin	Waveform cutoff external signal input pin
TSTR_3	Register	Enabling/disabling of ch3 timer counter operation
TCR_3	Register	Selection of ch3 timer counter clearing source and input clock
TMDR_3	Register	Sets reset-synchronized PWM mode for ch3, ch4
TGRA_3	Register	PWM period setting
TGRB_3	Registers	Output waveform transition timing setting
TGRA_4		
TGRB_4		
TOER	Register	Enabling/disabling of TIOC3B/D and TIOC4A/B/C/D pin timer output
ICSR	Register	POE input mode selection

3. Operation

Figure 3 illustrates the principles of operation of this sample task. Waveform cutoff is performed automatically by hardware. (See the section on positive-phase/negative-phase PWM 3-phase output in this Application Note for information on the principles of reset-synchronized PWM operation.)

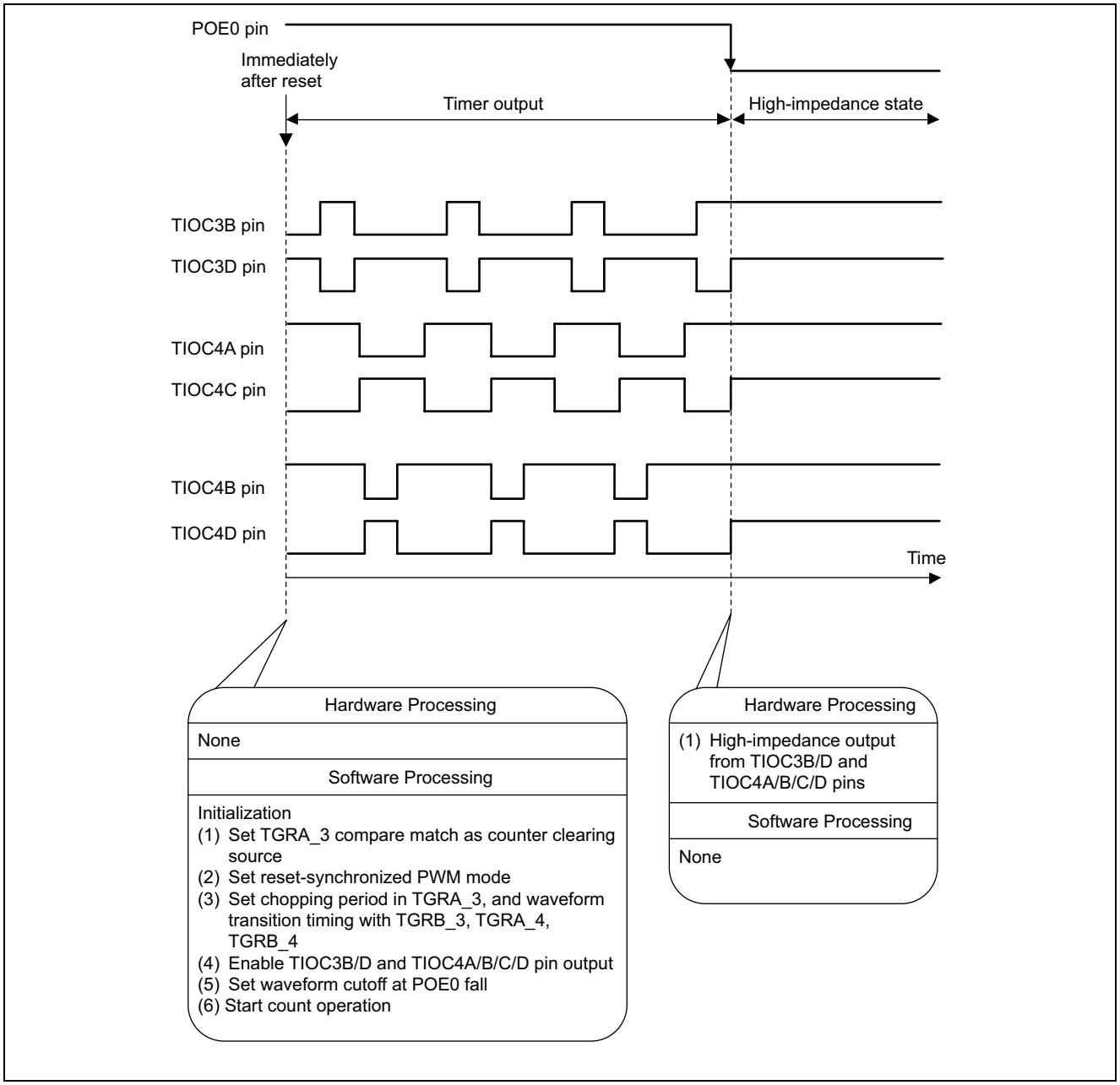


Figure 3 Principles of Operation of Externally Triggered Waveform Cutoff

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	down	DC motor control waveform generation

(2) Arguments

Label or Register Name	Function Assignment	Data Length	Module	Input/ Output
cycle	PWM period setting	1 word	Main routine	Input
duk1	Used to set TIOC3B/D output waveform transition timing			
duk2	Used to set TIOC4A/C output waveform transition timing			
duk3	Used to set TIOC4B/D output waveform transition timing			

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_STBY.MSTCR2	MTU module standby mode clearing, and setting of MTU to operational status	H'FFFF861E	H'd2fd
P_PORTE.PEIORL	Sets TIOC3B/D, TIOC4A/B/C/D as output pins	H'FFFF83B4	H'fa00
P_PORTE.PECRL1	Sets TIOC3B/D, TIOC4A/B/C/D as MTU output pins	H'FFFF83B8	H'5544
P_PORTB.PBCR2	Sets POE0 pin	H'FFFF839A	H'0020
P_MTU34.TCR_3	Selection of timer counter clearing source and input clock	H'FFFF8200	H'20
P_MTU34.TOCR	Enabling of toggle output synchronized with PWM period, and positive-phase/negative-phase output level setting	H'FFFF820B	H'00
P_MTU34.TGRA_3	PWM period setting	H'FFFF8218	cycle
P_MTU34.TGRB_3	Used to set TIOC3B, TIOC3D output waveform transition timing	H'FFFF821A	duk1
P_MTU34.TGRA_4	Used to set TIOC4A, TIOC4C output waveform transition timing	H'FFFF821C	duk2
P_MTU34.TGRB_4	Used to set TIOC4B, TIOC4D output waveform transition timing	H'FFFF821E	duk3
P_MTU34.TOER	Sets TIOC3B/D, TIOC4A/B/C/D as MTU output pins	H'FFFF820A	H'ff
P_MTU34.TMDR_3	Sets reset-synchronized PWM mode	H'FFFF8202	H'c8
P_MTU.ICSR1	Sets high-impedance output synchronized with falling edge of POE0 pin input signal	H'FFFF83C0	H'0000

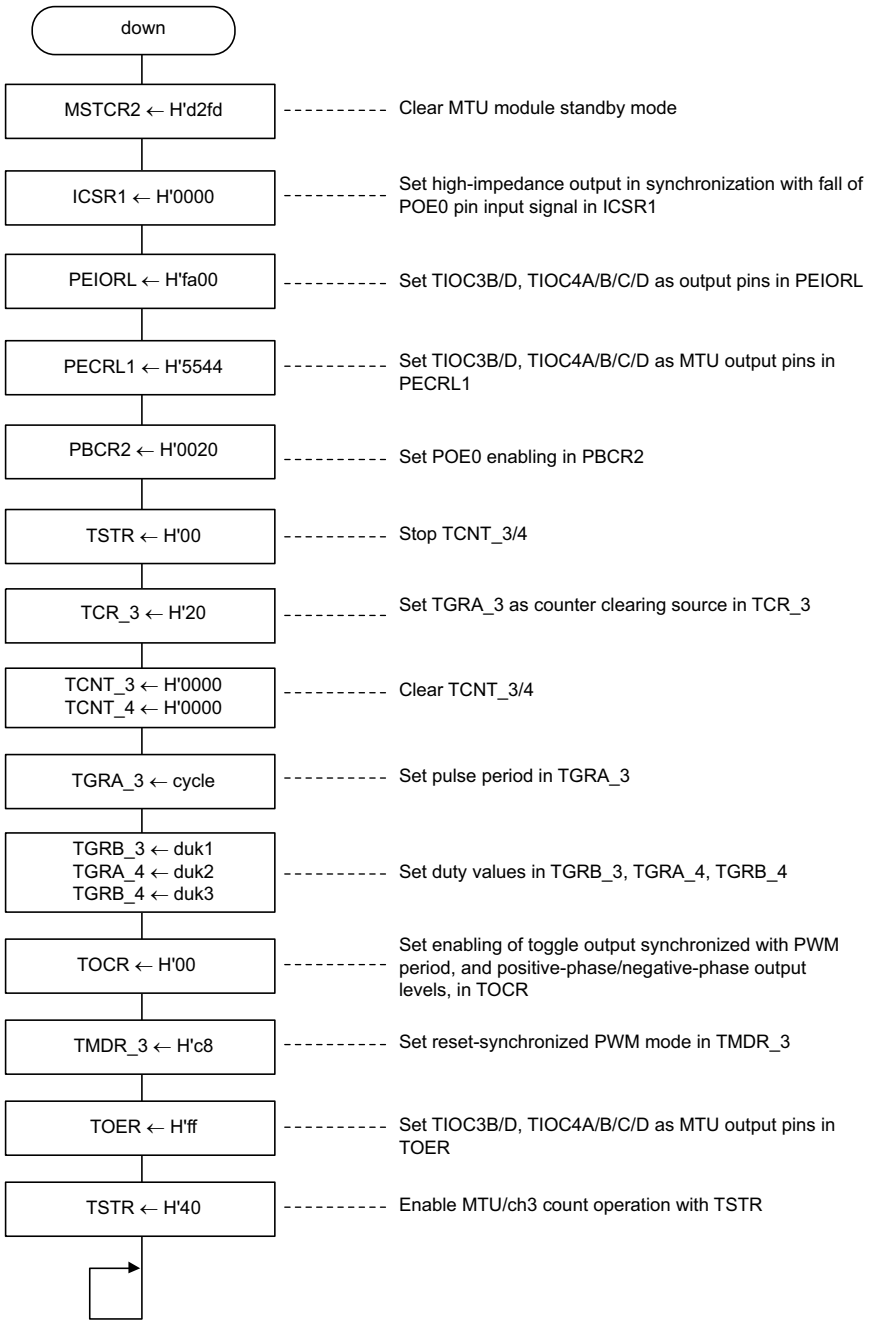
(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7046 header file names are used for register label names.

5. Flowcharts

(1) Main routine



6. Program Listing

```
/*----------------------------------------------------------------------*/
/*                            INCLUDE FILE                              */
/*----------------------------------------------------------------------*/
#include <machine.h>
#include "iodefine_7046.h"
/*----------------------------------------------------------------------*/
/*                            PROTOTYPE                                 */
/*----------------------------------------------------------------------*/
void down(void);
/*----------------------------------------------------------------------*/
/*                         RAM ALLOCATION                               */
/*----------------------------------------------------------------------*/
#define cycle   (*(unsigned short *)0xffffd000)
#define duk1    (*(unsigned short *)0xffffd002)
#define duk2    (*(unsigned short *)0xffffd004)
#define duk3    (*(unsigned short *)0xffffd006)
/*----------------------------------------------------------------------*/
/*                           MAIN PROGRAM                               */
/*----------------------------------------------------------------------*/
void down(void)
{
  P_STBY.MSTCR2.WORD = 0xd2fd;        /* MTU module stop mode clear */

  P_PORTE.PEIORL.WORD = 0xfa00;       /* TIOC3B/D,TIOC4A/B/C/D output */
  P_PORTE.PECRL1.WORD = 0x5544;       /* TIOC3B/D,TIOC4A/B/C/D output */
  P_PORTB.PBIOR.WORD = 0x0000;        /* POE enable */
  P_PORTB.PBCR1.WORD = 0x0000;        /* POE enable */
  P_PORTB.PBCR2.WORD = 0x0020;        /* POE enable */

  P_MTU.ICSR1.WORD = 0x0000;    /* stop timer POE0 falling edge */
  P_MTU.OCSR.WORD = 0x0000;

  P_MTU34.TSTR.BYTE = 0x00;
  P_MTU34.TCR_3.BYTE = 0x20;    /* timer clear input caputure TGRA_3 */

  P_MTU34.TCNT_3 = 0x0000;      /* set timer counter3 0x0000 */
  P_MTU34.TCNT_4 = 0x0000;      /* set timer counter4 0x0000 */
  P_MTU34.TGRA_3 = cycle;       /* period set */
  P_MTU34.TGRB_3 = duk1;        /* duty set */
  P_MTU34.TGRA_4 = duk2;
  P_MTU34.TGRB_4 = duk3;

  P_MTU34.TOCR.BYTE = 0x00;     /* set output level */
  P_MTU34.TMDR_3.BYTE = 0xc8;   /* reset-synchronized pwm mode */
  P_MTU34.TOER.BYTE = 0xff;     /* set timer3,4 output */
  P_MTU34.TSTR.BYTE = 0x40;     /* start timer3 */

  while(1);   /* loop */
 }
```

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