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April 1st, 2010
Renesas Electronics Corporation

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SH7046 Group

2-Phase Encoder Count

1. Specifications

Two external clocks are input to channel 1 (ch1), and a counter is incremented or decremented according to the phase difference of the pulses, as shown in figure 1. The ch1 count is measured in synchronization with measurement times set in ch0 (measurement times 1 and 2), and the result is set in RAM.

H'0000 is set as the timer counter initial value, and counting can be performed from -2,147,483,648 to 2,147,483,647 using a software counter.

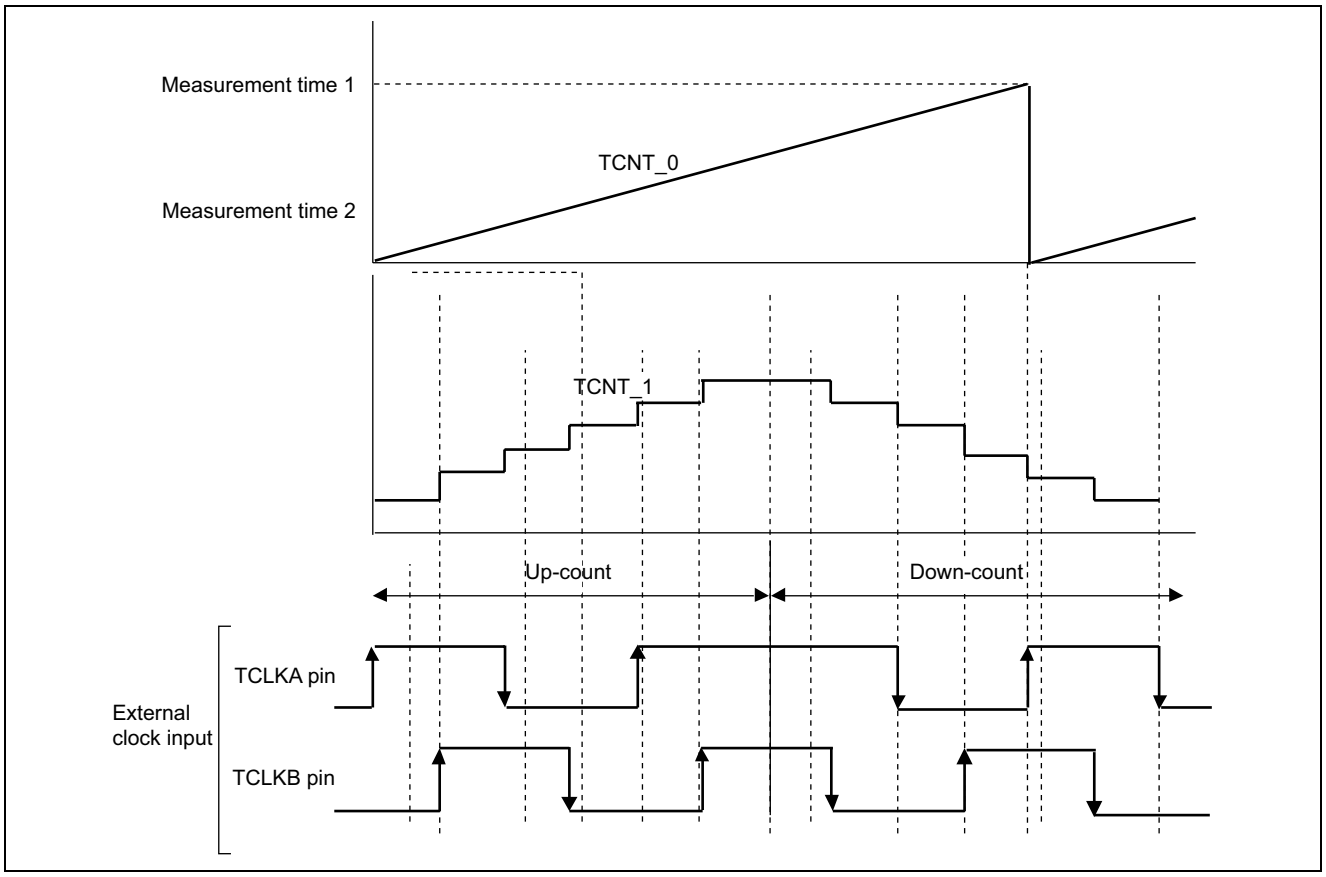


Figure 1 2-Phase Encoder Counter Capture

2. Functions Used

In this sample task, measurement times are set in TGRA/B_0 using an MTU ch1 up/down-counter.

Using a TGRA/B_0 output compare as a trigger, the TCNT_1 value for the control period is captured by ch1 input capture. In addition, the ch1 counter input clock width is captured using ch0 input capture.

Figure 2 shows a block diagram of ch0. In ch0, a ch1 input capture trigger is output every measurement time using the following functions. In ch1, the TCNT_1 value is measured when an input capture signal is input.

- A function that outputs pulses automatically by hardware without software intervention (output compare)
- A function that performs pulse input edge detection, and captures a timer value in an internal register (input capture)

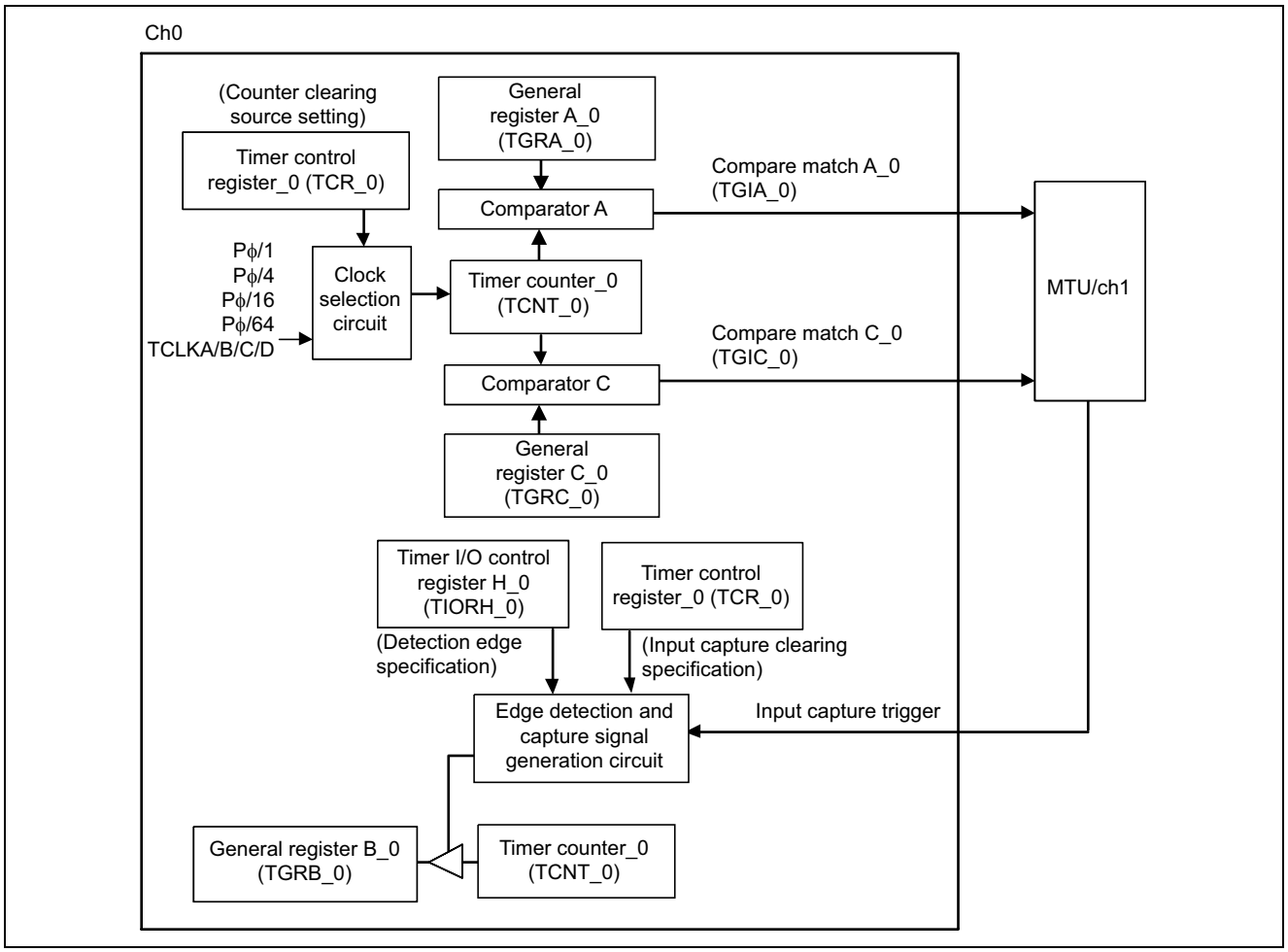


Figure 2 Block Diagram of MTU/ch0

Figure 3 shows a block diagram of ch1. In ch1, a timer counter is incremented/decremented using the following functions. The counter value when an input capture signal rising edge is detected is taken as the measurement result.

- A function that detects the phase difference between two external clocks, and increments/decrements a timer counter (phase counting mode)
- A function that performs pulse input edge detection, and captures the timer value at that point in an internal register (input capture)
- A function that initiates interrupt handling when input capture occurs
- A function that clears the timer counter when a pulse input edge is detected
- A function that initiates interrupt handling when timer counter overflow or underflow is detected

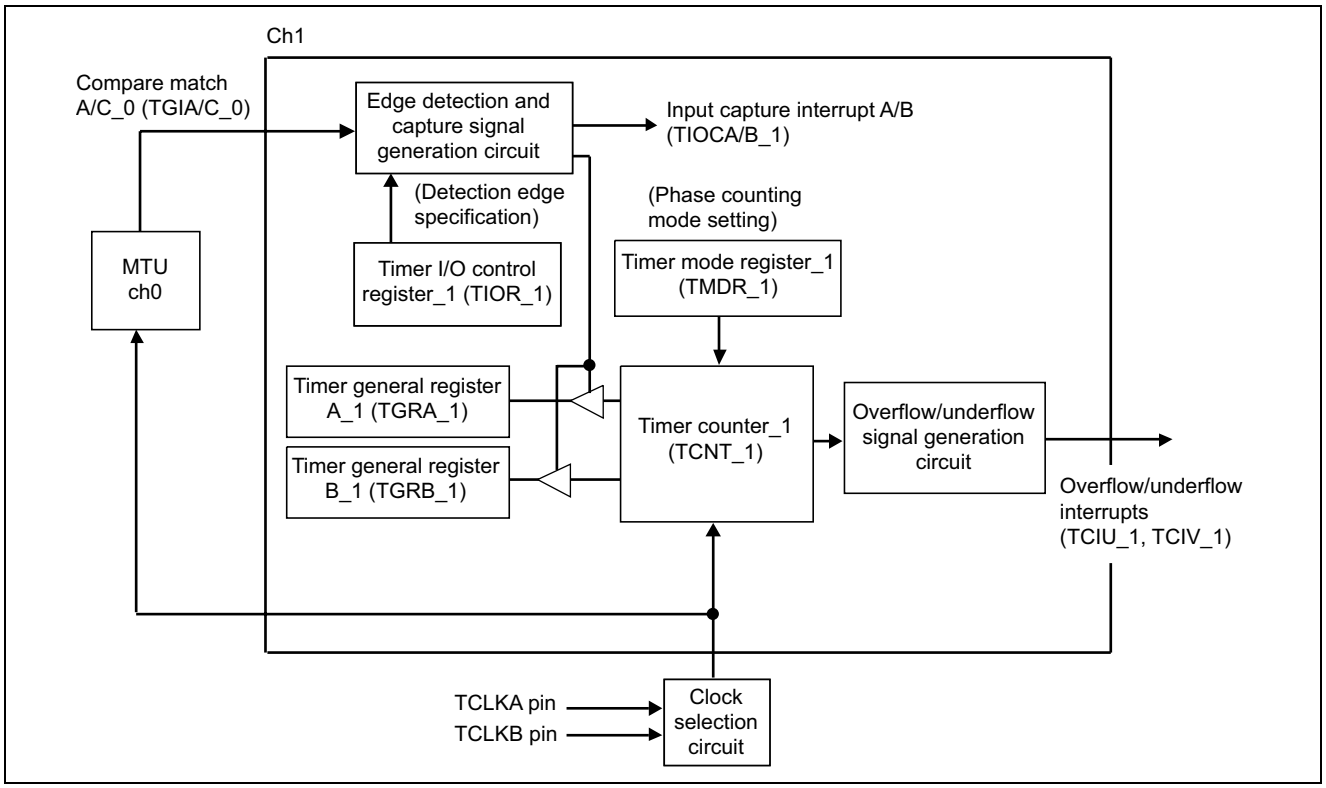


Figure 3 Block Diagram of MTU/ch1

Table 1 shows the function assignments used in this sample task. MTU functions are assigned as shown in the table to detect the phase difference between two 2-phase encoder pulses, and increment/decrement a counter.

Table 1 Function Assignments

Pin or Register Name	Function	Function Assignment
TCLKA	Pin	External clock input pins
TCLKB	Pin	
TSTR	Register	Enabling/disabling of ch0, ch1 timer counter operation
TCR_0	Register	Selection of counter clock and counter clearing source
TIORH_0	Register	TIOC0A output compare setting. Setting of TIOC0B for input capture on ch0 output compare occurrence
TIORL_0	Register	TIOC0C output compare setting
TGRA_0	Register	Measurement time 1 setting
TGRB_0	Register	Count result stored on input capture B
TGRC_0	Register	Measurement time 2 setting
TMDR_1	Register	Phase counting mode setting
TCR_1	Register	Selection of counter clock and counter clearing source
TIOR_1	Register	Setting of TIOC1A/C for input capture on ch1 output compare occurrence
TIER_1	Register	Enables TIOC1A/B, TCIU_1, TCIV_1 interrupts
TGRA_1	Register	Count result storage on input capture A
TGRB_1	Register	

3. Operation

Figure 4 illustrates the principles of operation. A counter is incremented or decremented by SH7046 hardware and software processing.

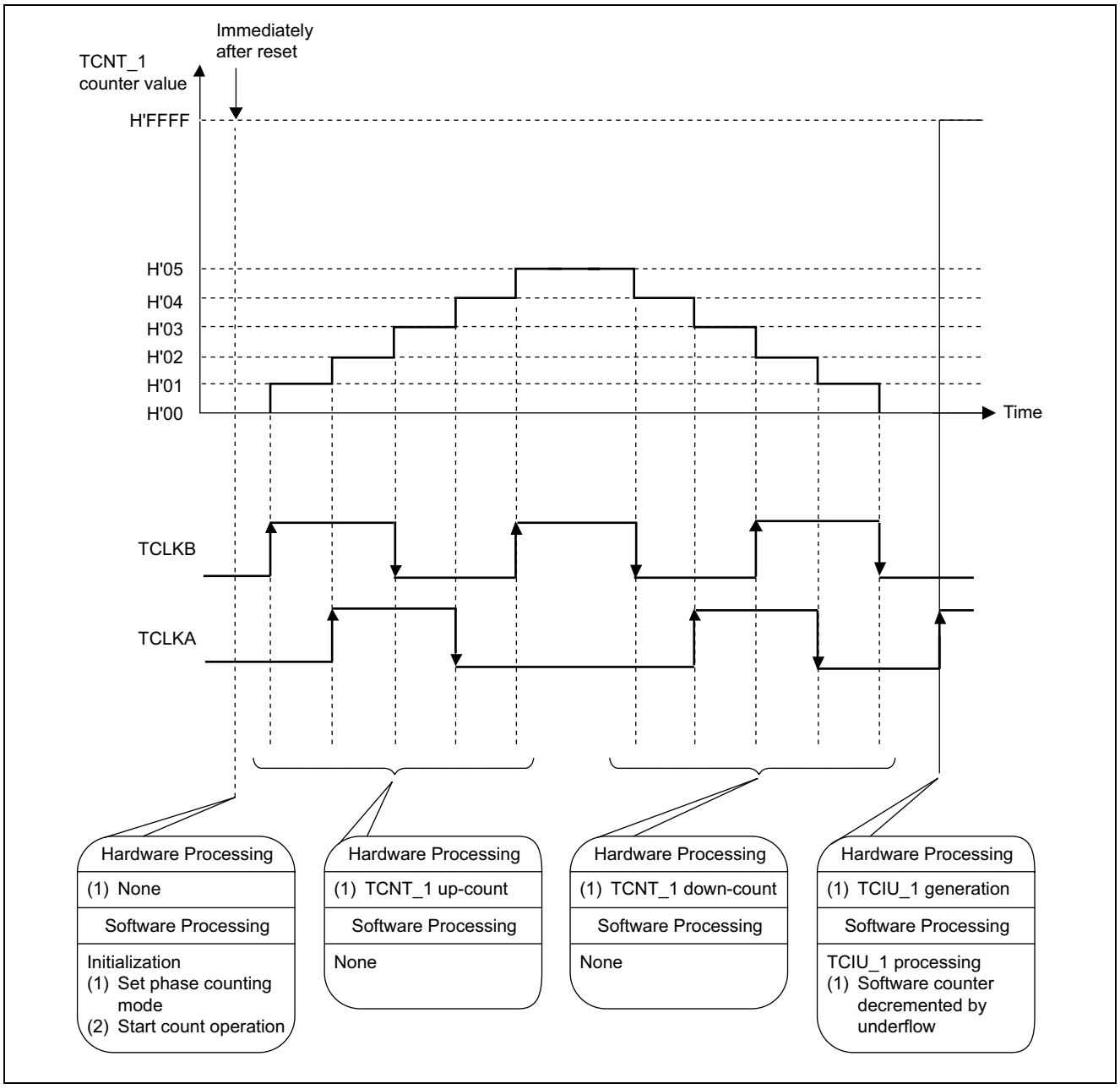


Figure 4 Principles of Operation in Phase Counting Mode (1)

Interrupt handling is executed on external event occurrence by means of SH7046 hardware and software processing as shown in figure 5.

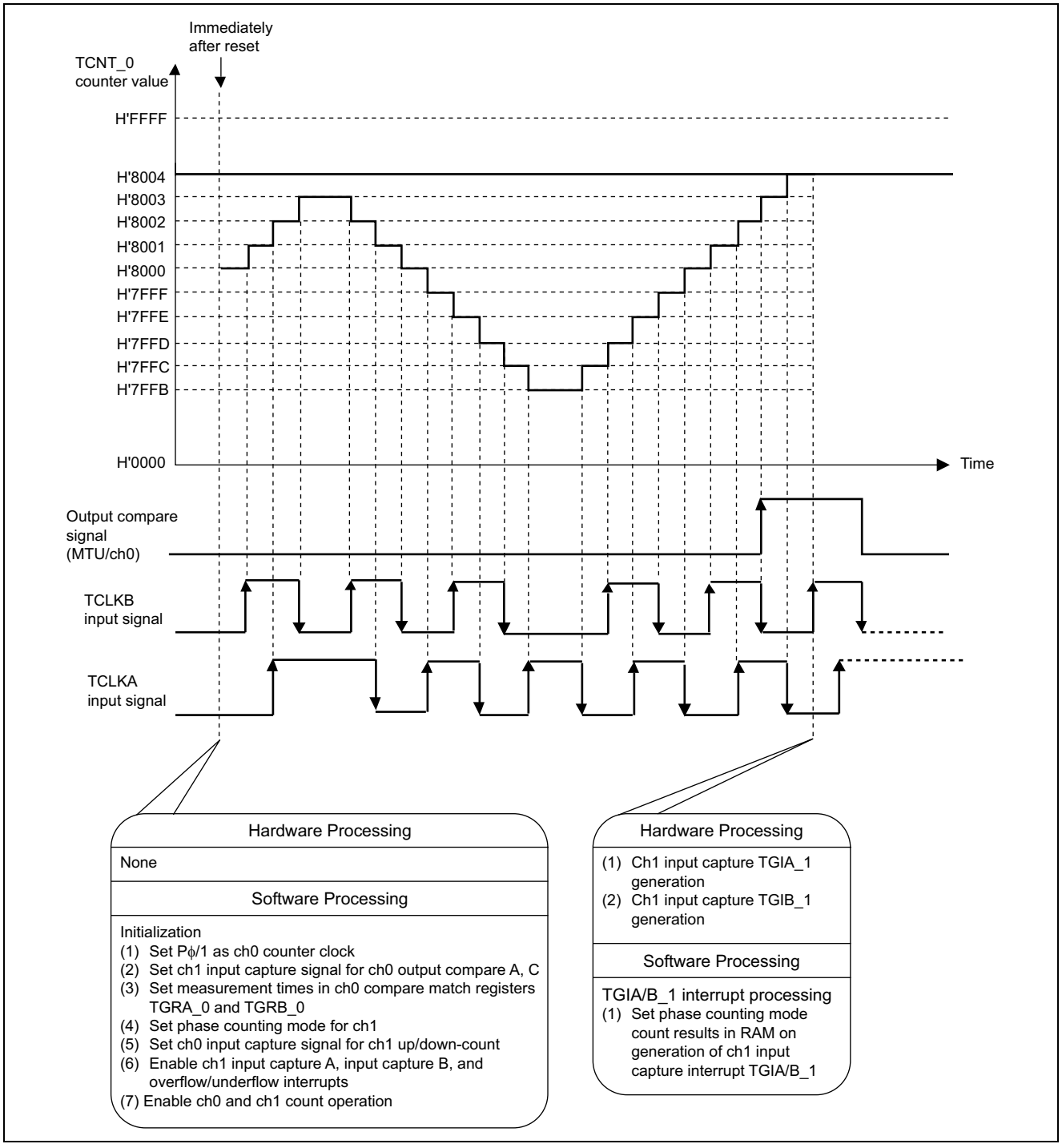


Figure 5 Principles of Operation in Phase Counting Mode (2)

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	en2	Initialization of MTU, etc.
Counter value measurement 1	phacnt1	Initiated by TGIA_1. Sets up/down-count result in RAM based on TGRA value. Sets counter period result in RAM based on TGRC value
Counter value measurement 2	phacnt2	Initiated by TGIB_1. Sets up/down-count result in RAM based on TGRB value
Overflow	ovf1	Initiated by TCIV_1. Software counter incrementing
Underflow	unf1	Initiated by TCIU_1. Software counter decrementing

(2) Arguments

Label or Register Name	Function Assignment	Data Length	Module	Input/ Output
msr_tim1 msr_tim2	Used to set timer value for counter measurement time Measurement time is calculated using following equation: Measurement time (ns) = timer value × ϕ period (50.0 ns at 20.0 MHz operation)	Word	Main routine	Input
cnt_data1 cnt_data2	Used to set up/down-count results	Longword	Counter value measurement 1 Counter value measurement 2	Output
p_cycle	Used to set count period result	Word	Counter value measurement 2	

(3) Internal Registers Used

Register Name	Function	Address	Set Value
P_STBY.MSTCR2	MTU module standby mode clearing, and setting of MTU to operational status	H'FFFF861E	H'd2fd
P_PORTA.PACRL2 P_PORTA.PACRL3	Used to set multiplex pins as timer pins TCLKA, TCLKB	H'FFFF838E H'FFFF838A	H'5000 H'0000
P_MTU0.TCR_0	Selection of counter clock and counter clearing source	H'FFFF8260	H'20
P_MTU0.TIORH_0	TIOC0A output compare setting. Setting of TIOBC0B for input capture on ch0 output compare	H'FFFF8262	H'f0
P_MTU0.TIORL_0	TIOC0C output compare setting	H'FFFF8263	H'00
P_MTU0.TGRA_0	Measurement time 1 setting	H'FFFF8268	msr_tim1
P_MTU0.TGRC_0	Measurement time 2 setting	H'FFFF826C	msr_tim2
P_MTU1.TMDR_1	Phase counting mode setting	H'FFFF8281	H'04
P_MTU0.TMDR_0	Sets buffer operation for GRD	H'FFFF8261	H'20
P_MTU1.TIOR_1	Setting of TIOC0A/C for input capture on ch1 output compare occurrence	H'FFFF8282	H'ff
P_MTU1.TIER_1	Enables interrupts by TGIA/B_1, TCIU_1, TCIV_1	H'FFFF8284	H'33
P_MTU34.TSTR	Starts ch0, ch1 timer count	H'FFFF8240	H'03
P_INTC.IPRD	Sets 15 as MTU0, MTU1 interrupt priority level	H'FFFF834E	H'00ff

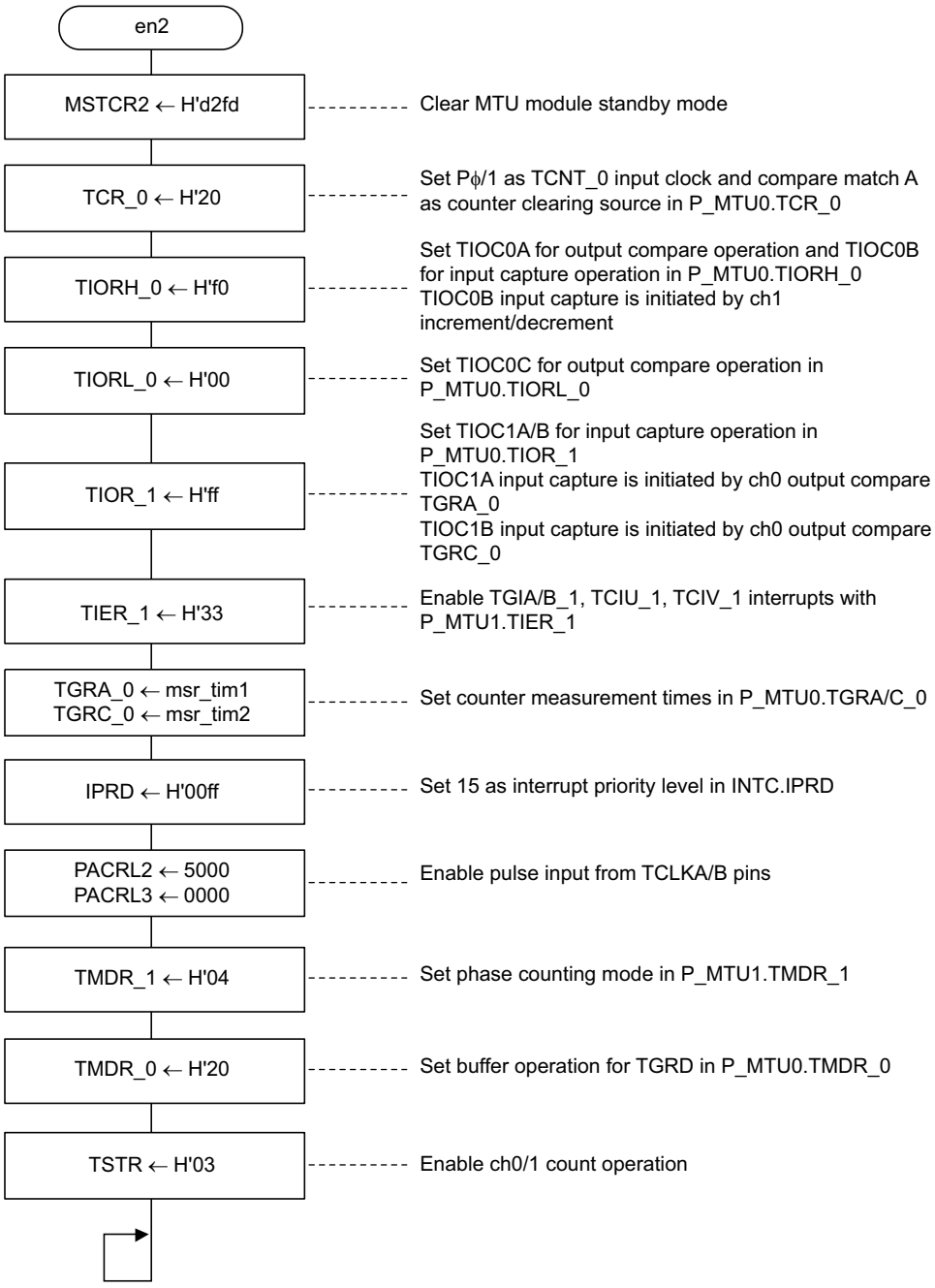
(4) RAM Used

Module	Label	Function Assignment
Counter value measurement 1, 2	wrk	Used as work area for data setting
All modules	cnt	Software counter

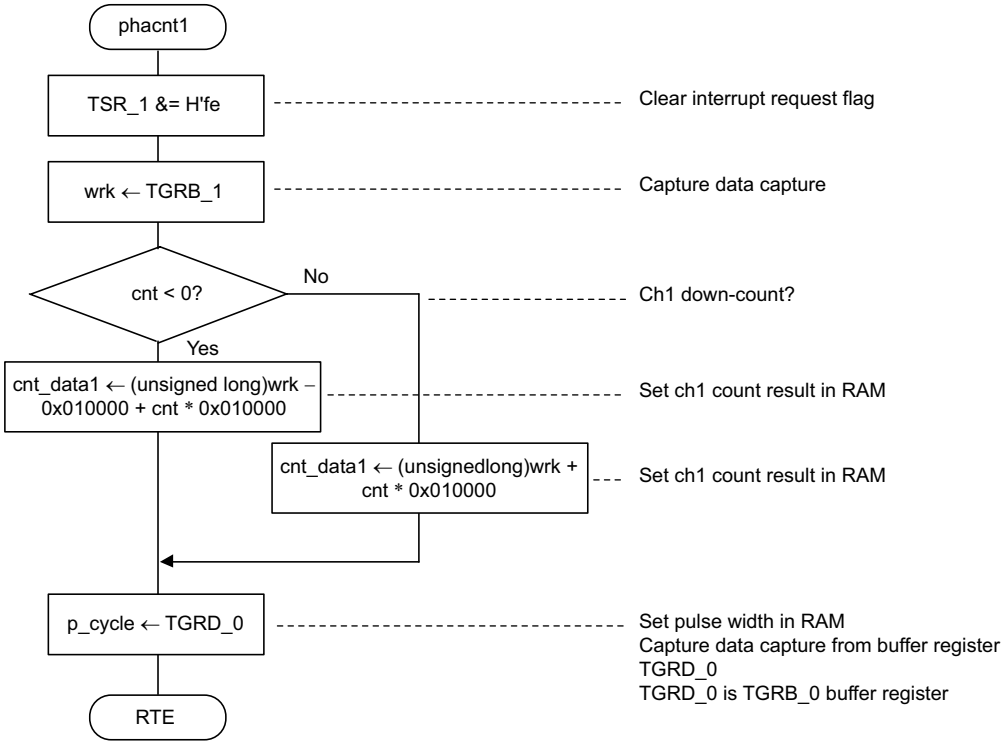
Note: SH7046 header file names are used for register label names.

5. Flowcharts

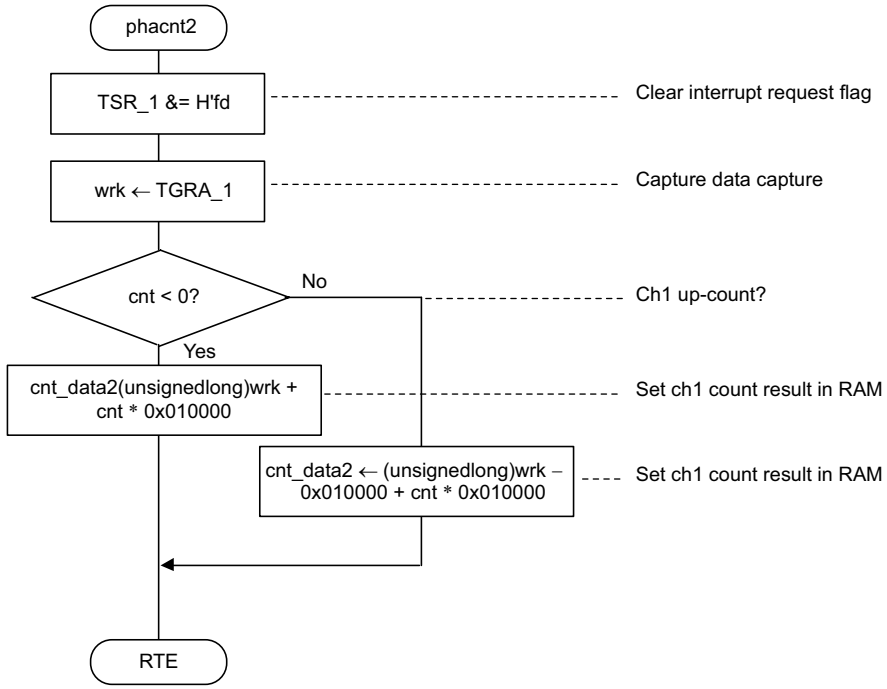
(1) Main routine



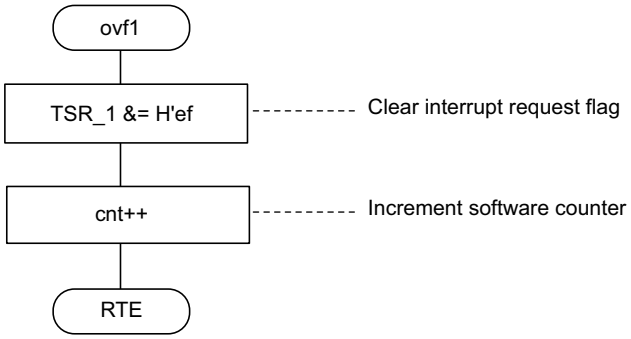
(2) Counter value measurement 1 (ch1 input capture B interrupt)



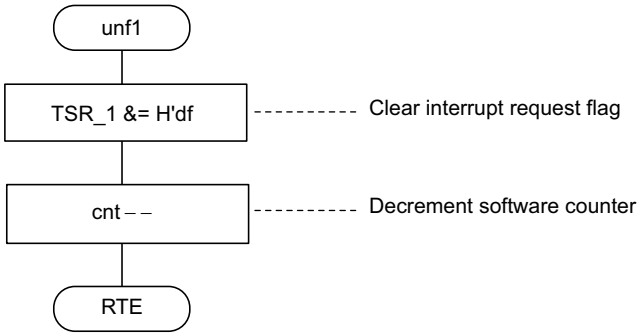
(3) Counter value measurement 2 (ch1 input capture B interrupt)



(4) Ch1 overflow interrupt



(5) Ch1 underflow interrupt



6. Program Listing

```
/*----------------------------------------------------------------------*/
/*                           INCLUDE FILE                               */
/*----------------------------------------------------------------------*/
#include <machine.h>
#include "iodefine_7046.h"
/*----------------------------------------------------------------------*/
/*                            PROTOTYPE                                 */
/*----------------------------------------------------------------------*/
void en2(void);
#pragma interrupt(phacnt1,phacnt2,ovf1,unf1)
/*----------------------------------------------------------------------*/
/*                          RAM ALLOCATION                              */
/*----------------------------------------------------------------------*/
#define msr_tim1    (*(unsigned short *)0xffffd000)
#define msr_tim2    (*(unsigned short *)0xffffd002)
#define cnt_data2   (*(signed long *)0xffffd004)
#define cnt_data1   (*(signed long *)0xffffd008)
#define p_cycle     (*(unsigned long *)0xffffd00c)
#define cnt   (*(signed long *)0xffffd010)
#define wrk   (*(unsigned short *)0xffffd014)
/*----------------------------------------------------------------------*/
/*                         MAIN PROGRAM                                 */
/*----------------------------------------------------------------------*/
void en2(void)
 {
    P_STBY.MSTCR2.WORD = 0xd2fd;      /* MTU module stop mode clear */

    P_MTU0.TCR_0.BYTE = 0x20;   /* timer clear output compare TGRA_0 */
    P_MTU0.TIORH_0.BYTE = 0xf0;       /* output compare TIOC0A */
   /* input capture TIOC0B */
    P_MTU0.TIORL_0.BYTE = 0x00;       /* output compare TIOC0C */
    P_MTU1.TIOR_1.BYTE = 0xff;        /* input capture TIOC1A,B */

    P_MTU1.TIER_1.BYTE = 0x33;        /* interrupt TIOC1A,TIOC1B,TCIU1,TCIV1 */
    P_MTU0.TGRC_0 = msr_tim2;   /* set position cycle */
    P_MTU0.TGRA_0 = msr_tim1;   /* set speed cycle */
    INTC.IPRD.WORD = 0x00ff;    /* set interrupt level=15 */

    P_PORTA.PACRL2.WORD = 0x5000;     /* TCLKA,TCLKB sellect */
    P_PORTA.PACRL3.WORD = 0x0000;

    P_MTU1.TMDR_1.BYTE = 0x04;        /* set phase counting mode1 */
    P_MTU0.TMDR_0.BYTE = 0x20;        /* TGRD buffer mode  */
    P_MTU34.TSTR.BYTE = 0x03;   /* start timer 0,1*/

    set_imask(0x0);     /* set imask level=0 */
    while(1);    /* loop*/
 }

void ovf1(void)
 {
   P_MTU1.TSR_1.BYTE &= 0xef;   /* clear flag */
```

```
    cnt++;     /* count up */
 }

void unf1(void)
 {
   P_MTU1.TSR_1.BYTE &= 0xdf;   /* clear flag */
   cnt--;     /* count down */
 }

void phacnt1(void)
 {
   P_MTU1.TSR_1.BYTE &= 0xfe;   /* clear flag */
   wrk = P_MTU1.TGRB_1;
   if(cnt < 0)   /* count < 0 */
    cnt_data1 = (unsigned long)wrk-0x010000+cnt*0x010000; /* set sp */
   else
   cnt_data1 = (unsigned long)wrk+cnt*0x010000;     /* set sp */
    p_cycle = P_MTU0.TGRD_0;    /* set width pulse */

 }

void phacnt2(void)
 {

   P_MTU1.TSR_1.BYTE &= 0xfd;   /* clear flag */
   wrk = P_MTU1.TGRA_1;
   if(cnt < 0)
    cnt_data2 = (unsigned long)wrk+cnt*0x010000;    /* set po */
     else
     cnt_data2 = (unsigned long)wrk-0x010000+cnt*0x010000;  /* set po */
 }
```

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