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H8/300H & H8/300L Super Low Power Series

Setting the Waiting Time to Cover Clock Stabilization (Timing of Reset Release and Setting of Wait States)

Introduction

The meanings of the register values used to make the wait setting for the oscillation circuits of H8/300H Super Low Power Series and H8/300L Super Low Power Series differ across the product range.

This application note describes how to set the oscillation stabilization wait times.

Contents

1. Specifications

This application note describes setting of the oscillation-stabilization waiting time with CERALOCK™ ceramic resonators (manufactured by Murata Manufacturing Co., Ltd.) mounted on the board as examples.

2. Description of Functions Code

2.1 Definition of Oscillation Stabilization Waiting Time

Figure 1 shows the oscillation waveform (OSC2), system clock (ϕ), and microcontroller operating mode when a transition is made from standby mode, watch mode, or subactive mode, to active (high-speed/medium-speed) mode, with a resonator connected to the system clock oscillator.

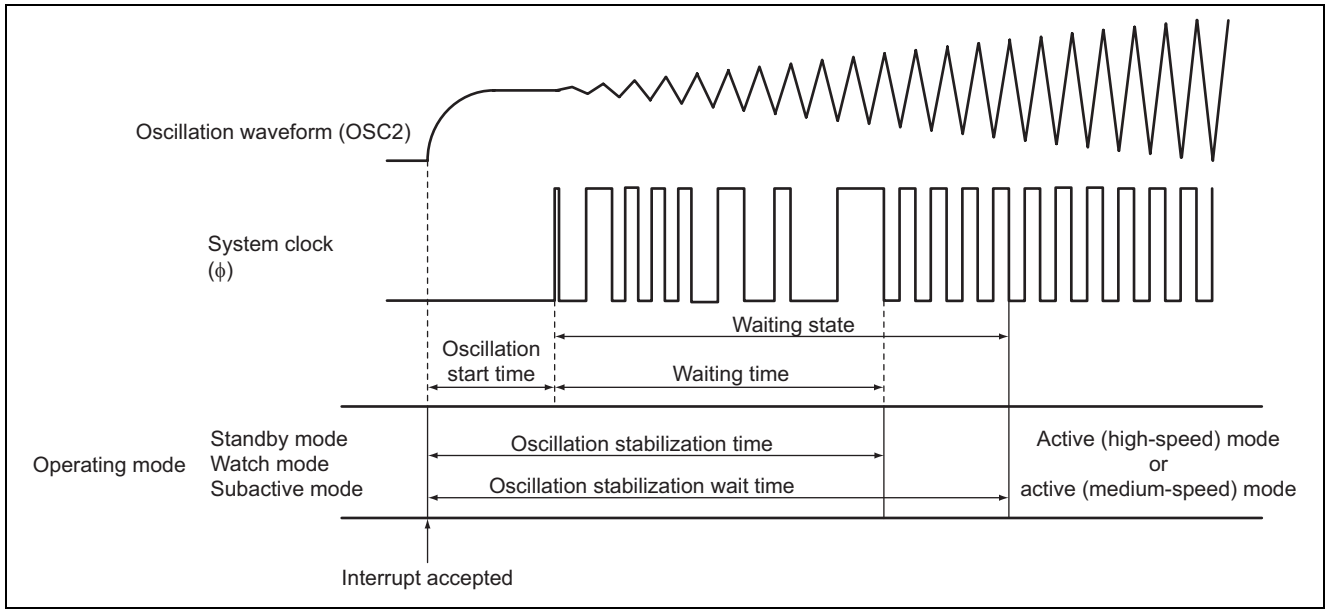


Figure 1 Oscillation Stabilization Waiting Time

As shown in figure 1, when a transition is made from a mode in which the system clock oscillator is halted to active (high-speed/medium-speed) mode, the sum of the following two times (oscillation start time and waiting time) is required.

- Oscillation Start Time
  The time from the point at which the system clock oscillator oscillation waveform starts to change when an interrupt is generated, until generation of the system clock starts.
- Waiting Time
  The time required for the CPU and peripheral functions to begin operating after generation of the oscillation waveform frequency and system clock have started, the oscillation amplitude has increased, and the oscillation frequency has stabilized.

The required oscillation stabilization time is the same as the “oscillation stabilization time (trc)” at power-on specified in the AC characteristics. Set STS2 to STS0 in SYSCR1 so that the corresponding period is greater than or equal to trc.

When a resonator is connected as the system clock oscillator, it is important to carefully evaluate the characteristics of the actual circuitry mounted on the board when a transition is made from standby mode, watch mode, or subactive mode to active (high-speed/medium-speed) mode. Set a waiting time that will allow sufficient increase in the oscillation amplitude of OSC1 and OSC2. The oscillation start time will differ with the time constant of the circuit with the resonator mounted, and the components of the constant will include stray capacitances etc.

Therefore, consult with the manufacturer of the resonator when setting the oscillation stabilization waiting time.

If the reset signal is released before the oscillation stabilization waiting time has elapsed, the microcontroller may go out of control. Make sure to release the reset after the oscillation stabilization waiting time has passed.

Also, verify that OSC oscillation reaches an amplitude of at least 1 V during the waiting time.

2.2 Need to Evaluate Matching

When a crystal or ceramic resonator is connected, the circuit’s overall time constant will differ with the stray capacitances of the resonator and on-chip circuit and so on. Ask the manufacturer of the crystal or ceramic resonator for the circuit-matching data, i.e. the characteristics data on the resonator when connected with an actual board.

2.3 Setting Numbers of CPU-Clock Cycles (States) to Wait

Table 1 is a list of products grouped with others that require the same setting for the waiting period as a number of cycles.

For all processors in a single group of the table, the various settings for bits STS2 to STS0 in system control register 1 (SYSCR1) in the same group (bits STS2 to STS0 in SYSCR1 and bit STS3 in SYSCR3 in the case of the H8/38099) select the same number of CPU cycles. Tables 2 to 6 show the periods selected by the settings of bits STS2 to STS0 bits in the system control register 1 (SYSCR1) of products in each group (bits STS2 to STS0 bits in SYSCR1 and bit STS3 in SYSCR3 in the case of H8/38099) at different frequencies.

These bits set the number of cycles to wait from the start of oscillation by the system clock oscillator to supply of the system clock. According to the operating frequency, set the waiting time so that it is longer than the time required for oscillation stabilization.

Table 1 H8/300H and H8/300L Microcontrollers Grouped by Wait State Settings

Group 1	Group 2	Group 3	Group 4	Group 5
H8/38347	H8/38024R	H8/38124	H8/38602R	H8/38099
H8/3847S	H8/38024S	H8/38104		
H8/38327	H8/38004			
H8/3827S	H8/38002S			
	H8/38076R			
	H8/38086R			

Table 2 Operating Frequency and Number of Cycles Set by the STS2 to STS0 Bits for Group 1

Bits				Waiting Time (unit: ms)	
STS2	STS1	STS0	Number of Cycles	Operating Frequency: 2 MHz	Operating Frequency: 1 MHz
0	0	0	8,192	4.1	8.2
0	0	1	16,384	8.2	16.4
0	1	0	32,768	16.4	32.8
0	1	1	65,536	32.8	65.5
1	0	0	131,072	65.5	131.1
1	0	1	2 (external clock input)	0.001	0.002
1	1	0	8	0.004	0.008
1	1	1	16	0.008	0.016

Note: When an external clock is in use, set the STS2, STS1, and STS0 bits to 1, 0, and 1, respectively. Other settings are available; however, when the setting for these bits is other than STS2 = 1, STS1 = 0, and STS0 = 1, operation may start before the waiting time ends.

Table 3 Operating Frequency and Waiting Times Set by the STS2 to STS0 Bits for Group 2

Bits				Waiting Time (unit: ms)	
STS2	STS1	STS0	Number of Cycles	Operating Frequency: 5 MHz	Operating Frequency: 2 MHz
0	0	0	8,192	1.638	4.1
0	0	1	16,384	3.277	8.2
0	1	0	1,024	0.205	0.512
0	1	1	2,048	0.410	1.024
1	0	0	4,096	0.819	2.048
1	0	1	2 (external clock input)	0.0004	0.001
1	1	0	8	0.002	0.004
1	1	1	16	0.003	0.008

Note: When an external clock is in use, set the STS2 to STS0 bits to the values for the external clock input mode before the mode transition. Also, do not make this setting when an external clock is not in use.

Table 4 Operating Frequency and Waiting Times Set by the STS2 to STS0 Bits for Group 3

Bits				Waiting Time (unit: ms)	
STS2	STS1	STS0	Number of Cycles	Operating Frequency: 5 MHz	Operating Frequency: 2 MHz
0	0	0	8,192	1.638	4.1
0	0	1	16,384	3.277	8.2
0	1	0	32,768	6.554	16.4
0	1	1	65,536	13.108	32.8
1	0	0	131,072	26.216	65.5
1	0	1	2 (external clock input)	0.0004	0.001
1	1	0	8	0.002	0.004
1	1	1	16	0.003	0.008

Note: When an external clock is in use, set the STS2 to STS0 bits to the values for the external clock input mode before the mode transition. Also, do not make this setting when an external clock is not in use.
When using the on-chip oscillator with products from the H8/38104 and H8/38124 groups, we recommend that you set the number of cycles to 8,192 (STS2 = 0, STS1 = 0, STS0 = 0)

Table 5 Operating Frequency and Waiting Times Set by the STS2 to STS0 Bits for Group 4

Bits				Waiting Time (unit: µs)				
STS2	STS1	STS0	Number of Cycles	10 MHz	8 MHz	5 MHz	4 MHz	2 MHz
0	0	0	8,192	819.2	1,024.0	1,638.4	2,048.0	4,096.0
0	0	1	16,384	1,638.4	2,048.0	3,276.8	4,096.0	8,192.0
0	1	0	1,024	102.4	128.0	204.8	256.0	512.0
0	1	1	2,048	204.8	256.0	409.6	512.0	1,024.0
1	0	0	4,096	409.6	512.0	819.2	1,024.0	2,048.0
1	0	1	256	25.6	32.0	51.2	64.0	128.0
1	1	0	512	51.2	64.0	102.4	128.0	256.0
1	1	1	16	1.6	2.0	3.2	4.0	8.0

Table 6 Operating Frequency and Waiting Times Set by the STS2 to STS0 Bits for Group 5

Bits					Waiting Time (unit: µs)				
STS3	STS2	STS1	STS0	Number of Cycles	10 MHz	8 MHz	5 MHz	4.19 MHz	2 MHz
0	0	0	0	8,192	819.2	1,024.0	1,638.4	1,953.3	4,096.0
0	0	0	1	16,384	1,638.4	2,048.0	3,276.8	3,906.5	8,192.0
0	0	1	0	1,024	102.4	128.0	204.8	244.2	512.0
0	0	1	1	2,048	204.8	256.0	409.6	488.3	1,024.0
0	1	0	0	4,096	409.6	512.0	819.2	976.6	2,048.0
0	1	0	1	2 (external clock input)	0.2	0.3	0.4	0.5	1.0
0	1	1	0	8	0.8	1.0	1.6	1.9	4.0
0	1	1	1	16	1.6	2.0	3.2	3.8	8.0
1	0	0	0	256	25.6	32.0	51.2	61.0	128.0
1	0	0	1	512	51.2	64.0	102.4	122.1	256.0
1	0	1	0	32,768	3,276.8	4,096.0	6,553.6	7,813.1	16,384.0
1	0	1	1	65,536	6,553.6	8,192.0	13,107.2	15,626.1	32,768.0
1	1	0	0	131,072	13,107.2	16,384.0	26,214.4	31,252.3	65,536.0
1	1	0	1	4	0.4	0.5	0.8	1.0	2.0
1	1	1	0	32	3.2	4.0	6.4	7.6	16.0
1	1	1	1	128	12.8	16.0	25.6	30.5	64.0

Note: When an external clock is in use, set the STS3 to STS0 bits to the values for the external clock input mode before the mode transition. Also, do not make this setting when an external clock is not in use.

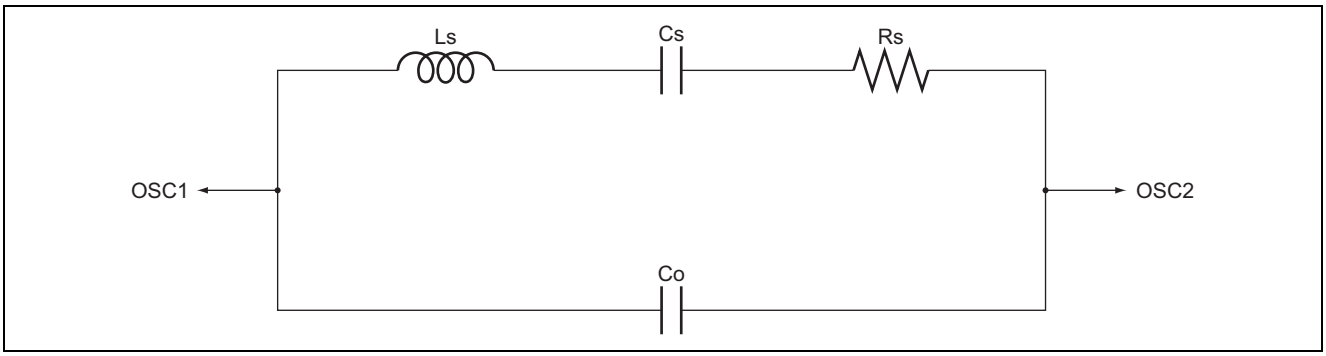
2.4 AC Characteristics (Oscillation Stabilization Time: trc)

Tables 7 to 11 show oscillation stabilization time (trc) values given in the AC characteristics for each group.

Table 7 Oscillation Stabilization Time for Group 1 (H8/3827S, H8/3847S)

Item	Symbol	Applicable Pins	Test Condition	Value			Unit	Notes
				Min.	Typ.	Max.		
Oscillation Stabilization Time	trc	OSC1 OSC2	Ceramic resonator Vcc = 2.2 V to 3.6 V	—	20	45	µs	See Reference 1.
			Ceramic resonators other than the above	—	80	—		
			Other than the above	—	—	50	ms	

Reference 1 Equivalent Circuit of Resonator (1)



- Parameters of Ceramic Resonator (Values from the Manufacturer's Specifications)

	Frequency (MHz)	Manufacturer	Format
	2		
Rs (max.)	18.3 Ω	Murata Manufacturing Co., Ltd.	CSTLS4M00G53/56
Co (max.)	36.94 pF		

Table 8 Oscillation Stabilization Time for Devices in Group 1 (H8/38327, H8/38347)

Item	Symbol	Applicable Pins	Test Condition	Value			Unit	Notes
				Min.	Typ.	Max.		
Oscillation Stabilization Time	trc	OSC1 OSC2	Ceramic resonator Vcc = 3.0 V to 5.5 V	—	20	45	µs	See Reference 2.
			Ceramic resonators other than the above	—	80	—		
			Other than ceramic resonators	—	—	50	ms	

Reference 2 Recommended Resonators (1)

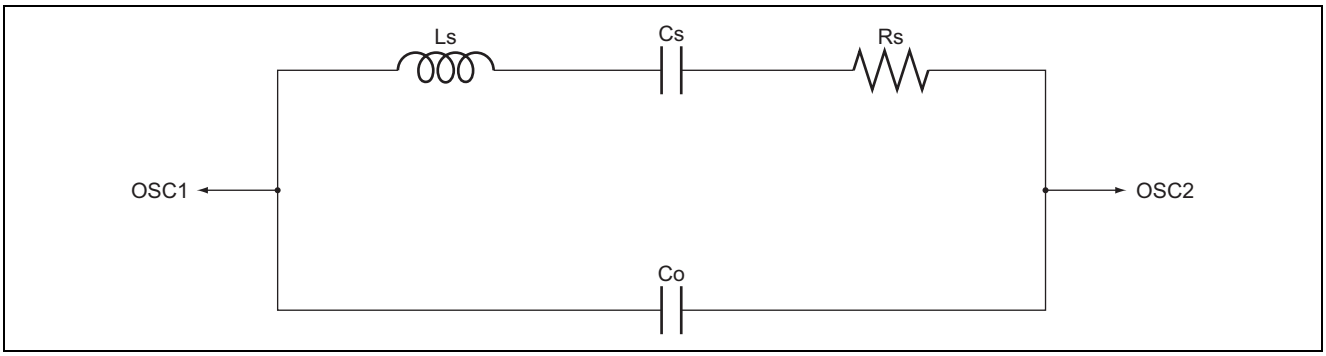
- Parameters of Ceramic Resonator (Values from the Manufacturer's Specifications)

Oscillation Frequency	Manufacturer	Format	Internal C1, C2
2 MHz	Murata Manufacturing Co., Ltd.	CSTCC2M00G53-B0	15 pF ± 20%
		CSTCC2M00G56-B0	47 pF ± 20%
4 MHz		CSTLS4M00G53-B0	15 pF ± 20%
		CSTLS4M00G56-B0	47 pF ± 20%
10 MHz		CSTLS10M0G53-B0	15 pF ± 20%
		CSTLS10M0G56-B0	47 pF ± 20%

Table 9 Oscillation Stabilization Time for Devices in Groups 2

Item	Symbol	Applicable Pins	Test Condition	Value			Unit	Notes
				Min.	Typ.	Max.		
Oscillation Stabilization Time	trc	OSC1 OSC2	Ceramic resonator Vcc = 2.2 V to 3.6 V	—	20	45	µs	See Reference 3.
			Ceramic resonators other than the above	—	80	—		
			Other than ceramic resonators	—	—	50	ms	

Reference 3 Equivalent Circuit of Resonator (2)



- Parameters of Ceramic Resonator (Value from the Manufacturer's Specifications)

	Frequency (MHz)			Manufacturer
	2	4.194	10	
Rs (max.)	18.3 Ω	68 Ω	4.6 Ω	Murata Manufacturing Co., Ltd.
Co (max.)	36.94 pF	36.72 pF	32.31 pF	

Table 10 Oscillation Stabilization Time for Devices in Groups 3

Item	Symbol	Applicable Pins	Test Condition	Value			Unit	Notes
				Min.	Typ.	Max.		
Oscillation Stabilization Time	trc	OSC1 OSC2		—	—	20	ms	See Reference 4.

Reference 4 Recommended Resonator (2)

- Parameters of Ceramic Resonator (Values from the Manufacturer's Specifications)

Oscillation Frequency	Manufacturer	Format	Internal C1, C2	Notes
2 MHz	Murata Manufacturing Co., Ltd.	CSTCC2M00G53-B0	15 pF ± 20%	
		CSTCC2M00G56-B0	47 pF ± 20%	
10 MHz		CSTLS10M0G53-B0	15 pF ± 20%	
		CSTLS10M0G56-B0	47 pF ± 20%	
16 MHz		CSTLS16M0X53-B0	15 pF ± 20%	
20 MHz		CSTLS20M0X53-B0	15 pF ± 20%	Not for use with the H8/38124.

Table 11 Oscillation Stabilization Time for Group 4 and 5

Item	Symbol	Applicable Pins	Test Condition	Value			Unit	Notes
				Min.	Typ.	Max.		
Oscillation Stabilization Time	trc	OSC1 OSC2	Ceramic resonator Vcc = 2.2 V to 3.6 V	—	20	45	µs	See Reference 5.
			Ceramic resonators other than the above	—	80	—		
			Other than ceramic resonators	—	—	50	ms	

Reference 5 Recommended Resonator (3)

- Parameters of Ceramic Resonators (Values from the Manufacturer's Specifications)

Oscillation Frequency	Manufacturer	Format	Internal C1, C2
2 MHz	Murata Manufacturing Co., Ltd.	CSTCC2M00G53-B0	15 pF ± 20%
		CSTCC2M00G56-B0	47 pF ± 20%
4.19 MHz		CSTLS4M19G53-B0	15 pF ± 20%
		CSTLS4M19G56-B0	47 pF ± 20%
10 MHz		CSTLS10M0G53-B0	15 pF ± 20%
		CSTLS10M0G56-B0	47 pF ± 20%

3. Setting Periods of Waiting to Cover Oscillation Stabilization

The following describes how to set oscillation stabilization wait time when the H8/38099 product is used with a CERALOCK™ ceramic resonator (10 MHz, CSTLS10M0G53-B0) manufactured by Murata Manufacturing Co., Ltd. The oscillation stabilization wait time is represented by the formula below.

Oscillation stabilization time
= oscillation start time + the number of cycles (“states”) of waiting > oscillation stabilization time (trc)
Oscillation stabilization time (t_{rc}): typ.: 20 µs,
max.: 45 µs (see Table 11.)

The number of cycles (“states”) of waiting is set as shown in Table 6. For example, when the STS3, STS2, STS1, and STS0 bits are set to 1, 0, 0 and 1 respectively, the number of cycles is 512, 51.2 µ.

In this case, the waiting time setting to ensure normal operation of the CPU and peripheral functions is 51.2 µs.

If the above setting leads to a malfunction in the CPU or peripheral functions, change the setting of the STS3 to STS0 bits to increase the number of cycles of waiting, and then use the product.

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