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H8/300L SLP Series

Setting Up Module-Standby Mode

Introduction

This sample task shows how to set up the module standby mode.

Target Device

H8/38024

Contents

1. Specifications

Module standby mode is the function to stop operation of modules by stopping the system clock supply to them. Module standby mode can be set up for individual peripheral functions. All the on-chip peripheral modules can be placed in module standby mode.

1.1 Setting module standby mode

Module standby mode can be set by clearing the corresponding bits in the clock stop register 1 (CKSTPR1) and clock stop register 2 (CKSTPR2) to 0.

1.2 Canceling module standby mode

Module standby mode can be canceled by setting the corresponding bits in the clock stop register 1 (CKSTPR1) and clock stop register 2 (CKSTPR2) to 1.

After a reset, CKSTPR1 and CKSTPR2 are both initialized to H'FF.

1.3 Description of CKSTPR1 and CKSTPR2 registers

Table 1.1 shows the description of CKSTPR1 and CKSTPR2 registers.

Table 1.1 CKSTPR1 and CKSTPR2 Registers

Register Name	Bit Number	Bit Name	Setting	Description
CKSTPR1	Bit 6	S31CKSTP	0	Sets SCI3-1 to module standby mode.
			1	Cancels SCI3-1 module standby mode.
	Bit 5	S32CKSTP	0	Sets SCI3-2 to module standby mode.
			1	Cancels SCI3-2 module standby mode.
	Bit 4	ADCKSTP	0	Sets A/D converter to module standby mode.
			1	Cancels A/D converter module standby mode.
	Bit 3	TGCKSTP	0	Sets timer G to module standby mode.
			1	Cancels timer G module standby mode.
	Bit 2	TFCKSTP	0	Sets timer F to module standby mode.
			1	Cancels timer F module standby mode.
	Bit 1	TCCKSTP	0	Sets timer C to module standby mode.
			1	Cancels timer C module standby mode.
	Bit 0	TACCKSTP	0	Sets timer A to module standby mode.
			1	Cancels timer A module standby mode.
CKSTPR2	Bit 4	PW2CKSTP	0	Sets PWM2 to module standby mode.
			1	Cancels PWM2 module standby mode.
	Bit 3	AECKSTP	0	Sets AEC to module standby mode.
			1	Cancels AEC module standby mode.
	Bit 2	WDCKSTP	0	Sets WDT to module standby mode.
			1	Cancels WDT module standby mode.
	Bit 1	PW1CKSTP	0	Sets PWM1 to module standby mode.
			1	Cancels PWM1 module standby mode.
	Bit 0	LDCKSTP	0	Sets LCD to module standby mode.
			1	Cancels LCD module standby mode.

1.4 Example of setting up module standby mode

1. Function

In this sample task, while in high-speed active mode, timer F and timer G are placed in module standby mode, and then a transition is made to watch mode.

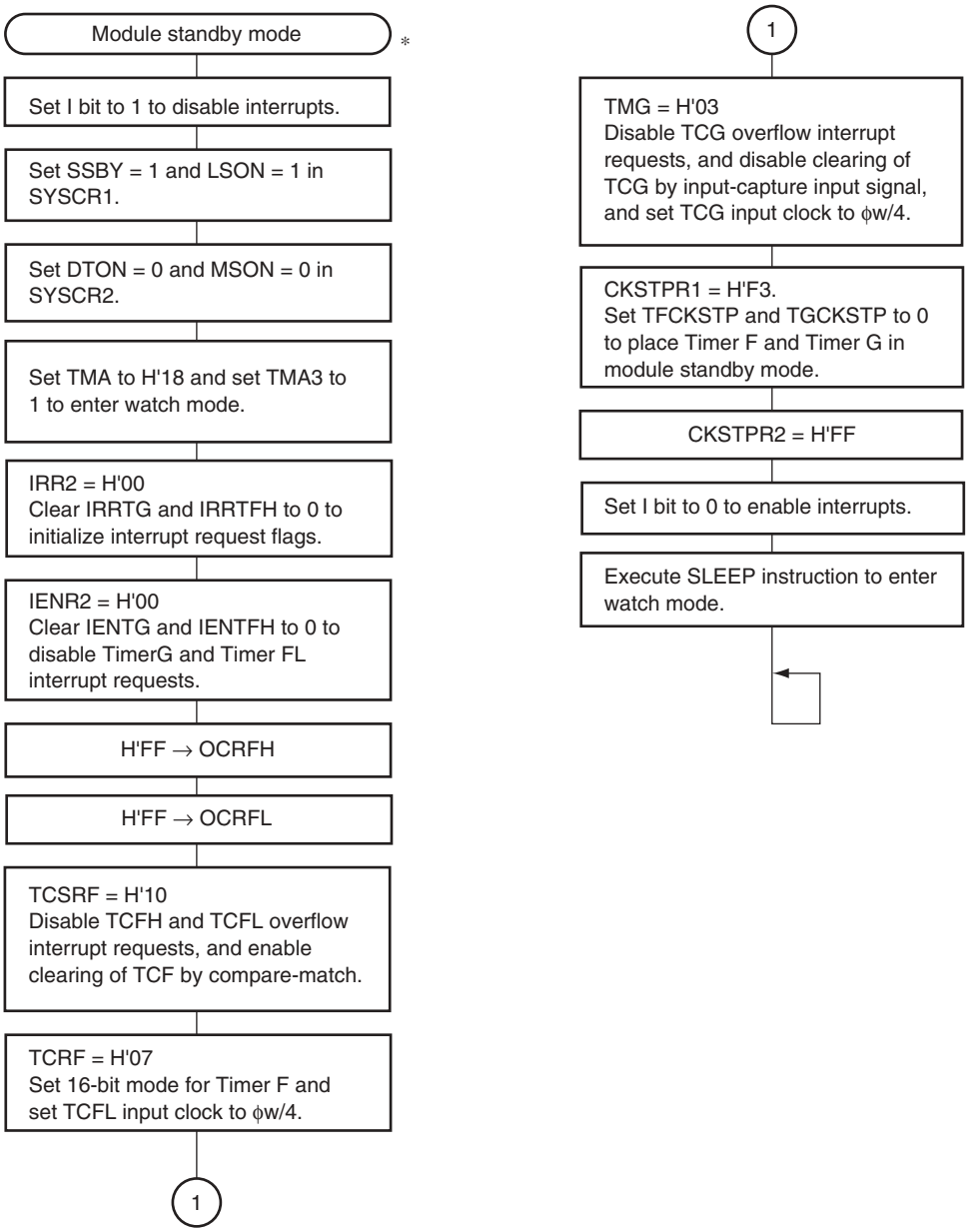
2. Notes

A. Timer F and timer G operate even in watch mode in the case when an external clock is selected as their input clock or when $\phi_w/4$ is selected as the internal clock. If any other clock is selected, operation is halted while in watch mode. Hence in this sample task, timer F and timer G is placed in module standby mode after their input clock is set to $\phi_w/4$, then transition to watch mode is made.

B. Since all interrupt requests are disabled in this sample task, once watch mode is entered, the watch mode can only be terminated by the input on the RES pin.

2. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

3. Program Listing

INIT.SRC (Program listing)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*  H8/300L Super Low Power Series                                                                                      */
/*      -H8/38024 Series-                                                                                               */
/*  Application Note                                                                                                    */
/*                                                                                                                      */
/*  'Module Standby Mode                                                                                                */
/*      -In Watch Mode, Timer F&G Module Standby Mode Set                                                               */
/*                                                                                                                      */
/*  Function                                                                                                            */
/*  : Module Standby Mode                                                                                               */
/*                                                                                                                      */
/*  External Clock : 10MHz                                                                                              */
/*  Internal Clock : 5MHz                                                                                               */
/*  Sub Clock      : 32.768kHz                                                                                          */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*  Symbol Definition                                                                                                   */
/************************************************************************************************************************/
struct BIT {
    unsigned char   b7:1;       /* bit7 */
    unsigned char   b6:1;       /* bit6 */
    unsigned char   b5:1;       /* bit5 */
    unsigned char   b4:1;       /* bit4 */
    unsigned char   b3:1;       /* bit3 */
    unsigned char   b2:1;       /* bit2 */
    unsigned char   b1:1;       /* bit1 */
    unsigned char   b0:1;       /* bit0 */
};

#define     TMA         *(volatile unsigned char *)0xFFB0       /* Timer Mode Register A                   */
#define     TCA         *(volatile unsigned char *)0xFFB1       /* Timer Counter A                         */
#define     TCRF        *(volatile unsigned char *)0xFFB6       /* Timer Control Register F                */
#define     TCRF_BIT    (*(struct BIT *)0xFFB6)                 /* Timer Control Register F                */
#define     TOLH        TCRF_BIT.b7                             /* Toggle Output Level F                   */
#define     CKSH2       TCRF_BIT.b6                             /* Clock Select H2                         */
#define     CKSH1       TCRF_BIT.b5                             /* Clock Select H1                         */
#define     CKSH0       TCRF_BIT.b4                             /* Clock Select H0                         */
#define     TCSRF       *(volatile unsigned char *)0xFFB7       /* Timer Control Status Register F         */
#define     TCSRF_BIT   (*(struct BIT *)0xFFB7)                 /* Timer Control Status Register F         */
```

```
#define     OVFH        TCSRF_BIT.b7                        /* Timer Overflow Flag H                    */
#define     CMFH        TCSRF_BIT.b6                        /* Compare Match Flag H                     */
#define     OVIEH       TCSRF_BIT.b5                        /* Timer Overflow Interrupt Enable          */
#define     CCLRH       TCSRF_BIT.b4                        /* Output Select 3                          */
#define     OCRFH       *(volatile unsigned char *)0xFFBA   /* Output Compare Register FH               */
#define     OCRFL       *(volatile unsigned char *)0xFFBB   /* Output Compare Register FH               */
#define     TMG         *(volatile unsigned char *)0xFFBC   /* Output Compare Register FH               */
#define     SYSCR1      *(volatile unsigned char *)0xFFF0   /* System Control Register 1                */
#define     SYSCR1_BIT  (*(struct BIT *)0xFFF0)             /* System Control Register 1                */
#define     SSBY        SYSCR1_BIT.b7                       /* Software Standby                         */
#define     STS2        SYSCR1_BIT.b6                       /* Standby Timer Select 2                   */
#define     STS1        SYSCR1_BIT.b5                       /* Standby Timer Select 1                   */
#define     STS0        SYSCR1_BIT.b4                       /* Standby Timer Select 0                   */
#define     LSON        SYSCR1_BIT.b3                       /* Low Speed On Flag                        */
#define     MA1         SYSCR1_BIT.b1                       /* Active Mode Clock Select 1               */
#define     MA0         SYSCR1_BIT.b0                       /* Active Mode Clock Select 0               */
#define     SYSCR2      *(volatile unsigned char *)0xFFF1   /* System Control Register 2                */
#define     SYSCR2_BIT  (*(struct BIT *)0xFFF1)             /* System Control Register 2                */
#define     NESEL       SYSCR2_BIT.b4                       /* Noise Elimination Sampling               */
                                                            /*                          Frequency Select */
#define     DTON        SYSCR2_BIT.b3                       /* Direct Transfer On Flag                  */
#define     MSON        SYSCR2_BIT.b2                       /* Middle Speed On Flag                     */
#define     SA1         SYSCR2_BIT.b1                       /* Subactive Mode Clock Select 1            */
#define     SA0         SYSCR2_BIT.b0                       /* Subactive Mode Clock Select 0            */
#define     IENR2       *(volatile unsigned char *)0xFFF4   /* Interrupt Enable Register 2              */
#define     IENR2_BIT   (*(struct BIT *)0xFFF4)             /* Interrupt Enable Register 2              */
#define     IENTFH      IENR2_BIT.b3                        /* Timer FH Interrupt Enable                */
#define     IENTG       IENR2_BIT.b4                        /* Timer FH Interrupt Enable                */
#define     IRR2        *(volatile unsigned char *)0xFFF7   /* Interrupt Request Register 2             */
#define     IRR2_BIT    (*(struct BIT *)0xFFF7)             /* Interrupt Request Register 2             */
#define     IRRTFH      IRR2_BIT.b3                         /* Timer FH Interrupt Request Flag          */
#define     IRRTG       IRR2_BIT.b4                         /* Timer FH Interrupt Request Flag          */
#define     CKSTPR1     *(volatile unsigned char *)0xFFFA   /*                                          */
#define     CKSTPR2     *(volatile unsigned char *)0xFFFB   /*                                          */

/************************************************************************************************************/
/*  Function define                                                                                         */
/************************************************************************************************************/
extern void INIT ( void );                                  /* SP Set                                   */
void        main ( void );

/************************************************************************************************************/
/*  Vector Address                                                                                          */
/************************************************************************************************************/
#pragma section     V1                                      /* Vector Section Set                       */
void (*const VEC_TBL1[])(void) = {
    INIT                                                    /* 0x0000 Reset Vector                      */
};

#pragma section                                             /* P                                        */
```

```
/*****************************************************************************************************************/
/*  Main Program                                                                                                 */
/*****************************************************************************************************************/
void    main ( void )
{
    set_imask_ccr(1);                                   /* Interrupt Disable                    */

    SYSCR1 = 0x8F;                                      /* Set SYSCR1                           */
    SYSCR2 = 0xF0;                                      /* Set SYSCR2                           */

    TMA = 0x18;                                         /* Initialize TCA Overflow Period       */

    IRR2 = 0;                                           /* Clear IRRTA                          */
    IENR2 = 0;                                          /* Timer A Interrupt Enable             */

    OCRFH = 0xFF;                                       /* Initialize Compare Match FH Value    */
    OCRFL = 0xFF;                                       /* Initialize Compare Match FL Value    */
    TCSRF = 0x10;                                       /* Initialize Overflow Interrupt        */
    TCRF = 0x07;                                        /* TMOFH High level Output              */

    TMG = 0x03;                                         /* Timer G                              */

    CKSTPR1 = 0xF3;
    CKSTPR2 = 0xFF;

    set_imask_ccr(0);                                   /* Interrupt Enable                     */

    sleep();                                            /* Transition to Sleep Mode             */

    while(1){
        ;
    }
}
```

Link address specifications

Section Name	Address
CV1	H'0000
P	H'0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

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