To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

H8/300L Series

Serial Data Reception in Synchronous Mode (H8/3644)

Introduction

Four bytes of 8-bit data is received using the serial data transfer function in synchronous mode. Data is received LSB first.

Target Device

H8/3644

Contents

1. Specifications

1. As shown in figure 1.1, four bytes of 8-bit data are received using the serial data transfer function in synchronous mode.
2. An external clock is used as the transfer clock.
3. The data length of receive data is eight bits and data is received LSB first, which means the lowest bit of data is received first.

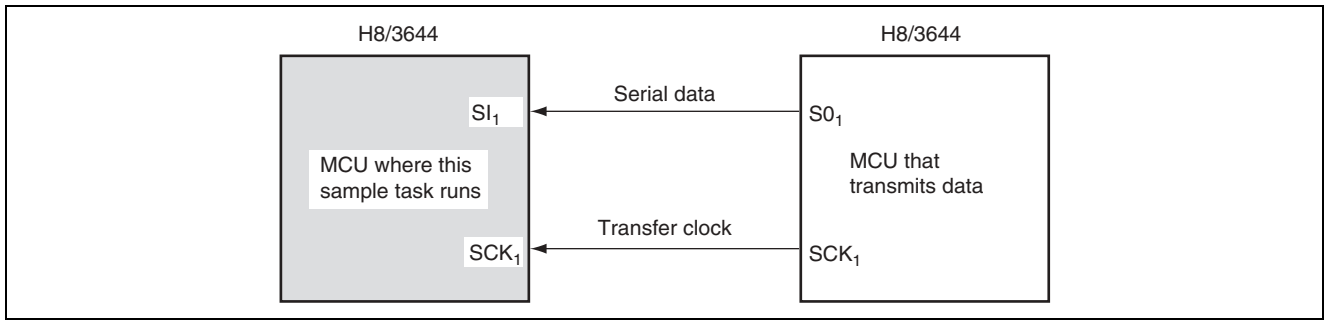


Figure 1.1 Serial Data Reception in Synchronous Mode

2. Description of Functions

1. In this sample task, serial data is received in synchronous mode via the serial communication interface (SCI). Figure 2.1 shows a block diagram of serial data reception in synchronous mode, and the following is the description for the block diagram:
   - The serial control register 1 (SCR1) is an 8-bit readable/writable register that selects operating mode, transfer clock source, and prescaler division ratio.
   - The serial control/status register 1 (SCSR1) is an 8-bit register that indicates operation status, error status, etc. If the synchronous clock is input continuously after the reception completion, reception is not performed but ORER in SCSR1 is set to 1 to indicate an overrun state.
   - The serial data register U (SDRU) is an 8-bit readable/writable register that functions as a data register for the upper 8 bits in 16-bit data transfer. Data written to SDRU is output to SDRL with the LSB first. Then, data is in turn input from the SI_1 pin with the LSB first, and data is shifted from the MSB to the LSB.
   - The serial data register L (SDRL) is an 8-bit readable/writable register that functions as a data register in 8-bit data transfer and as a data register for the lower 8 bits in 16-bit data transfer. In 8-bit data transfer, data written to SDRL is output from the SO_1 pin with the LSB first. Then, data is in turn input from the SI_1 pin with the LSB first, and data is shifted from the MSB to the LSB. In 16-bit data transfer, operation is the same as that in 8-bit data transfer except that data is input from SDRU.
   - SDRU and SDRL should be read or written to after data transmission or reception is complete. If they are read or written to during data transmission or reception, data may not be guaranteed.
   - The transfer clock can be selected from eight internal clocks and external clocks. When an internal clock is selected, the SCK_1 pin is used as an output pin. The selected clock is continuously output from the SCK_1 pin if clock continuous output mode is set. When an external clock is selected, the SCK_1 pin is used as the clock input pin.
   - In this sample task, an external clock is set as the transfer clock.
   - The SCI1 transfer data format can be selected from 8 bits and 12 bits. Data is transferred in the LSB first method that transmits or receives data from the lowest bit. Transmit data is output from the falling edge of the transfer clock to the next rising edge. Receive data is acquired on the rising edge of the transfer clock.
   - In this sample task, the 8-bit operating mode is set to perform 8-bit data reception.
   - The SCI1 clock pin (SCK_1) functions as a clock input/output pin for the SCI1.
   - The SCI1 data input pin (SI_1) functions as a receive data input pin for the SCI1.

— When SCI1 completes data transfer, the SCI1 interrupt request flag bit (IRRS1) in the interrupt request register 2 (IRR2) is set to 1. SCI1 interrupt requests can be enabled/disabled with the SCI1 interrupt enable bit (IENS1) in the interrupt enable register 2 (IENR2).

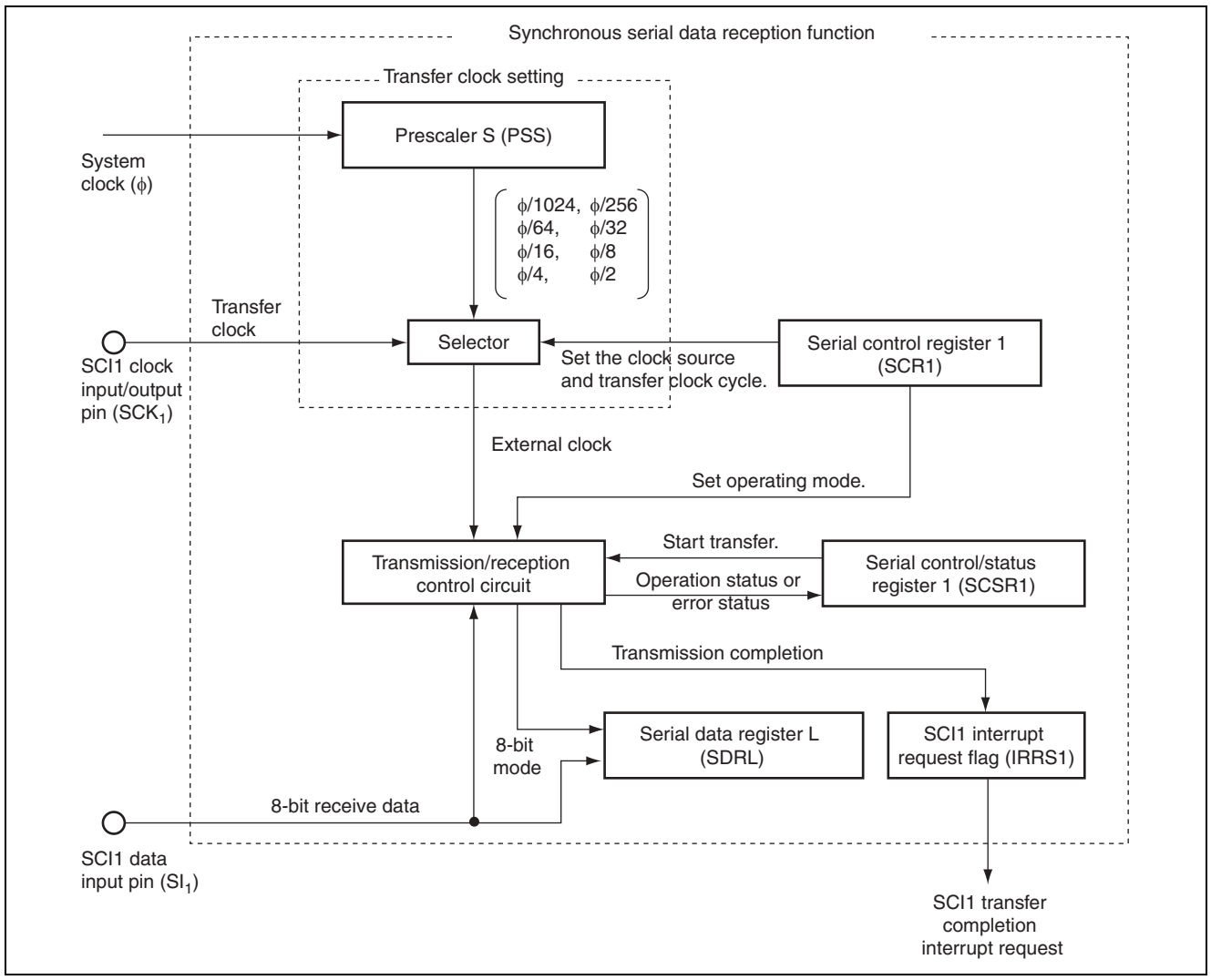


Figure 2.1 Block Diagram of Synchronous Serial Data Reception Function

2. Table 2.1 shows the allocation of functions used in this sample task. Functions are allocated as shown in table 1 to perform serial data reception in synchronous mode.

Table 2.1 Function Allocation

Function	Function Allocation
SCR1	Operating mode, transfer clock source and prescaler division ratio are set.
SCSR1	Operation status or error status is indicated.
SDRL	Data register for 8-bit receive data
SCK_1	Transfer clock input pin of SCI1
SI_1	Receive data output pin of SCI1
IRRS1	SCI1 transfer completion is indicated.
IENS1	Enabling/disabling of SCI1 interrupt requests is controlled.
PMR3	$P3_2/SO_1$ and $P3_0/SCK_1$ pin functions are set.

3. Principle of Operation

1. Figure 3.1 shows the principle of operation. Serial data reception is performed in synchronous mode with the hardware and software processing shown in the figure.

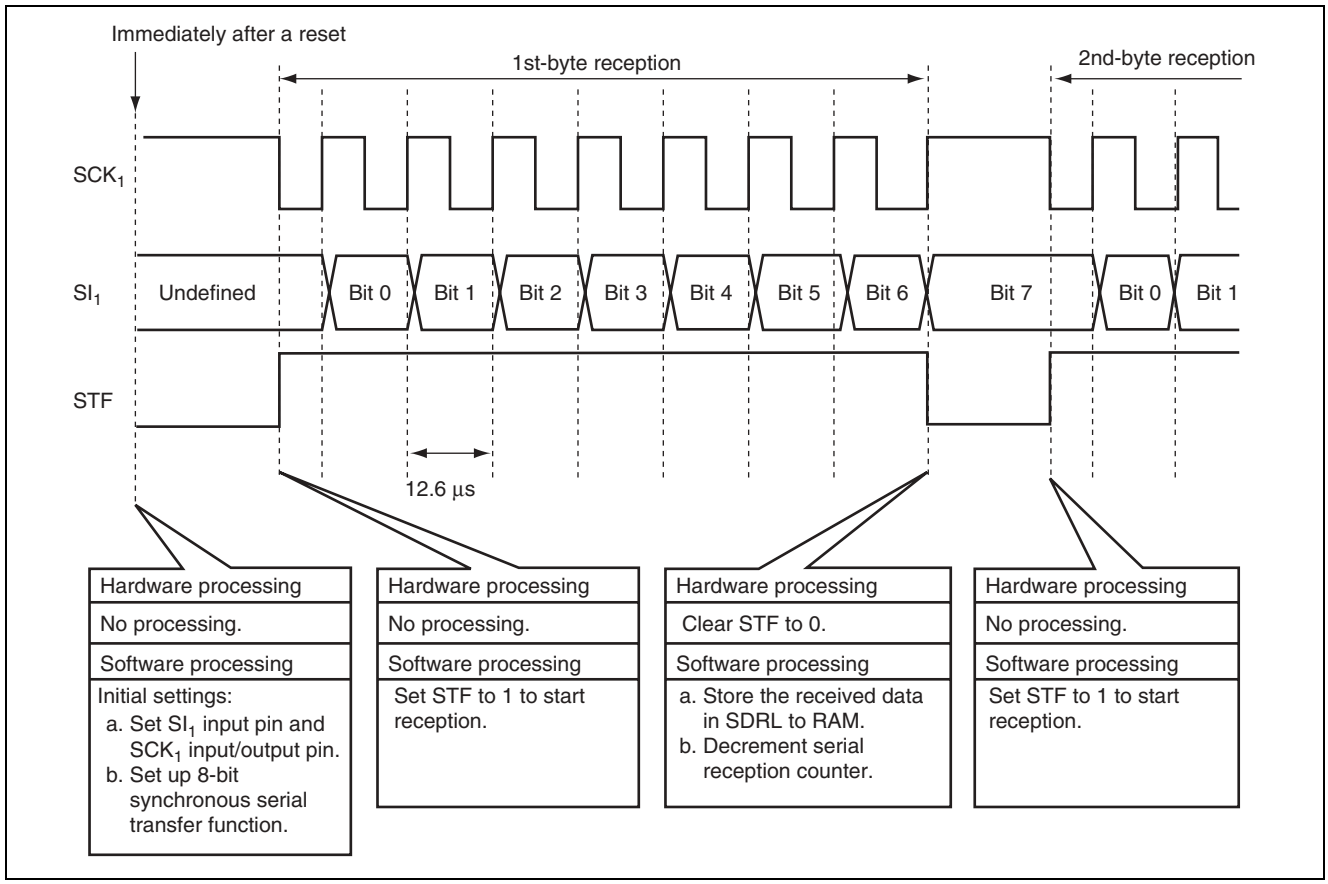


Figure 3.1 Operation Principle of Serial Data Reception in Synchronous Mode

4. Description of Software

4.1 Module

Table 4.1 describes the module used in this sample task.

Table 4.1 Description of Module

Module	Label	Function
Main routine	main	Initializes the stack pointer, sets transfer data, sets for synchronous serial data reception, enables interrupts, stores receive data to RAM, and ends when 4 bytes of data have been received.

4.2 Arguments

Table 4.2 describes the arguments used in this sample task.

Table 4.2 Description of Arguments

Argument	Function	Used in	Data Length	Input/ Output
SRD0 to SRD3	Data received in synchronous mode	Main routine	1 byte	Output

4.3 Internal Registers

The internal registers used in this sample task are described in table 4.3.

Table 4.3 Description of Internal Registers

Register		Function	Address	Setting
SCR1	SNC1 SNC0	Serial Control Register 1 (Operating Mode Select 1, 0) When SNC1 = 0 and SNC0 = 0, operating mode is set to 8-bit mode.	H'FFA0 Bit 7 Bit 6	SNC1 = 0 SNC0 = 0
	MRKON	Serial Control Register 1 (Tail Mark Control) When MRKON = 0, a tail mark is not output.	H'FFA0 Bit 5	0
	CKS3	Serial Control Register 1 (Clock Source Select 3) When CKS3 = 1, an external clock is selected as the clock source.	H'FFA0 Bit 3	1
SCSR1	ORER	Serial Control/Status Register 1 (Overrun Error Flag) When ORER = 0, indicates that no overrun error occurred. When ORER = 1, indicates that an overrun error occurred.	H'FFA1 Bit 5	0
	STF	Serial Control/Status Register 1 (Start Flag) When STF = 0, transfer operation is complete. When SOL = 1, transfer operation starts.	H'FFA1 Bit 0	0
SDRL		Serial Data Register L Stores 8-bit receive data during 8-bit transfer	H'FFA3	—

Register		Function	Address	Setting
IENR2	IENS1	Interrupt Enable Register 2 (SCI1 Interrupt Enable) When IENS1 = 0, SCI1 interrupt requests are disabled. When IENS1 = 1, SCI1 interrupt requests are enabled.	H'FFF5 Bit 4	0
IRR2	IRRS1	Interrupt Request Register 2 (SCI1 Interrupt Request Flag) When IRRS1 = 0, SCI1 interrupt requests are not requested. When IRRS1 = 1, SCI1 interrupt requests are requested.	H'FFF8 Bit 4	0
PMR3	SI1	Port Mode Register 3 ($P3_1$/SI_1 Pin Function Switch) When SI1 = 1, this pin functions as SI_1 output pin.	H'FFFD Bit 1	1
	SCK1	Port Mode Register 3 ($P3_0$/SCK_1 Pin Function Switch) When SCK1 = 1, this pin functions as SCK_1 input/output pin.	H'FFFD Bit 0	1

4.4 Description of RAM

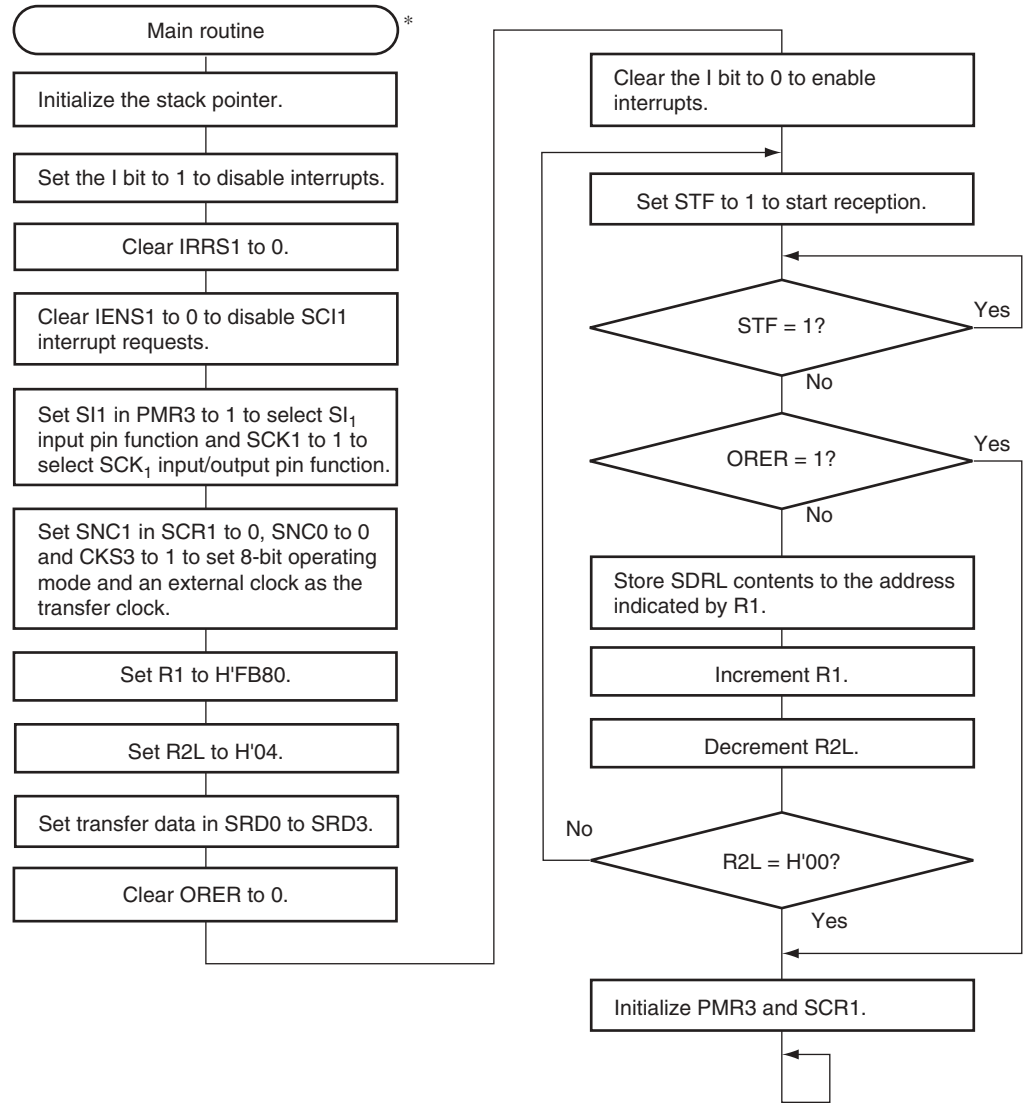
Table 4.4 describes the RAM used in this sample task.

Table 4.4 Description of RAM

Label	Function	Address	Used in
SRD0	Stores the first byte of received data.	H'FB80	Main routine
SRD1	Stores the second byte of received data.	H'FB81	Main routine
SRD2	Stores the third byte of received data.	H'FB82	Main routine
SRD3	Stores the fourth byte of received data.	H'FB83	Main routine

5. Flowchart

1. Main routine



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly language).

6. Program Listing

```
;*****************************************************************************
;*                                                                           *
;*     H8/300L Series -H8/3644,H8/3657-                                      *
;*     Application Note                                                      *
;*                                                                           *
;*     'Synchronous Serial Data Reception'                                   *
;*                                                                           *
;*     Function                                                              *
;*     : Serial Communication Interface                                      *
;*       Synchronous Serial Interface                                        *
;*       -Receiving                                                          *
;*                                                                           *
;*     External Clock : 10MHz                                                *
;*     Internal Clock :  5MHz                                                *
;*     Sub Clock      : 32.768kHz                                            *
;*                                                                           *
;*****************************************************************************
;
          .cpu         300L
;
;*****************************************************************************
;*  Symbol Defnition                                                         *
;*****************************************************************************
;
SCR1      .equ         H'FFA0        ;Serial Control Register 1
SNC1      .bequ        7,SCR1        ;Select the Operation Mode 1
SNC0      .bequ        6,SCR1        ;Select the Operation Mode 0
MRKON     .bequ        5,SCR1        ;TAIL MARK Control
LTCH      .bequ        4,SCR1        ;LATCH TAIL Select
CKS3      .bequ        3,SCR1        ;Clock Source Select 3
CKS2      .bequ        2,SCR1        ;Clock Select 2
CKS1      .bequ        1,SCR1        ;Clock Select 1
CKS0      .bequ        0,SCR1        ;Clock Select 0
SCSR1     .equ         H'FFA1        ;Serial Control Status Register 1
SOL       .bequ        6,SCSR1       ;Extended Data Bit
ORER      .bequ        5,SCSR1       ;Overrun Error Flag
MTRF      .bequ        1,SCSR1       ;TAIL MARK Transmit Flag
STF       .bequ        0,SCSR1       ;Start Flag
SDRU      .equ         H'FFA2        ;Serial Data Register U
SDRL      .equ         H'FFA3        ;Serial Data Register L
IENR2     .equ         H'FFF5        ;Interrupt Enable Register 2
IENS1     .bequ        4,IENR2       ;SCI1 Interrupt Enable
IRR2      .equ         H'FFF8        ;Interrupt Request Register 2
IRRS1     .bequ        4,IRR2        ;SCI1 Interrupt Request Flag
PMR3      .equ         H'FFFD        ;Port Mode Register 3
SO1       .bequ        2,PMR3        ;P32/SO1 Pin Function Switch
SI1       .bequ        1,PMR3        ;P31/SI1 Pin Function Switch
SCK1      .bequ        0,PMR3        ;P30/SCK1 Pin Function Switch
;
```

```
;*****************************************************************************
;*  RAM Allocation                                                           *
;*****************************************************************************
;
STACK     .equ          H'FF80        ;Stack Pointer
SRD0      .equ          H'FB80        ;Serial Receiving Data 0
SRD1      .equ          H'FB81        ;Serial Receiving Data 1
SRD2      .equ          H'FB82        ;Serial Receiving Data 2
SRD3      .equ          H'FB83        ;Serial Receiving Data 3
;
;*****************************************************************************
;*  Vector Address                                                           *
;*****************************************************************************
;
          .org          H'0000
          .data.w       MAIN          ;Reset Interrupt
;
          .org          H'0008
          .data.w       MAIN          ;IRQ0 Interrupt
          .data.w       MAIN          ;IRQ1 Interrupt
          .data.w       MAIN          ;IRQ2 Interrupt
          .data.w       MAIN          ;IRQ3 Interrupt
          .data.w       MAIN          ;INT0 - INT7 Interrupt
;
          .org          H'0014
          .data.w       MAIN          ;Timer A Interrupt
          .data.w       MAIN          ;Timer B1 Interrupt
;
          .org          H'0020
          .data.w       MAIN          ;Timer X Interrupt
          .data.w       MAIN          ;Timer V Interrupt
;
          .org          H'0026
          .data.w       MAIN          ;SCI1 Interrupt
;
          .org          H'002A
          .data.w       MAIN          ;SCI3 Interrupt
          .data.w       MAIN          ;A/D Converter Interrupt
          .data.w       MAIN          ;SLEEP Instruction Executed Interrupt
;
;*****************************************************************************
;*  Main Program                                                             *
;*****************************************************************************
;
          .org          H'1000
;
MAIN      .equ          $
          MOV.W         #STACK,SP     ;Initialize Stack Pointer
          ORC           #H'80,CCR     ;Interrupt Disable
;
          BCLR          IRRS1         ;Clear IRRS1
          BCLR          IENS1         ;SCI1 Interrupt Disable
;
          MOV.W         #H'0308,R0
          MOV.B         R0H,@PMR3     ;Initialize SI1 & CKS1 Pin Function
          MOV.B         R0L,@SCR1     ;Initialize Synchronous Serial Transfer Function
;
          MOV.W         #H'FB80,R1    ;Initialize Serial Receiving Data Address
          MOV.B         #H'04,R2L     ;Initialize Serial Receiving Data Counter
```

```
;
          MOV.B         #H'00,R0L
          MOV.B         R0L,@SRD0      ;Initialize Serial Receiving Data 0
          MOV.B         R0L,@SRD1      ;Initialize Serial Receiving Data 1
          MOV.B         R0L,@SRD2      ;Initialize Serial Receiving Data 2
          MOV.B         R0L,@SRD3      ;Initialize Serial Receiving Data 3
;
          BTST          ORER
          BCLR          ORER           ;Clear ORER
;
          ANDC          #H'7F,CCR      ;Interrupt Enable
;
MAIN1     .equ          $
          BSET          STF            ;Start Serial Receiving
;
MAIN2     .equ          $
          BTST          STF            ;End Serial Receiving ?
          BNE           MAIN2          ;No.
;
          BTST          ORER           ;Overrun Error Flag = 1 ?
          BNE           MAIN3          ;Yes.
;
          MOV.B         @SDRL,R0L      ;Load
          MOV.B         R0L,@R1        ;Save
;
          ADDS          #1,R1          ;Increment Serial Receiving Data Address
          DEC           R2L            ;Decrement Serial Receiving Data Counter
          BNE           MAIN1          ;Serial Receiving Data Counter = H'00 ? No.
;
          MOV.B         #H'00,R0L
          MOV.B         R0L,@PMR3      ;Initialize SI1 & SCK1 Pin Function
          MOV.B         R0L,@SCR1      ;Initialize Synchronous Serial Transfer Function
          BRA           MAIN9
;
MAIN3    .equ           $
          MOV.B         #H'FF,R0L
          MOV.B         R0L,@SRD0      ;Overrun Error
          MOV.B         R0L,@SRD1      ;Overrun Error
          MOV.B         R0L,@SRD2      ;Overrun Error
          MOV.B         R0L,@SRD3      ;Overrun Error
;
          MOV.B         R0L,@PMR3      ;Initialize SI1 & SCK1 Pin Function
          MOV.B         R0L,@SCR1      ;Initialize Synchronous Serial Transfer Function
;
MAIN9     .equ          $
          BRA           MAIN9
;
          .end
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Dec.19.03	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.