

RZ/G Series

Getting Started with Flexible Software Package

Introduction

This application note describes how to use the Renesas Flexible Software Package (FSP) for writing applications for the RZ/G microprocessor series.

Target Device

RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/G3S, RZ/G3E, RZ/G3L

Contents

1. Introduction.....	4
1.1 Overview.....	4
1.2 Introduction to FSP.....	4
1.2.1 Purpose	4
1.2.2 e ² studio IDE.....	4
1.3 Limitations	4
1.3.1 Peripherals and Pins Assignment	4
1.3.2 RAM Initialization.....	4
2. Starting Development Introduction.....	5
2.1 e ² studio Setup	5
2.1.1 What is e ² studio?.....	5
2.1.2 e ² studio Prerequisites.....	5
2.1.3 e ² studio Installation for Windows PC	5
2.1.4 e ² studio Installation for Linux PC.....	12
2.2 FSP Setup	19
2.2.1 Installation of FSP using Package Installer.....	19
2.2.2 Installation of FSP Packs using Package Zip file	21
3. Set up an SMARC EVK	23
3.1 RZ/G2L SMARC EVK.....	23
3.1.1 Supported Debugger	23
3.1.2 Board Setup.....	23
3.2 RZ/G3S SMARC EVK	27
3.2.1 Supported Debugger	27
3.2.2 Board Setup.....	27
3.3 RZ/G3E SMARC EVK	33
3.3.1 Supported Debugger	33
3.3.2 Board Setup.....	33
3.4 RZ/G3L SMARC EVK.....	38
3.4.1 Supported Debugger	38
3.4.2 Board Setup.....	38
4. Tutorial: Your First RZ MPU Project - Blinky	43
4.1 Tutorial Blinky	43
4.2 What Does Blinky Do?	43
4.3 Create a New Project for Blinky	45
4.3.1 Details about the Blinky Configuration	50
4.3.2 Configuring the Blinky Clocks.....	50
4.3.3 Configuring the Blinky Pins	50
4.3.4 Configuring the Parameters for Blinky Components	50

4.3.5	Where is main()?	50
4.3.6	Blinky Example Code	50
4.4	Build the Blinky Project	51
4.5	Debug the Blinky Project	52
4.5.1	Debug prerequisites	52
4.5.2	Debug Steps	52
4.5.3	Details about the Debug Process	58
4.5.4	Run the Blinky Project	58
5.	FSP Application Launch with e ² studio	59
5.1	Creating a Project	59
5.1.1	What is a Project?	59
5.1.2	Creating a New Project	61
5.1.3	Duplication of Resources	66
5.2	Configuring a Project	66
5.2.1	Summary Tab	67
5.2.2	Configuring the BSP	67
5.2.3	Configuring Clocks	68
5.2.4	Configuring Pins	69
5.2.5	Configuring Interrupts from the Stacks Tab	70
5.2.6	Creating Interrupts from the Interrupts Tab	70
5.2.7	Viewing Event Links	70
5.2.8	Adding and Configuring HAL Drivers	71
5.3	Reviewing and Adding Components	73
5.4	Debugging the Project	74
5.5	Modifying Toolchain Settings	76
5.6	Importing an Existing Project into e ² studio	77
	Revision History	80

1. Introduction

1.1 Overview

This application note describes how to use the Renesas Flexible Software Package (FSP) running on the Cortex®-M33 (hereinafter referred to as CM33) incorporated on RZ/G Series.

1.2 Introduction to FSP

1.2.1 Purpose

The Renesas Flexible Software Package (FSP) is an optimized software package designed to provide easy-to-use, scalable, high-quality software for embedded system design. The primary goal is to provide lightweight, efficient drivers that meet common use cases in embedded systems.

1.2.2 e² studio IDE

FSP provides a host of efficiency-enhancing tools for developing projects targeting the Renesas RZ series of MPU devices. The e² studio IDE provides a familiar development cockpit that manages the key steps of project creation, module selection and configuration, code development, code generation, and debugging.

1.3 Limitations

1.3.1 Peripherals and Pins Assignment

RZ/G Series has a multi-core configuration of Cortex®-A55 (hereinafter referred to as CA55) and CM33. It is possible to use each peripheral and GPIO from each core. This package provides drivers for the peripheral for CM33, but each driver can operate on the assumption that it is not used in CA55.

1.3.2 RAM Initialization

Initialization of DDR SDRAM is always carried out in the CA55 bootstrap regardless of the selection of the boot CPU; meanwhile, internal SRAM is initialized in the bootstrap of the boot CPU.

2. Starting Development Introduction

2.1 e² studio Setup

2.1.1 What is e² studio?

Renesas e² studio is a development tool encompassing code development, build, and debug. e² studio is based on the open-source Eclipse IDE and the associated C/C++ Development Tooling (CDT).

When developing the software for RZ MPUs, e² studio hosts the Renesas Flexible Software Package (FSP). FSP provides a wide range of time-saving tools to simplify the selection, configuration, and management of modules and threads, to easily implement complex applications.

2.1.2 e² studio Prerequisites

2.1.2.1 Obtaining an RZ MPU Kit

To develop applications with RZ FSP, start with each Evaluation Board Kit. The start-up guide of each Evaluation Board Kit is available on the page below.

- RZ/G2L
[RZ/G2L Evaluation Board Kit Quick Start Guide](#)
- RZ/G2LC and RZ/G2UL
[SMARC EVK of RZ/G2L, RZ/G2LC, RZ/G2UL Linux Start-up Guide](#)
- RZ/G3S
[RZ/G3S Evaluation Board Kit Quick Start Guide](#)
- RZ/G3E
[RZ/G3E Evaluation Board Kit Quick Start Guide](#)
- RZ/G3L
[RZ/G3L Evaluation Board Kit Quick Start Guide](#)

2.1.2.2 PC Requirements

The following are the minimum PC requirements to use e² studio:

- Windows 11 or Ubuntu 20.04 LTS Desktop(64-bit) with Intel i5 or i7, or AMD A10-7850K or FX
- Memory: 8-GB DDR3 or DDR4 DRAM (16-GB DDR4/2400-MHz RAM is preferred)
- Minimum 250 GB hard disk

2.1.2.3 Licensing

FSP licensing includes full source code, limited to Renesas hardware only.

2.1.3 e² studio Installation for Windows PC

This chapter describes how to install the e² studio IDE on a Windows PC.

2.1.3.1 Download

The latest e² studio IDE installer package can be downloaded from the Renesas website for free. Please check the detailed information from: https://www.renesas.com/e2_studio. Note that users have to login to the Renesas account (on the [MyRenesas page](#)) for the software to download.

2.1.3.2 Installation of e² studio IDE

1. Invoke Installer

Double-click on the e² studio installer to invoke the e² studio installation wizard page. First, you need to select the Install Type. In this material, it is expected that Custom Install will be selected.

Then, click the **[Next >]** button to continue.

Note: If e² studio was installed on your PC, the option to modify, remove the existing version, or install the e² studio to a different location will be displayed

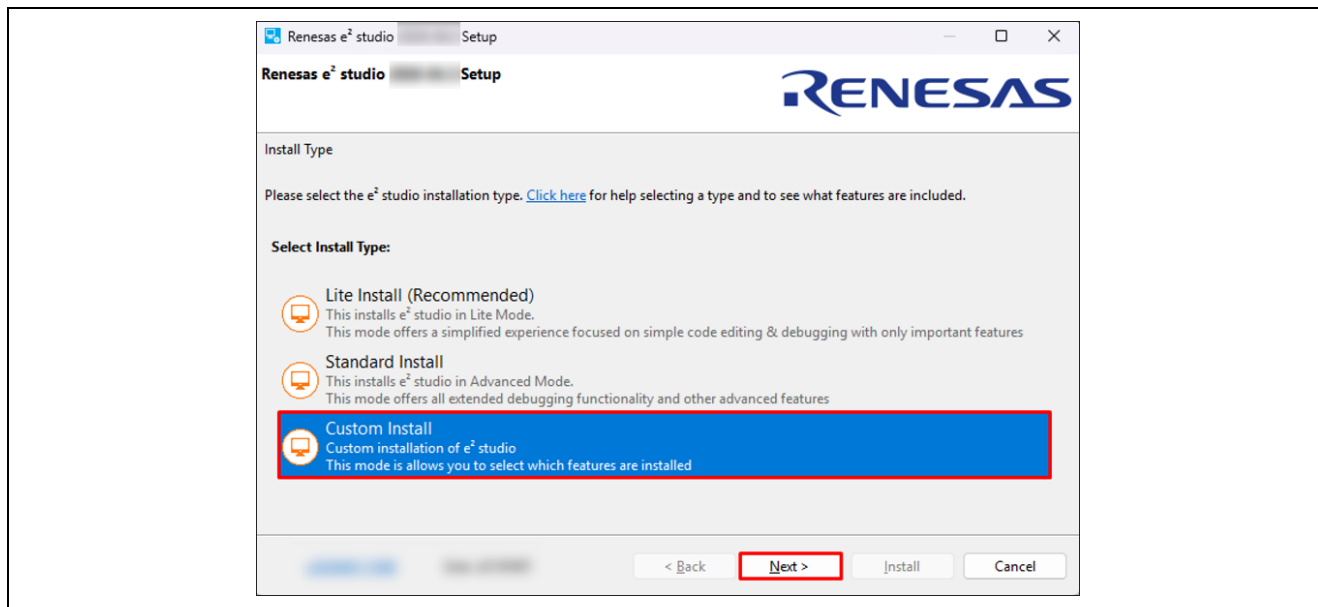


Figure 1. Installation of e² studio – Install Type

2. Welcome page

Users can change the installation folder by clicking the **[Change...]** button. Click the **[Next >]** button to continue.

Notes:

1. If you would like to have multiple versions of e² studio, please specify the new folder here.
2. Multi-byte characters cannot be used for the e² studio installation folder name.

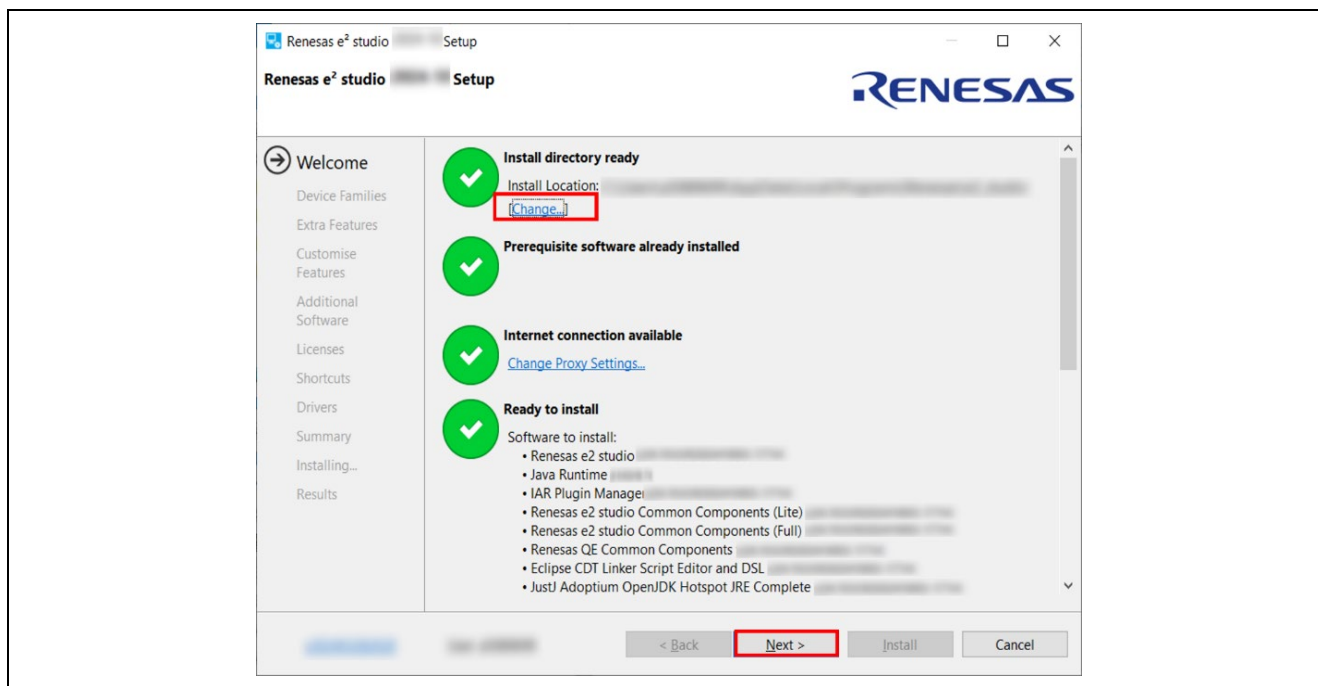


Figure 2. Installation of e² studio – Welcome page

3. Device Families

Select Device Families to install. Click the [Next >] button to continue.

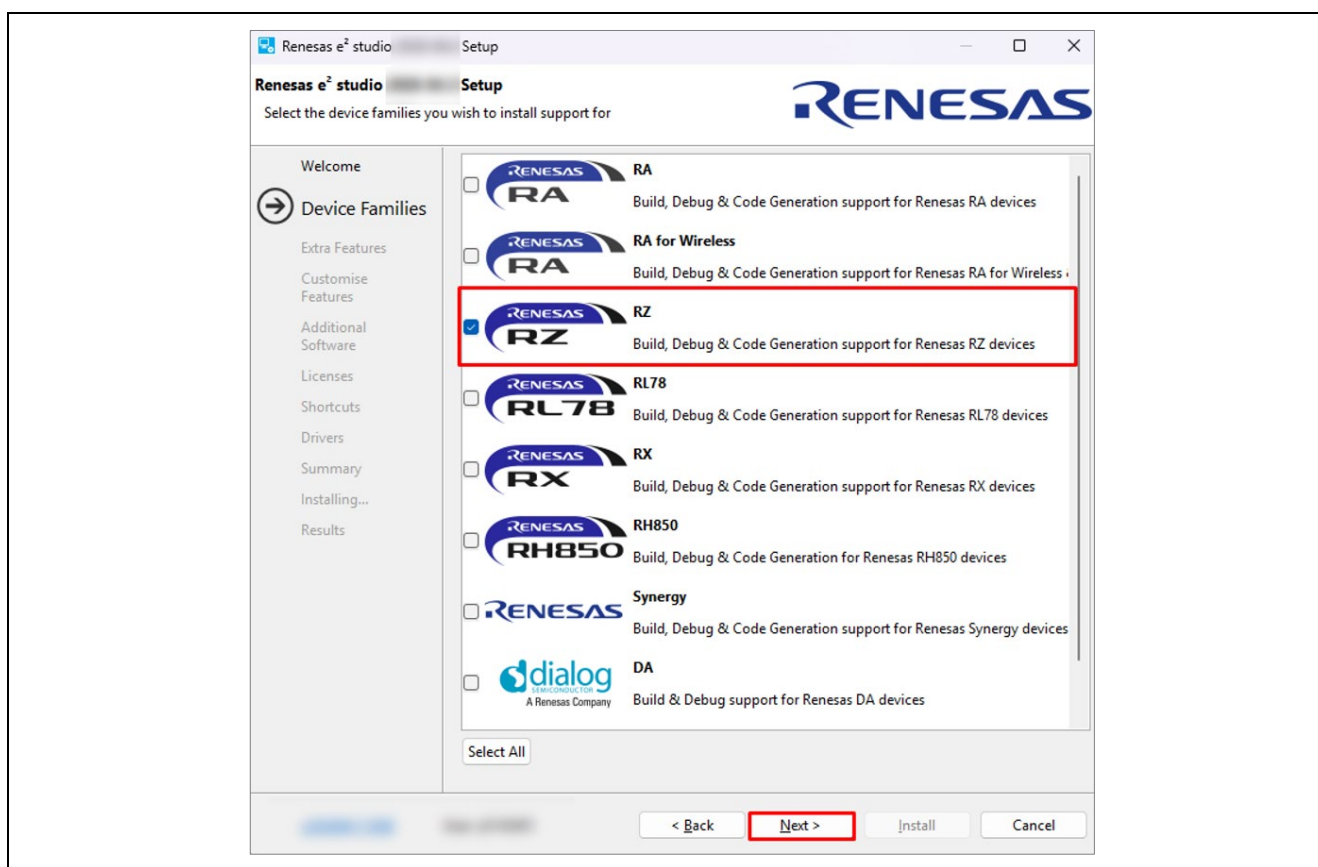


Figure 3. Installation of e² studio – Device Families

4. Extra Features

Select Extra Features (e.g., Language packs, SVN & Git support...) to be installed. For non-English language users, please select Language packs at this step if needed. Then, click the **[Next >]** button to continue.

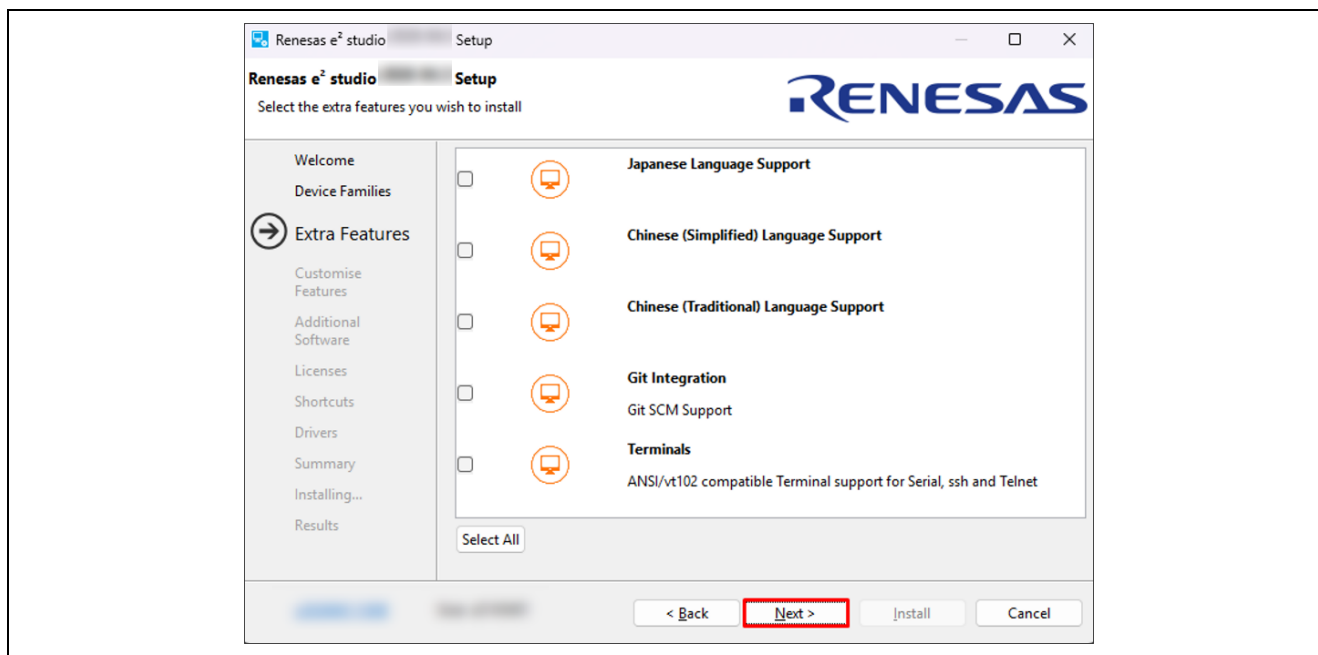


Figure 4. Installation of e² studio – Extra Features

5. Customize Features

Select the components to install and click the **[Next >]** button to continue. Ensure that the Renesas FSP Smart Configurator Core and the Renesas FSP Smart Configurator ARM are selected.

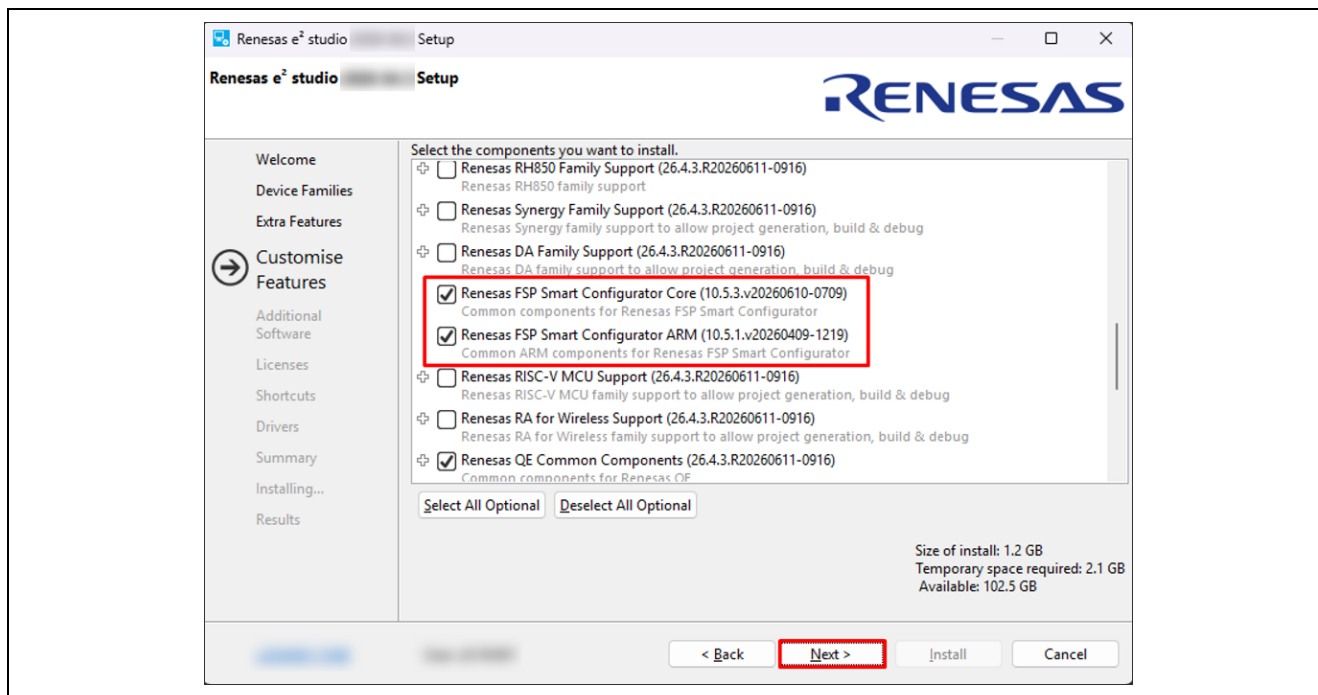


Figure 5. Installation of e² studio – Customize Features

6. Additional Software

Select additional software (i.e., compilers, utilities, QE...) to be installed. Be sure to select the toolchain item (**GNU ARM Embedded 13.3-Rel1**) and click the **[Next >]** button to continue.

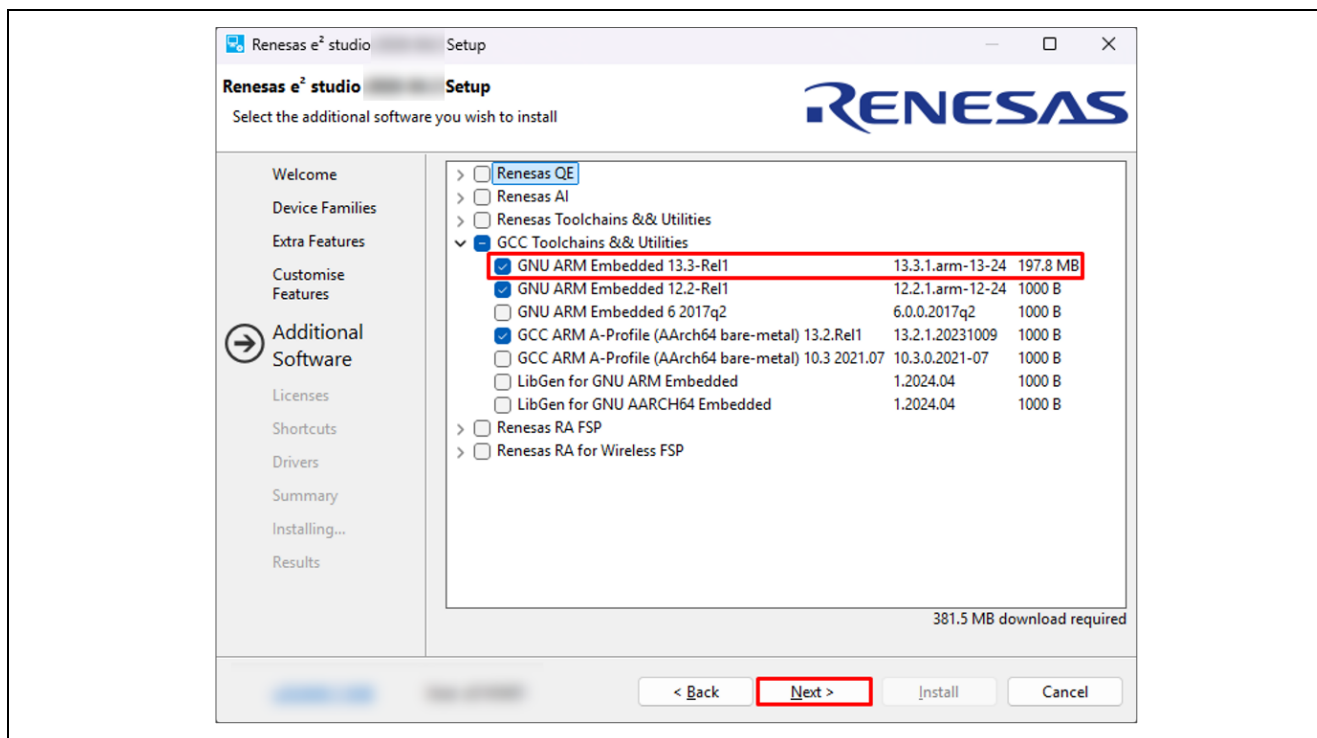


Figure 6. Installation of e² studio – Additional Software

For more details on the installation of Additional Software, please see section 2.1.3.3.

7. License Agreement

Read and accept the software license agreement. Click the **[Next >]** button. Please note that users must accept the license agreement; installation cannot continue.

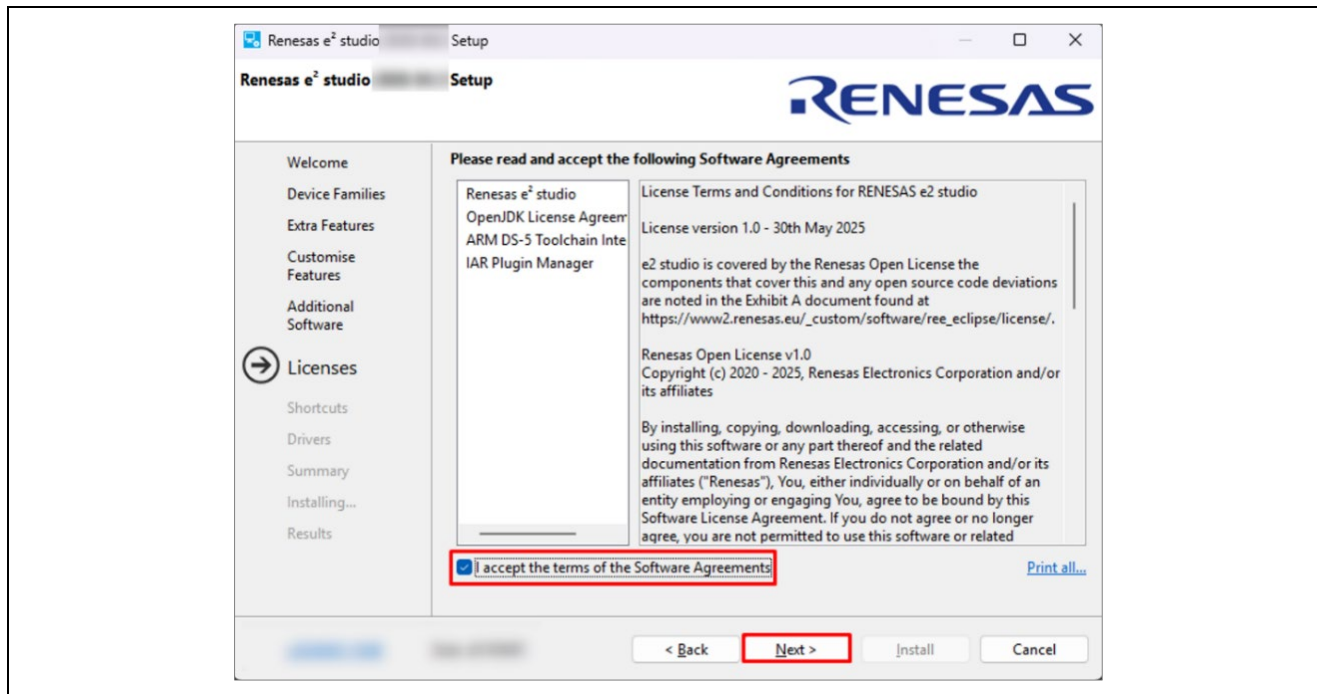


Figure 7. Installation of e² studio – Licenses

8. Shortcuts

Select the shortcut name for the Start menu and click the **[Next >]** button to continue.

Note: If e² studio has already been installed in another location, it is recommended to rename the shortcut to distinguish it from the other e² studio(s).

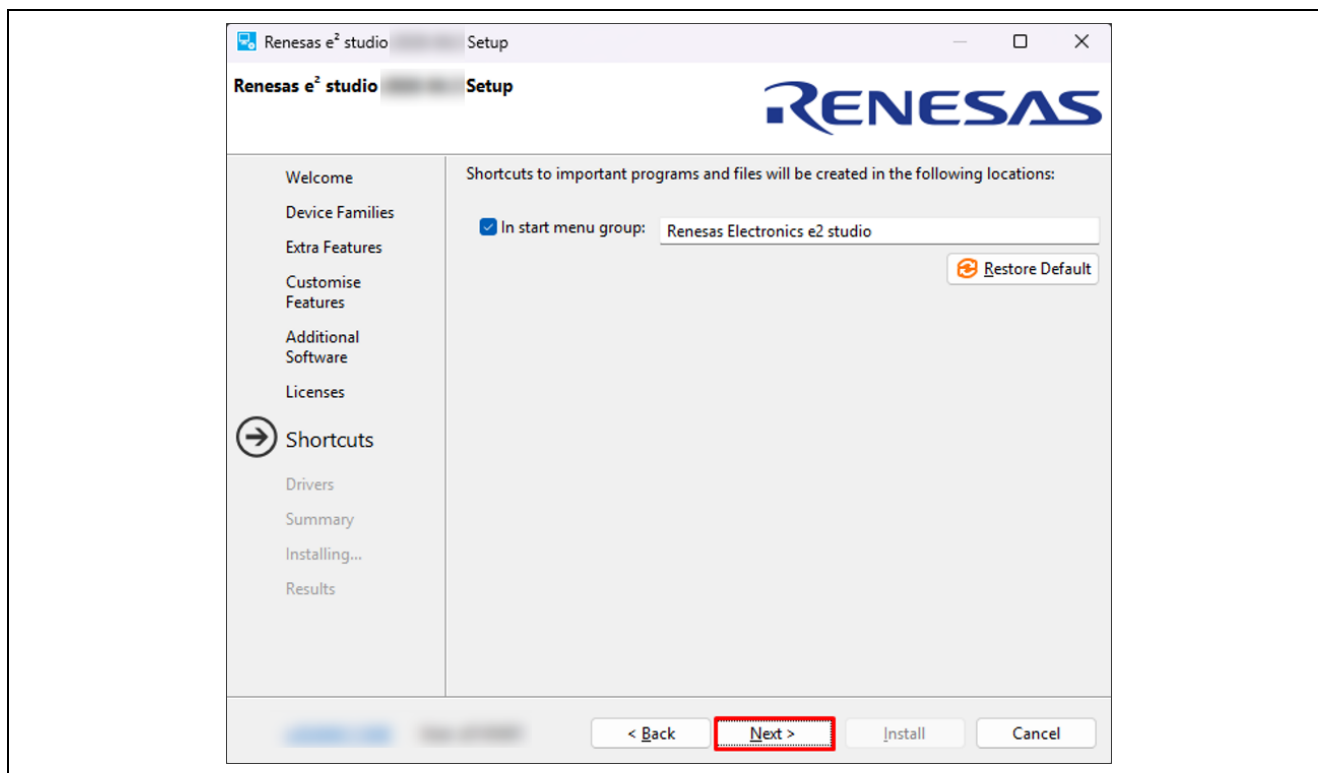


Figure 8. Installation of e² studio – Shortcuts

9. Summary

The components to be installed are shown. Please confirm the contents and click the **[Install]** button to install the Renesas e² studio IDE.

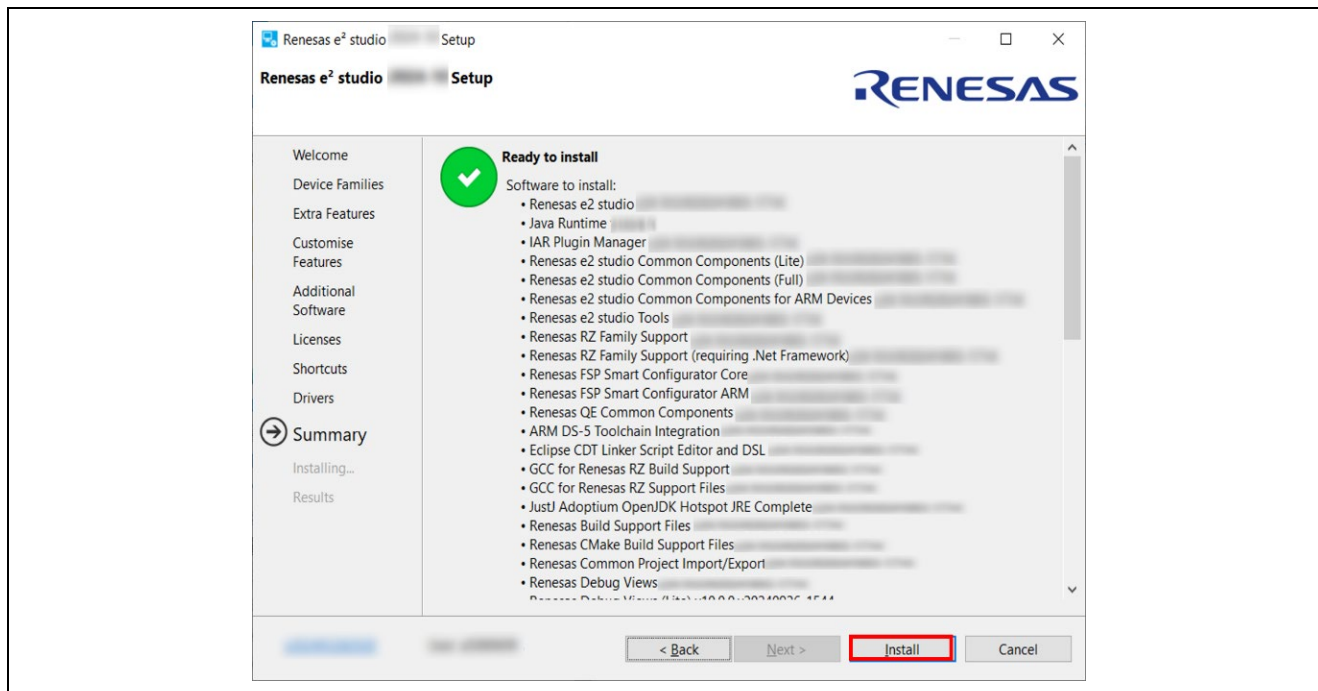


Figure 9. Installation of e² studio – Summary

10. Installing...

The installation will proceed. Depending on selected items of additional software, new dialog prompts may appear during the installation process. Please see section 2.1.3.3 for more detailed information.

11. Results

Click the **[OK]** button to complete the installation.

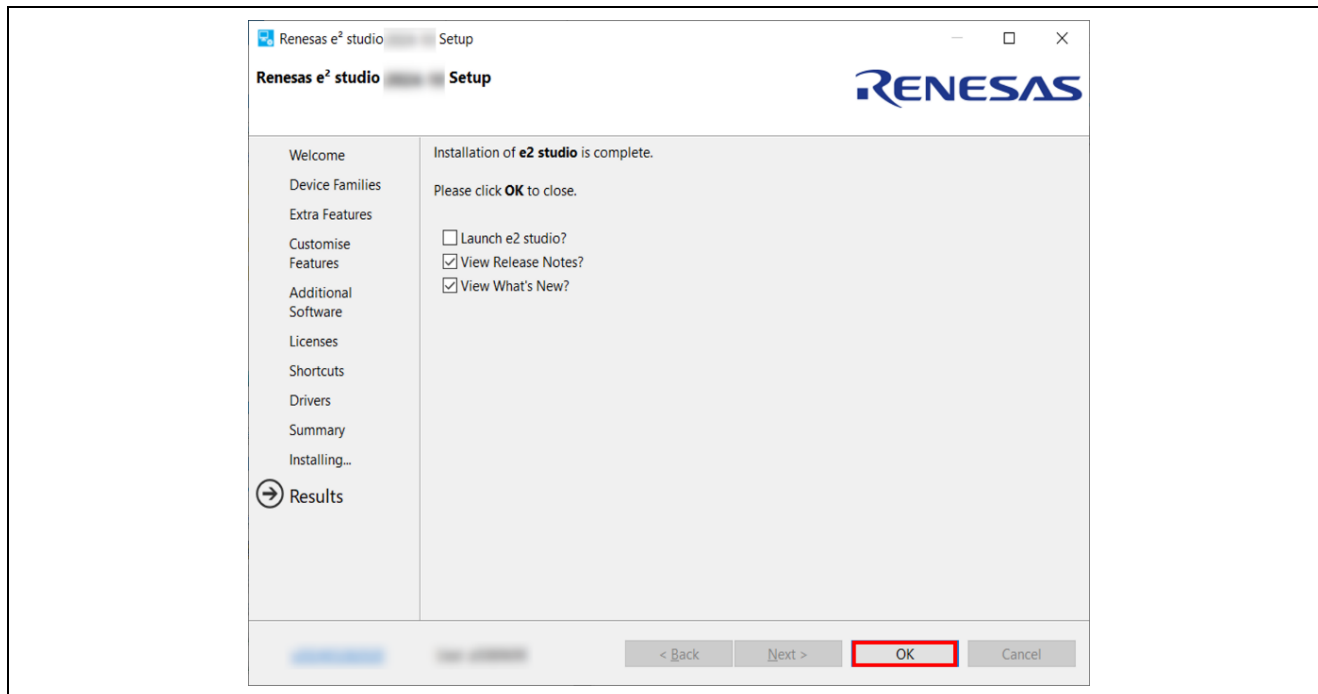


Figure 10. Summary Page

2.1.3.3 Installation of Additional Software

As mentioned in section 2.1.3.2, the additional software listed below is essential for RZ/G FSP.

- GNU ARM Embedded 13.3-Rel1.

The detailed procedure for installing these tools is provided in the following section.

- **GNU ARM Embedded Toolchain 13.3-Rel1**

If it was selected in the Additional Software pane of e² studio, you will see the installation wizard for the GNU ARM Embedded Toolchain during the installation process.

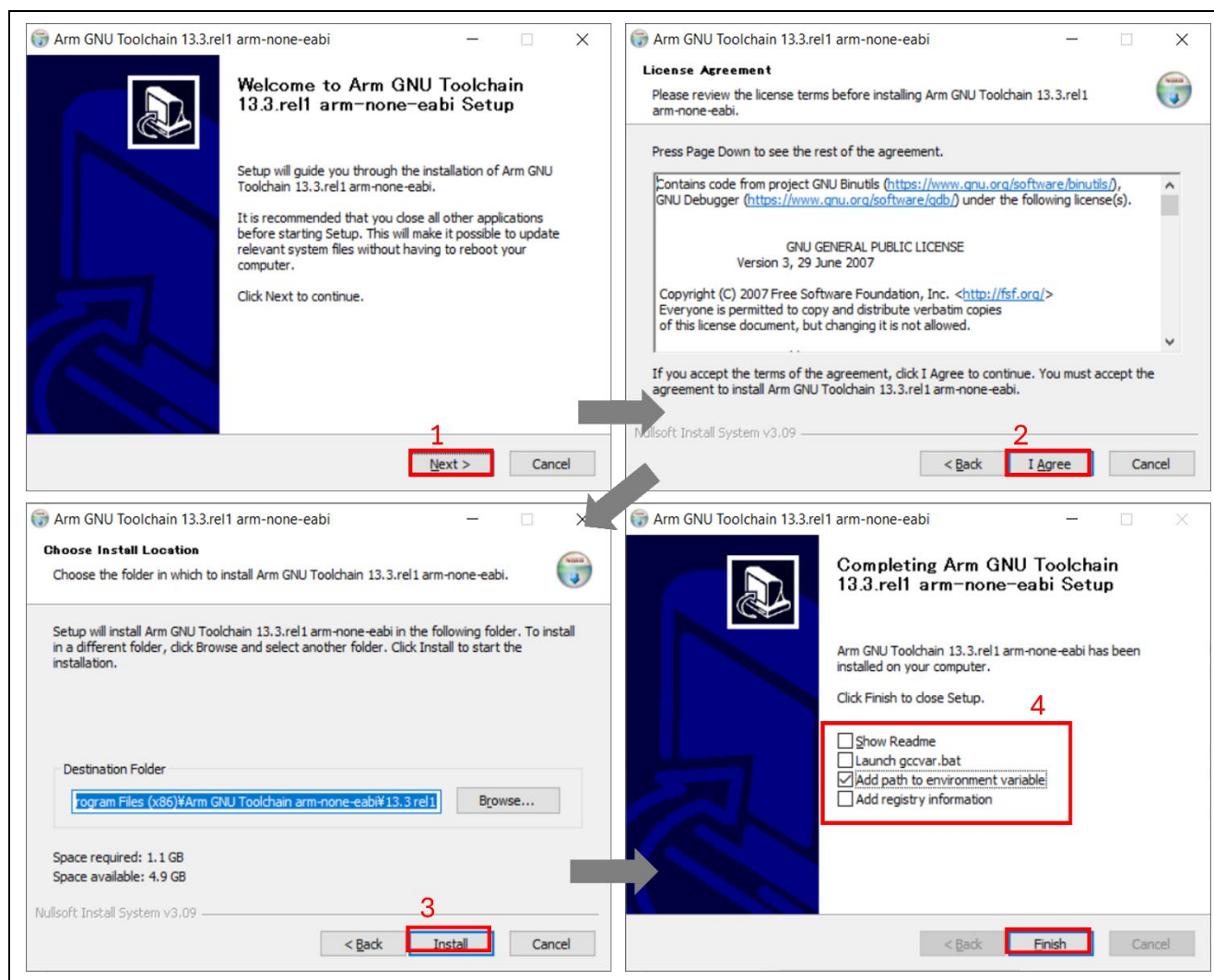


Figure 11. Installation of GNU ARM Embedded Toolchain

e² studio Installation for Linux PC

This chapter describes how to install the e² studio IDE on a Linux PC.

2.1.4.1 Download

The following files are required to download before installation.

- SEGGER J-Link driver
Please choose the version V9.44 or later and download the Linux 64-bit DEB Installer at the URL below:
<https://www.segger.com/downloads/jlink/>
- e² studio IDE installer
The e² studio IDE installer package can be downloaded from the Renesas website for free. Please check the detailed information from: https://www.renesas.com/e2_studio.

2.1.4.2 Installation

This section describes the procedure for each software installation.
Filename, version number, and file path are provided for example purposes only.

- SEGGER J-Link driver
Open a terminal window and enter the commands stated below.
sudo dpkg -i JLink_Linux_V944_x86_64.deb
(If the previous install fails with unmet dependencies, retry it as follows)


```
sudo apt-get -f install  
sudo dpkg -i JLink_Linux_V944_x86_64.deb
```

- e² studio IDE

1. Run the e² studio IDE Installer

Note: Before running the installer, check the execution permission of the installer.)

```
./e2studio_installer-2026-07_linux_host.run
```

2. Select Install Type

Users need to select Install Type as shown below. In this material, it is expected that Custom Install will be selected. Then, click the **[Next >]** button to continue.

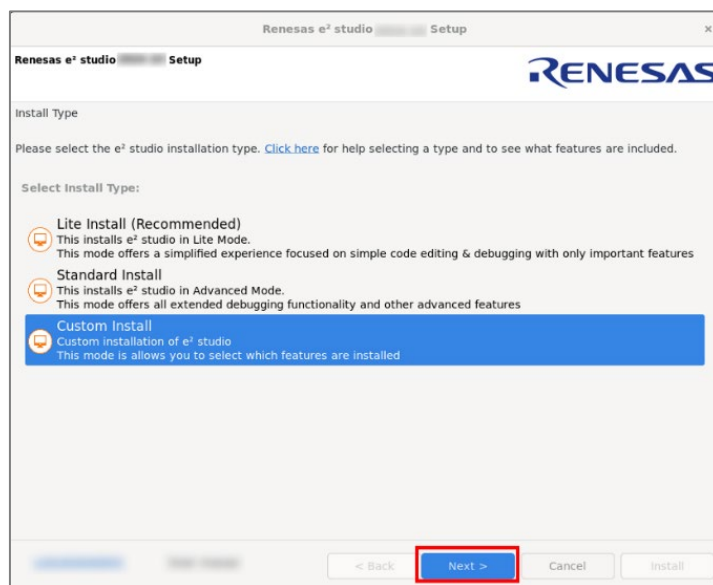


Figure 12. Selection of Install Type

3. Welcome page (Cont'd)

Users can change the install folder by clicking the **[Change...]** button.

Click the **[Next >]** button to continue.

Note 1: If you would like to have multiple versions of e² studio, please specify a new folder here.

Note 2: Multi-byte characters cannot be used for the e² studio installation folder name.

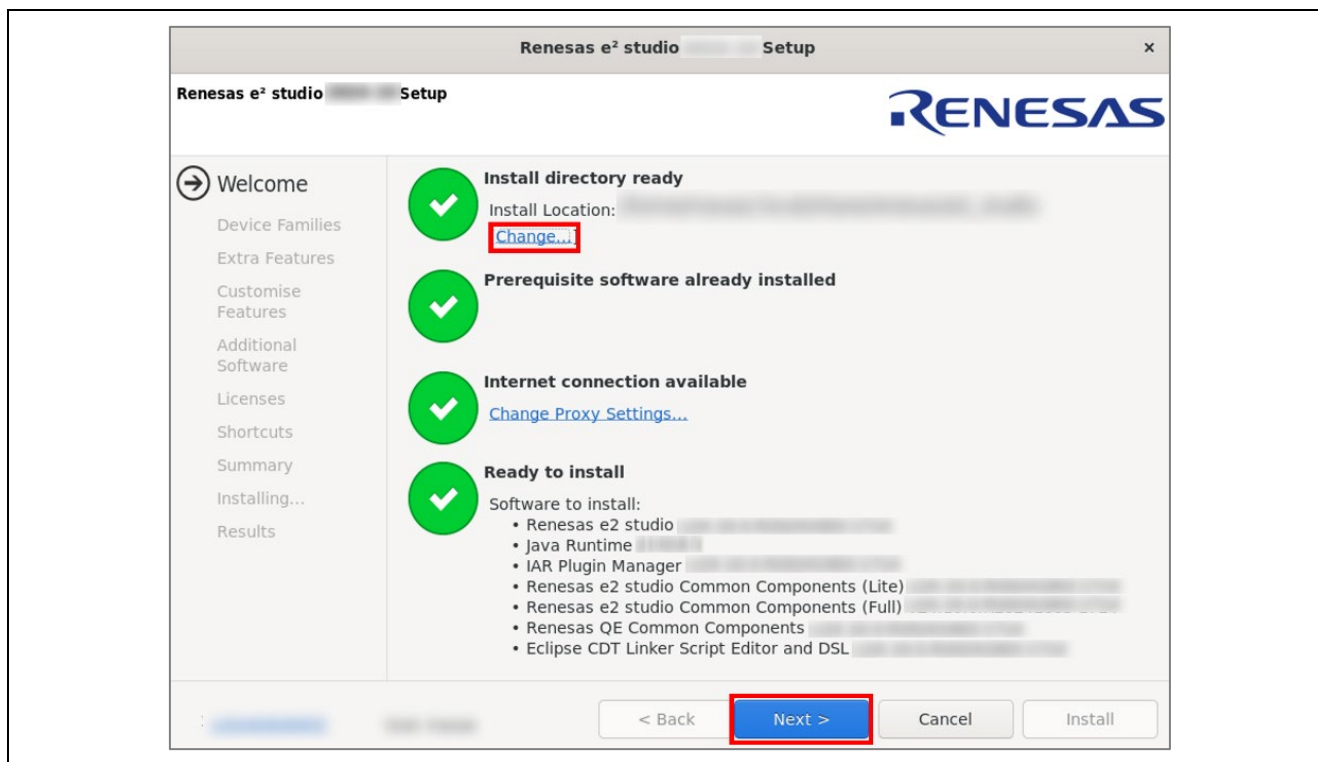


Figure 13. Installation of e² studio – Welcome page

4. Device Families

Select Device Families to install. Click the [Next >] button to continue.

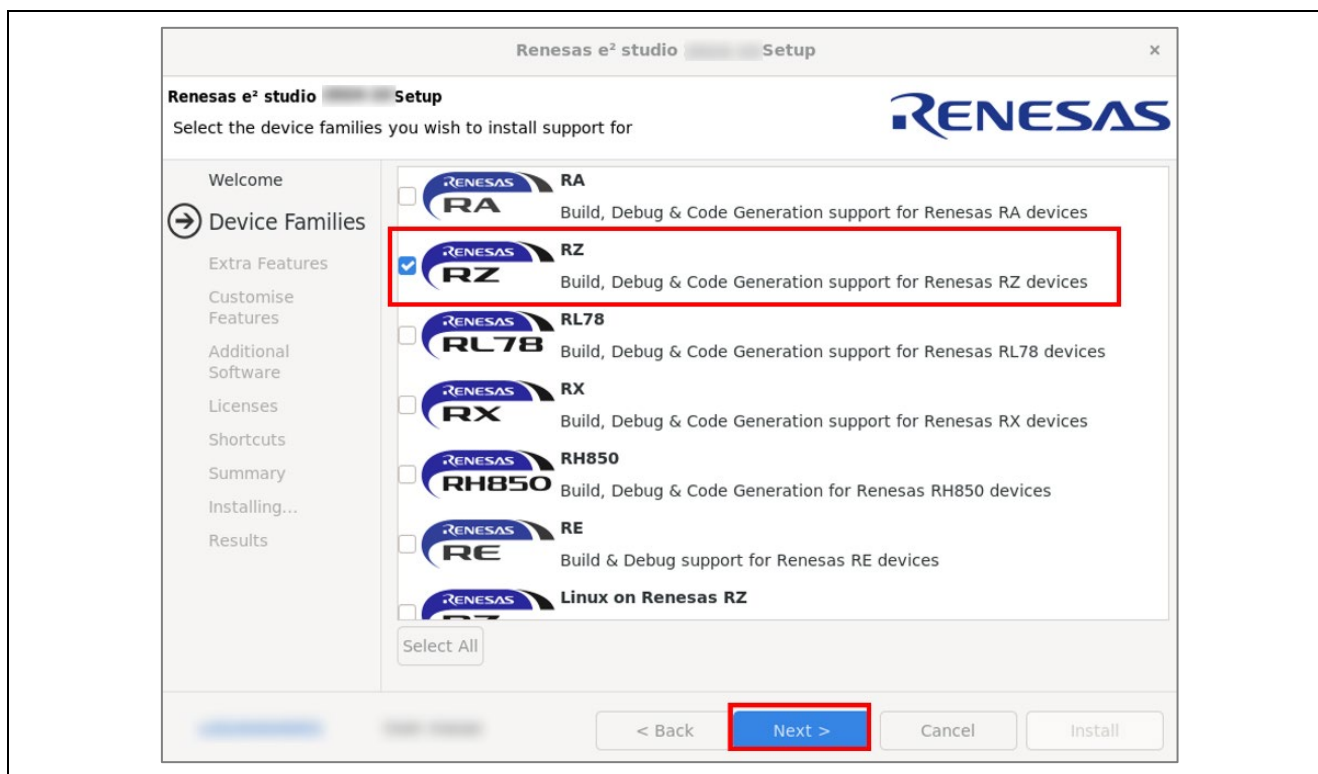


Figure 14. Installation of e² studio – Device Families

5. Extra Features

Select Extra Features (e.g., Language packs, SVN & Git support...) to be installed. For non-English language users, please select Language packs at this step if needed. Then, click the **[Next >]** button to continue.

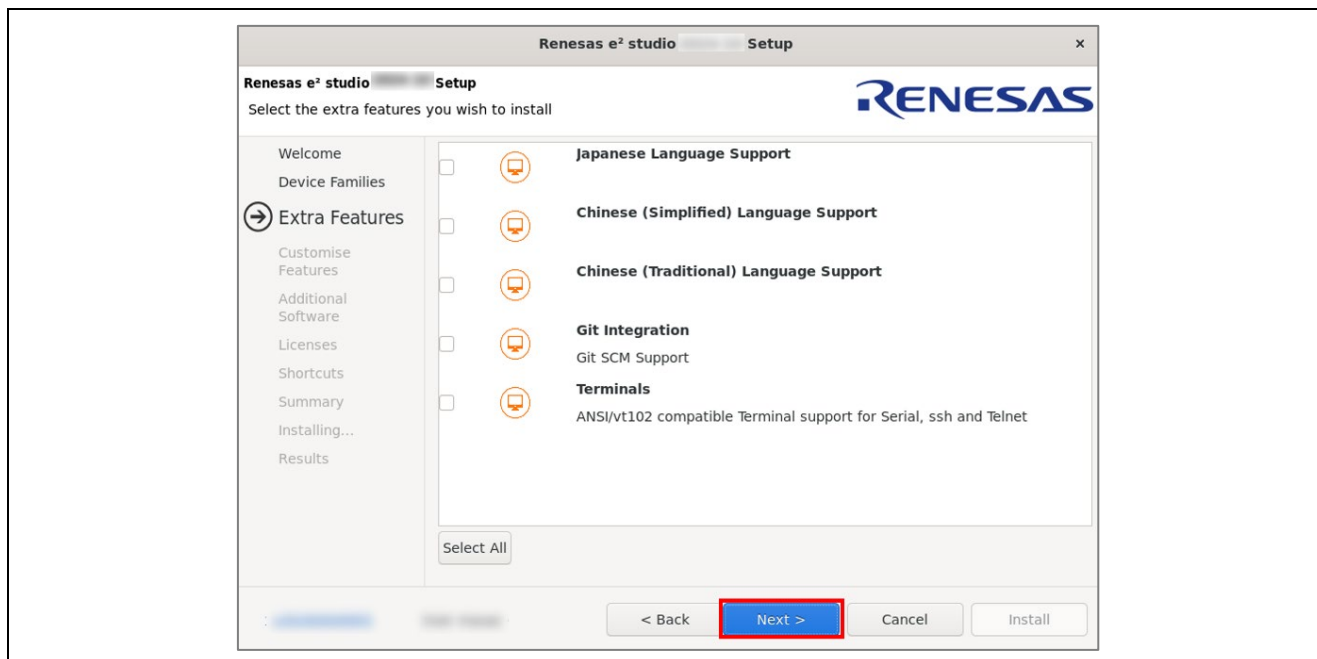


Figure 15. Installation of e² studio – Extra Features

6. Customize Features

Select the components to install and click the **[Next >]** button to continue. Be sure that Renesas FSP Smart Configurator Core and Renesas FSP Smart Configurator ARM are selected.

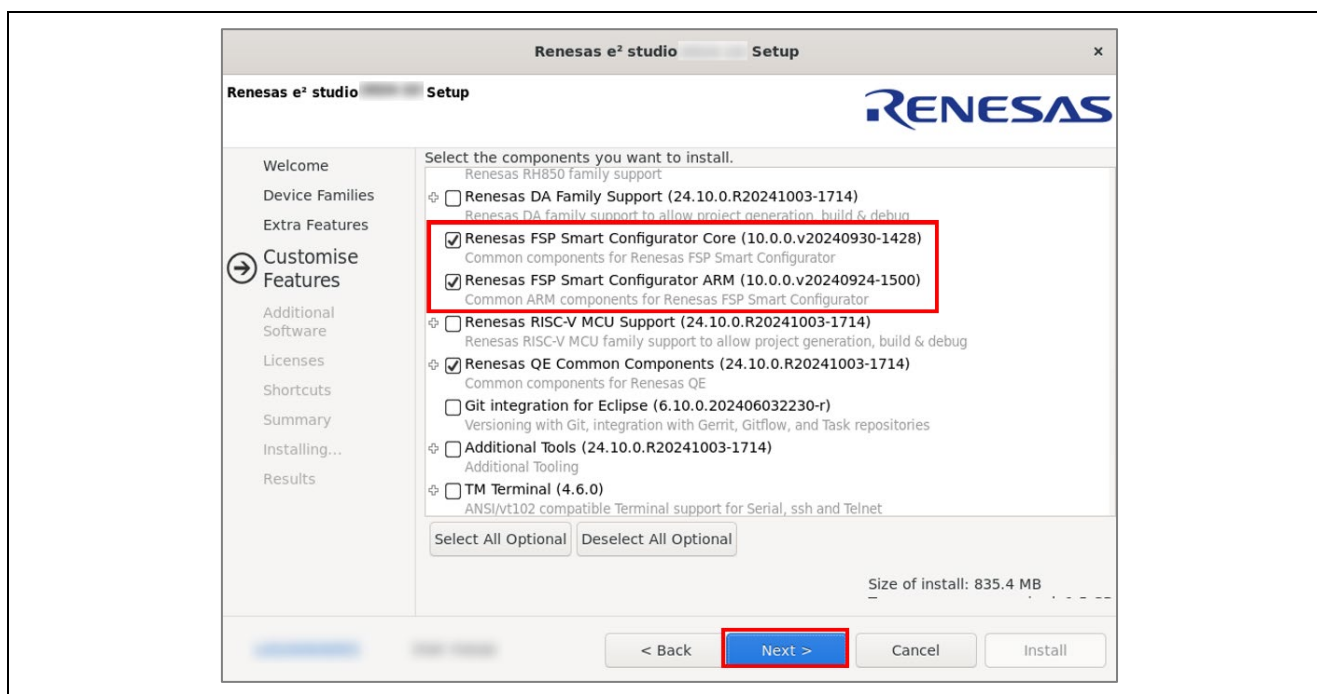


Figure 16. Installation of e² studio – Customize Features

7. Additional Software

Select the additional software (i.e., compilers, utilities, QE...) to be installed.

Be sure to select the “GNU ARM Embedded 13.3-Rel1” and click the **[Next >]** button to continue.

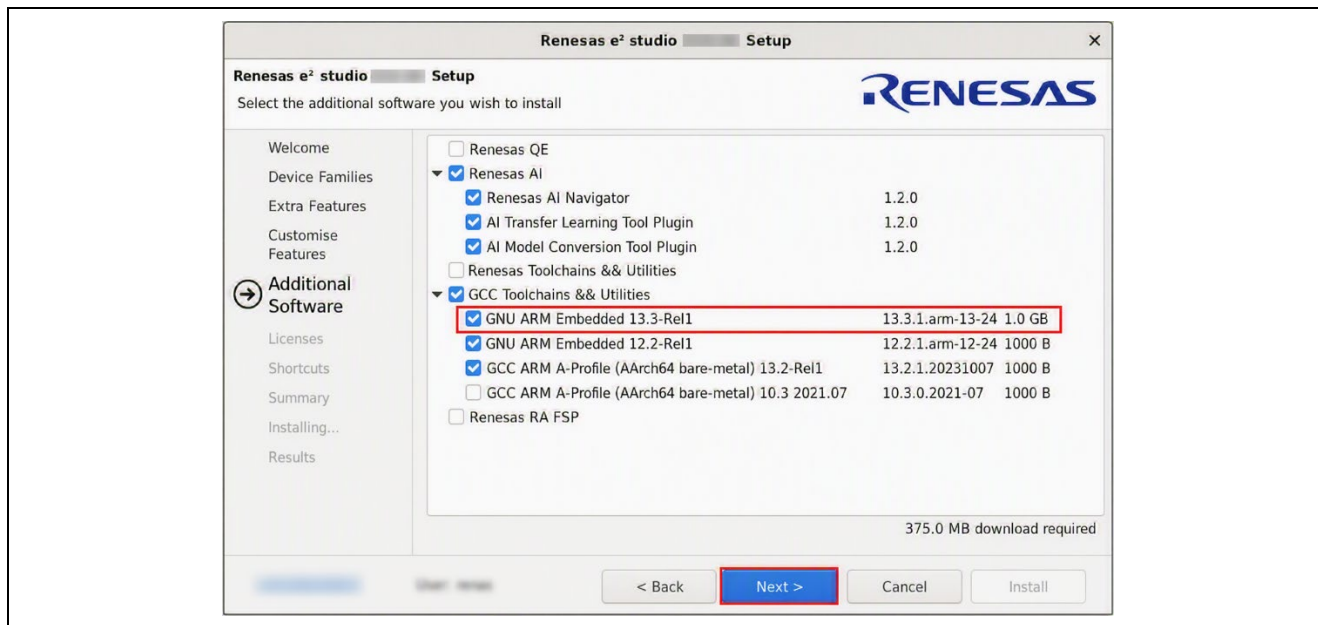


Figure 17. Installation of e² studio – Additional Features

8. License Agreement

Read and accept the software license agreement. Click the **[Next >]** button to continue.

Please note that the user must accept the license agreement; installation cannot continue.

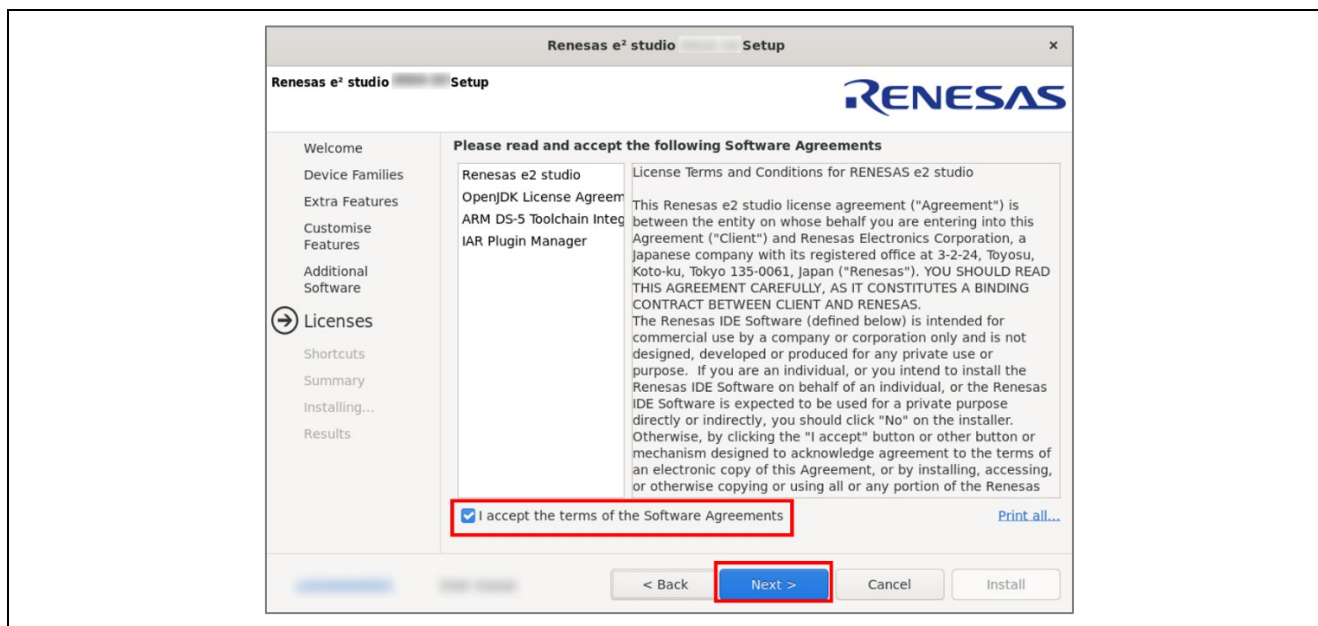


Figure 18. Installation of e² studio – Licenses

9. Shortcuts

Select the shortcut name for the Start menu and click the **[Next >]** button to continue.

Note: If e² studio was installed in another location, it is recommended to rename it to distinguish it from the other e² studio(s).

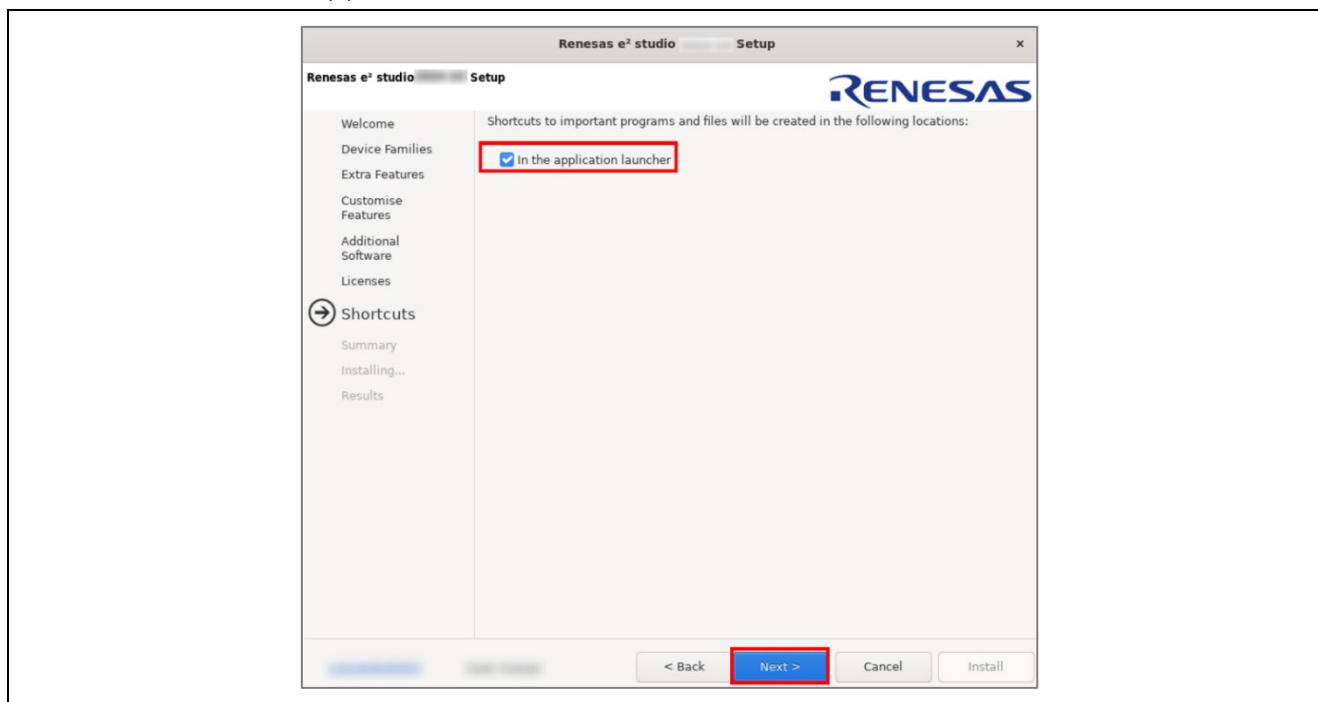


Figure 19. Installation of e² studio – Shortcuts

10. Summary

The components to be installed are shown. Please confirm the contents and click the **[Install]** button to install the Renesas e² studio IDE.

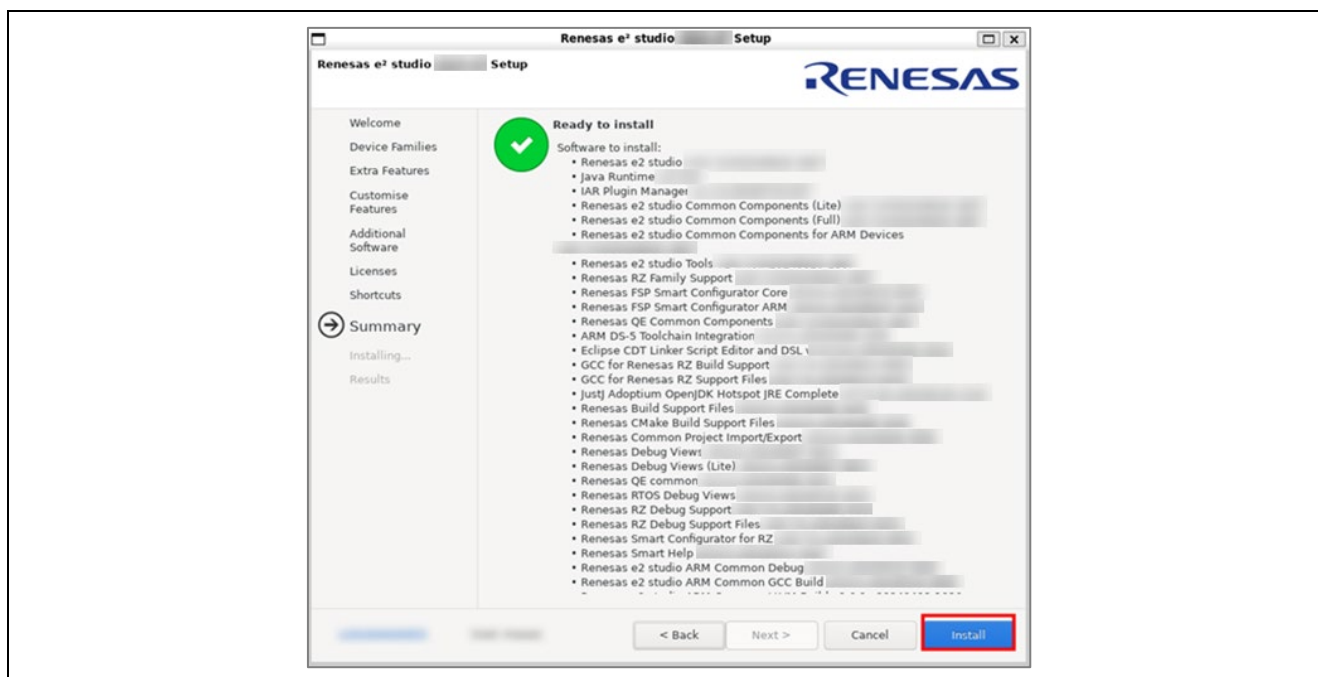


Figure 20. Installation of e² studio – Summary

11. Installing...

The installation is performed. Depending on the selected items of additional software, new dialog prompts may appear during the installation process.

12. Results

Click the **[OK]** button to complete the installation.

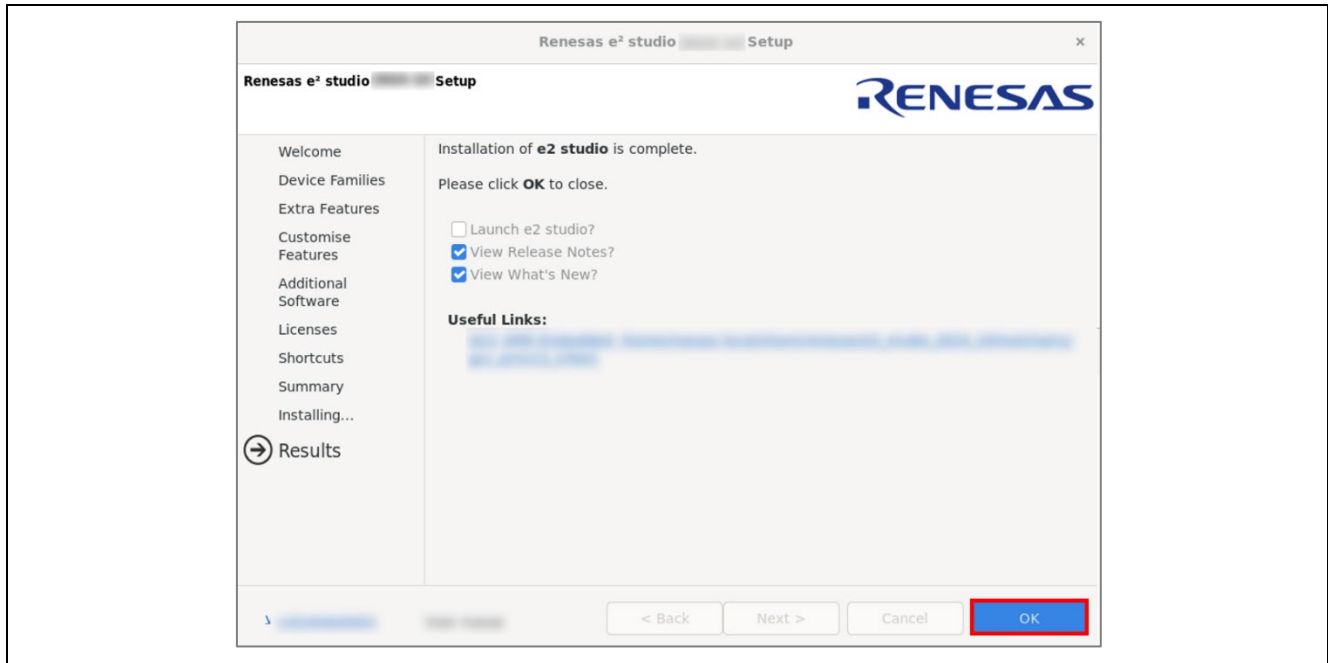


Figure 21. Installation of e² studio – Results

2.2 FSP Setup

2.2.1 Installation of FSP using Package Installer

Package Installer **RZ_FSP_Packs_v4.2.0.exe** is showcased [here](#). Please note that it's for the Windows Host PC only.

1. Quit e² studio.
2. Invoke RZ_FSP_Packs_v4.2.0.exe.
3. Click **[Next >]** to start the installation.

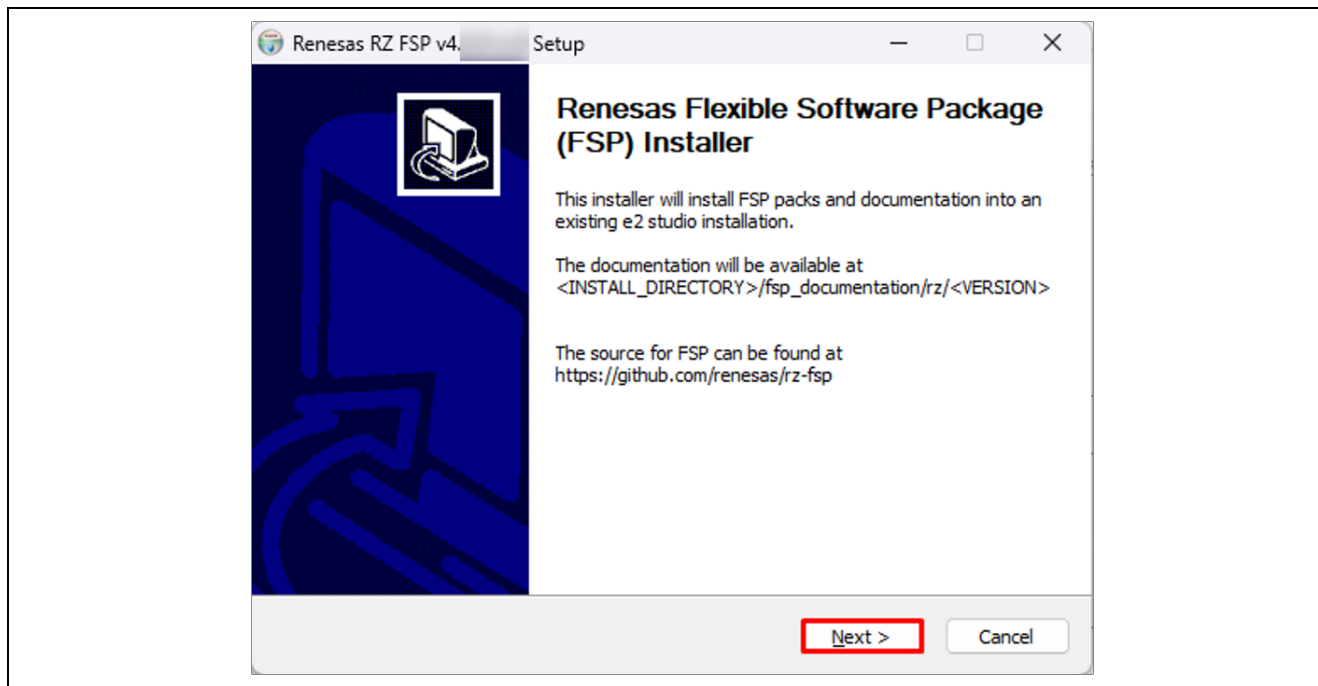


Figure 22. FSP Package Installer

4. See the license terms and click the **[I Agree]** button if it's acceptable.

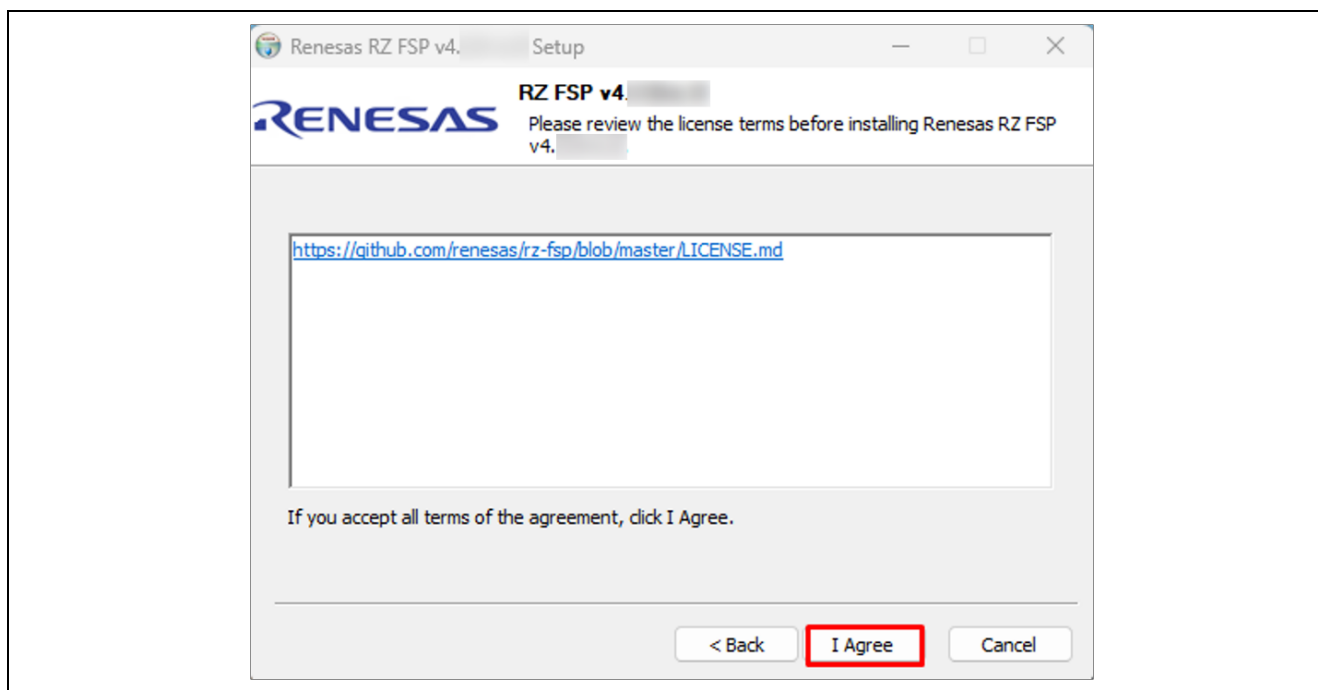


Figure 23. FSP License Term

5. Specify the e² studio installation folder (e.g., C:\Renesas\e² studio) and click the **[Install]** button.

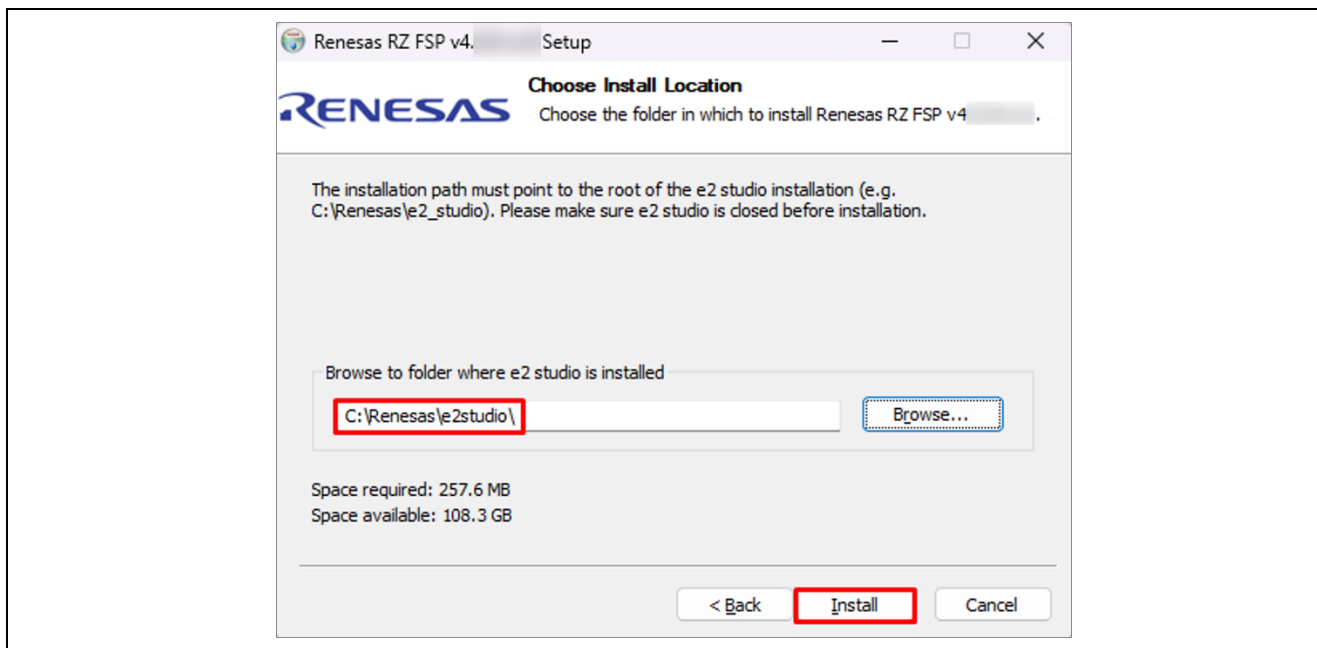


Figure 24. Browse to the folder where e² studio is installed

6. Click the **[Finish]** button to complete the installation.

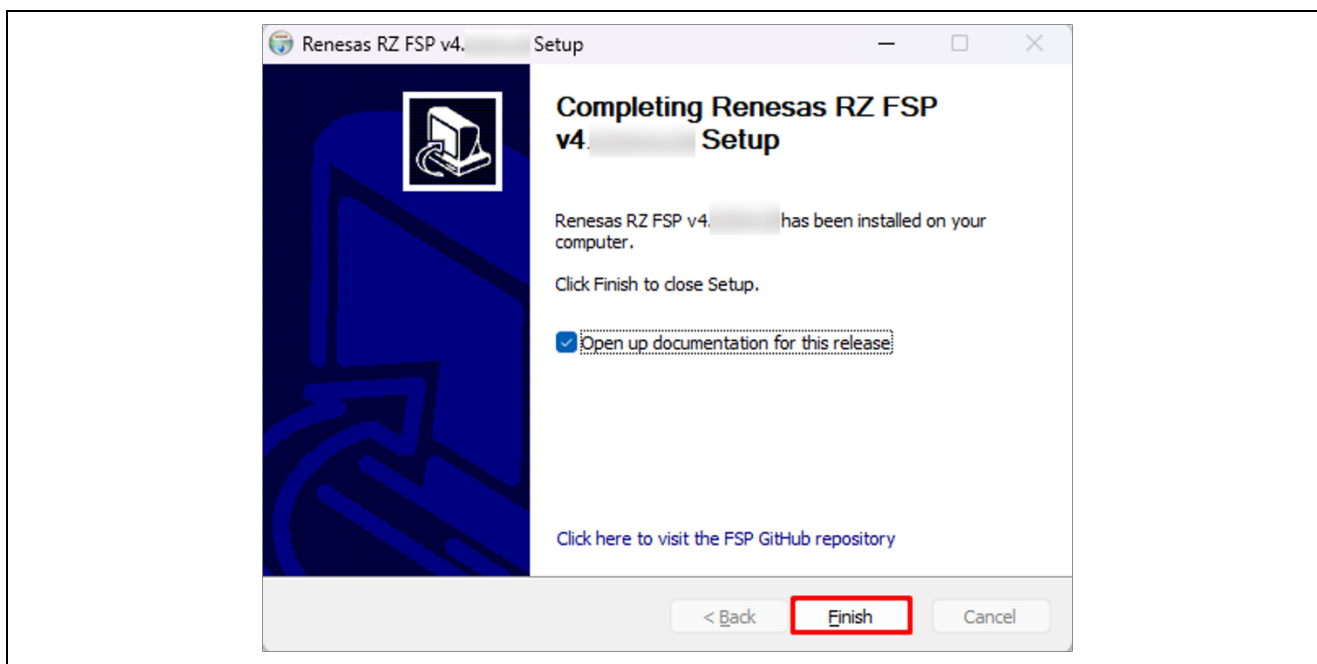


Figure 25. Completion of FSP Installation

If the box **Open up documentation for this release** is checked at that time, FSP documentation for the installed version of FSP should be opened.

2.2.2 Installation of FSP Packs using Package Zip file

No Package installer is available for the Linux Host PC, and therefore, you need to install FSP Packs with **RZ_FSP_Packs_v4.2.0.zip**. This section describes how to install it. Please note that the same installation procedure is valid for the Windows Host PC.

1. Download **RZ_FSP_Packs_v4.2.0.zip** from [here](#).
2. Extract the zip file to the e² studio installation directory. If it's successfully extracted, **rz_fsp/packs** should be placed at **<e2 studio installation directory>/internal/projectgen**.

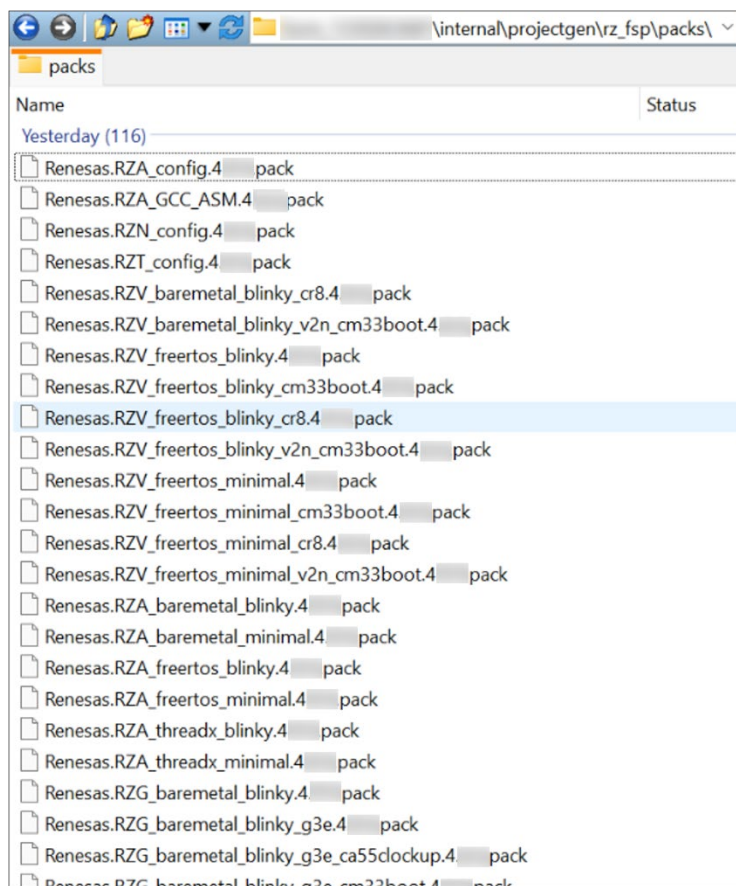


Figure 26. FSP Packs on the e² studio installation directory

3. At the first invocation of e² studio after the extraction, FSP should be automatically installed.
4. You can check if the installation is successful by following the procedure below:
 - Click Help > CMSIS Packs Management > Renesas RZ

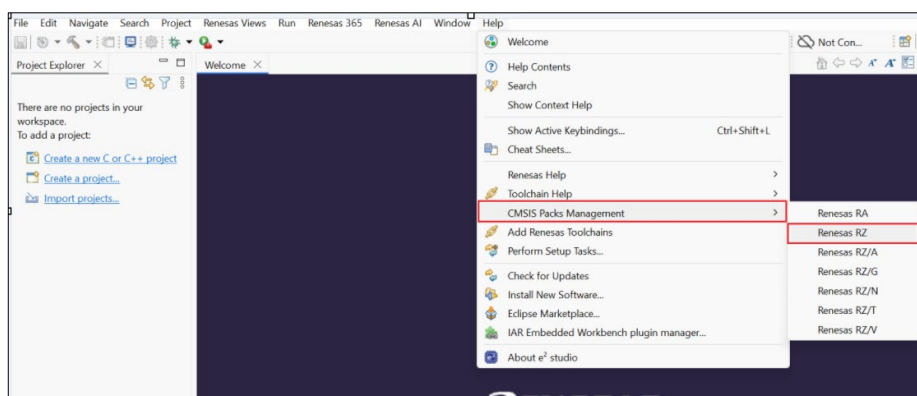


Figure 27. CMSIS Packs Management (1)

- If FSP is successfully installed, 4.2.0 should be listed under FSP as shown below:

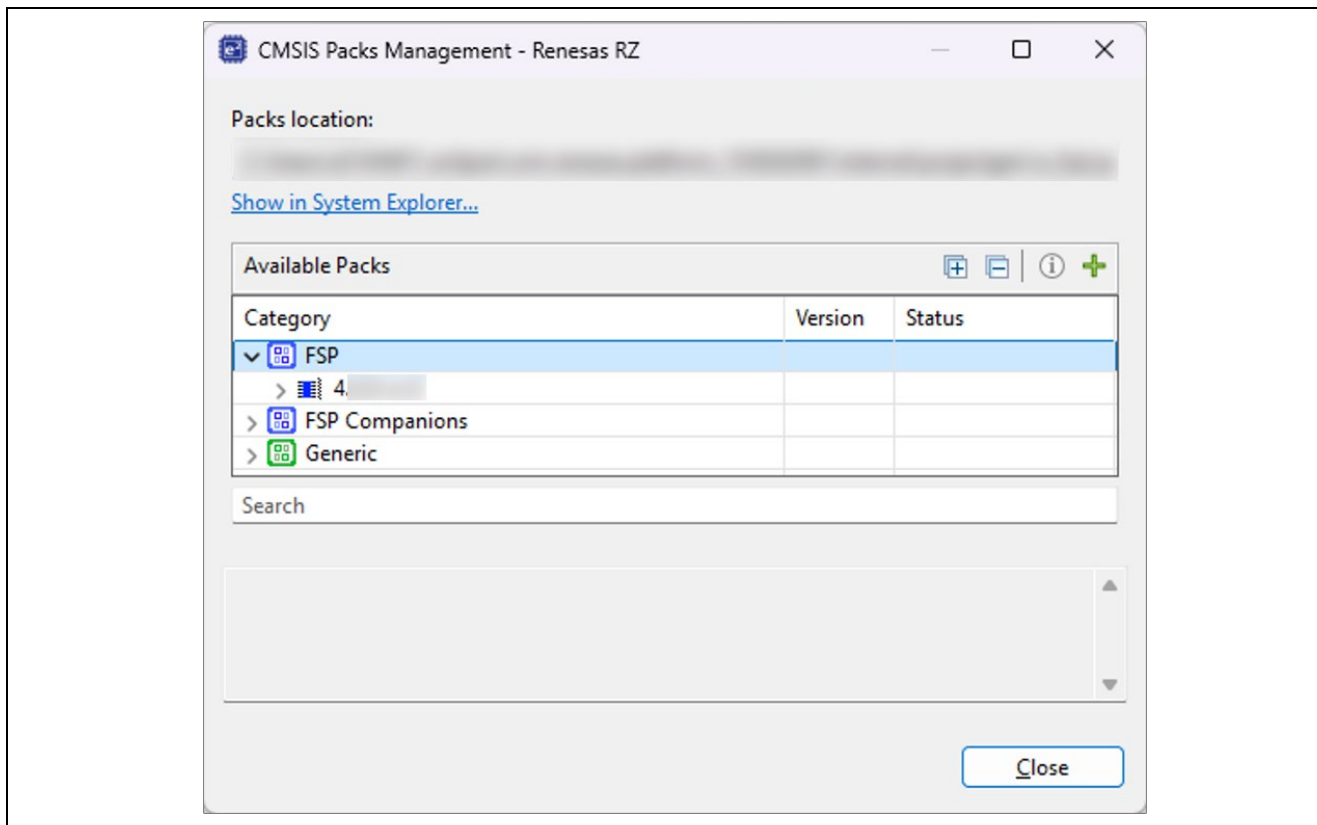


Figure 28. CMSIS Packs Management (2)

3. Set up an SMARC EVK

3.1 RZ/G2L SMARC EVK

Below is an example of a typical system configuration.

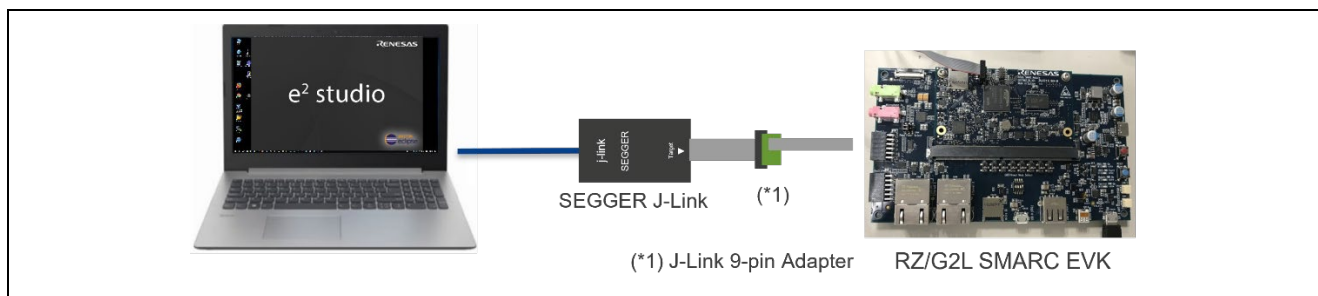


Figure 29. System Configuration Example – RZ/G2L SMARC EVK

3.1.1 Supported Debugger

- SEGGER J-Link

For details on SEGGER J-Link, please see [J-Link Debug Probes by SEGGER – the Embedded Experts](#).

3.1.2 Board Setup

3.1.2.1 Boot MODE

To set the board to Boot mode 3 (QSPI Boot (1.8V) Mode), set SW11 as below.

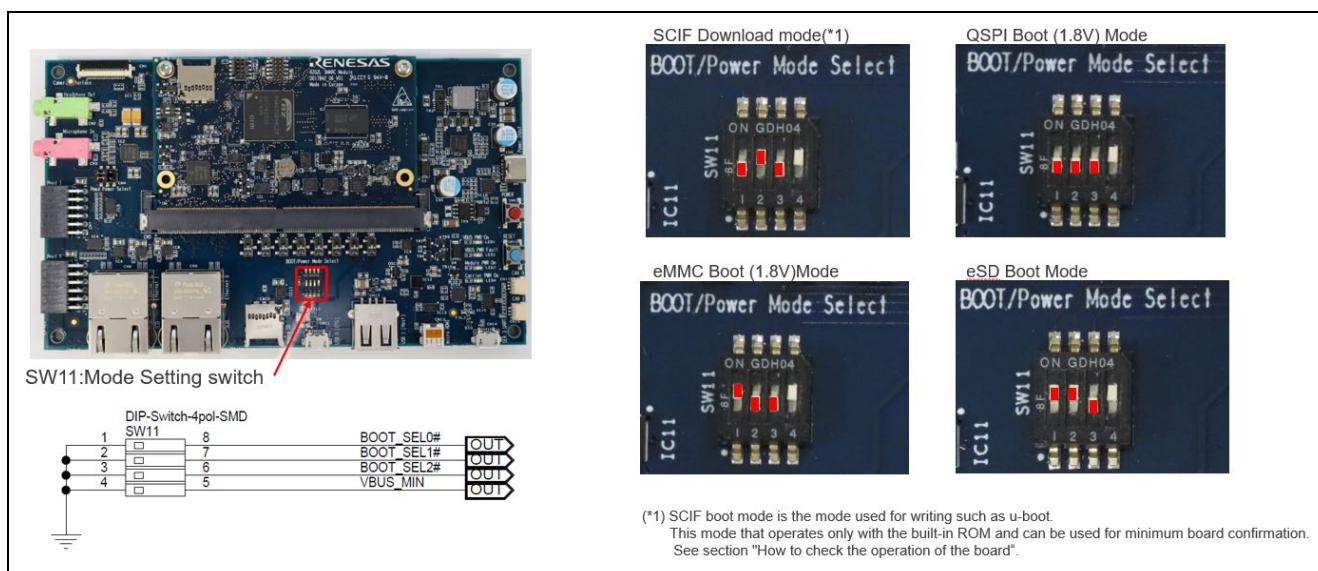


Figure 30. Boot MODE

JTAG connection

When connecting JTAG, you must set the DIP SW1 settings as follows:

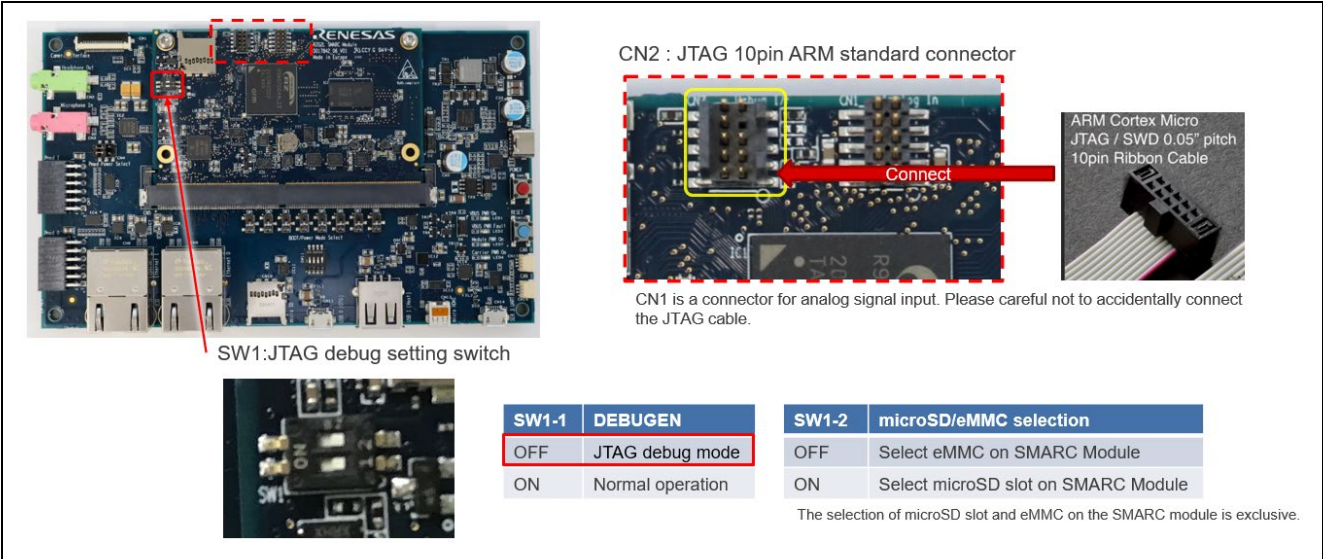


Figure 31. JTAG connection

Please note that RZ/G2L SMARC EVK has a CoreSight 10 connector and therefore, the following adapter is needed to connect to Segger J-Link.

<https://www.segger.com/products/debug-probes/j-link/accessories/adapters/9-pin-cortex-m-adapter/>

3.1.2.3 Debug Serial (console output)

Debug serial uses CN14. The baud rate is 115200bps.

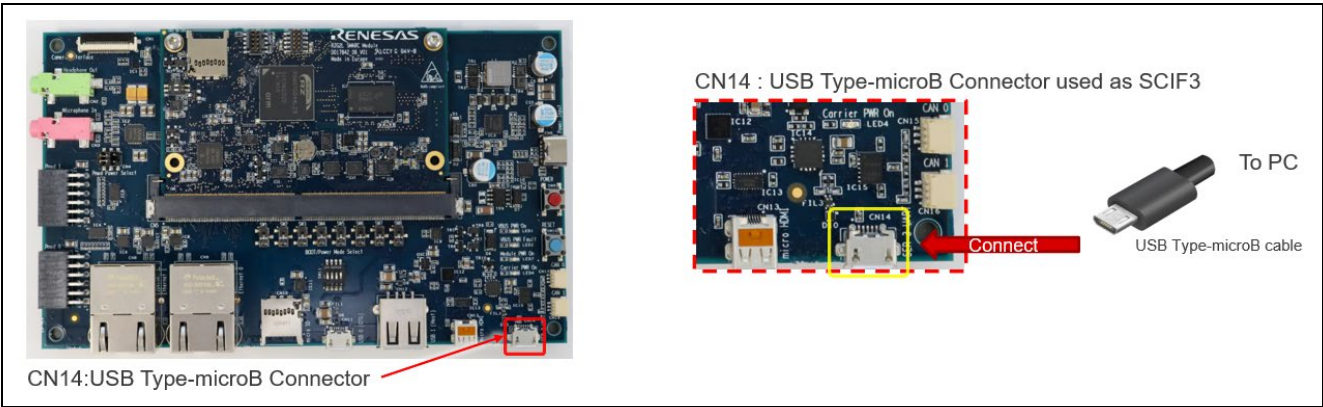


Figure 32. Debug Serial (console output)

Power Supply

Here are the power supply-related items to be used for Renesas development. Please prepare equivalent items for your development.

- USB Type-C cable CB-CD23BK (manufactured by Aukey)
- USB PD Charger Anker PowerPort III 65W Pod (manufactured by Anker)

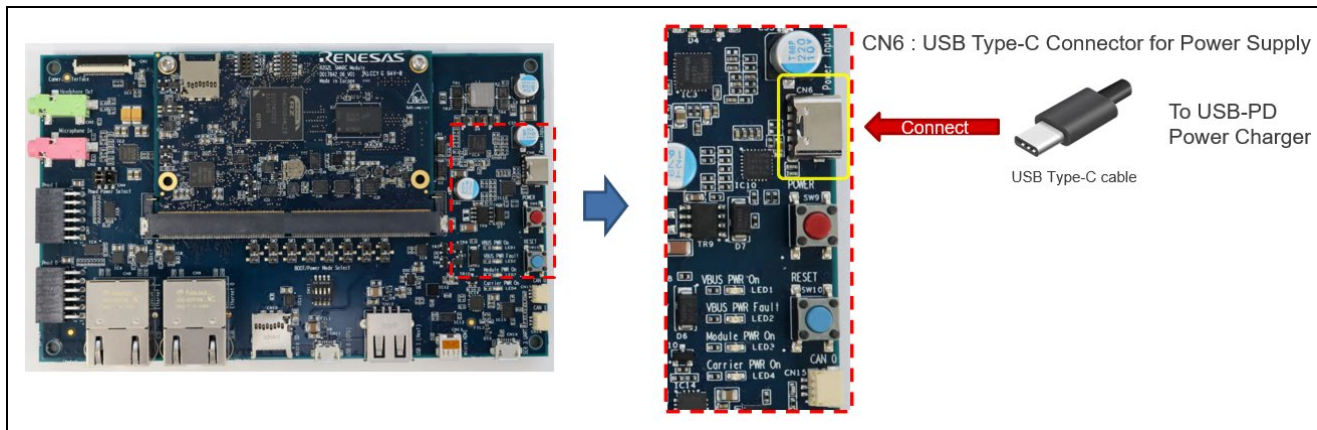


Figure 33. Power Supply

Connect the USB-PD Power Charger to the USB Type-C Connector. Then LED1(VBUS PWR On) and LED3 (Module PWR On) light up. Press SW9 to turn on the power. Then LED4(Carrier PWR On) lights up.

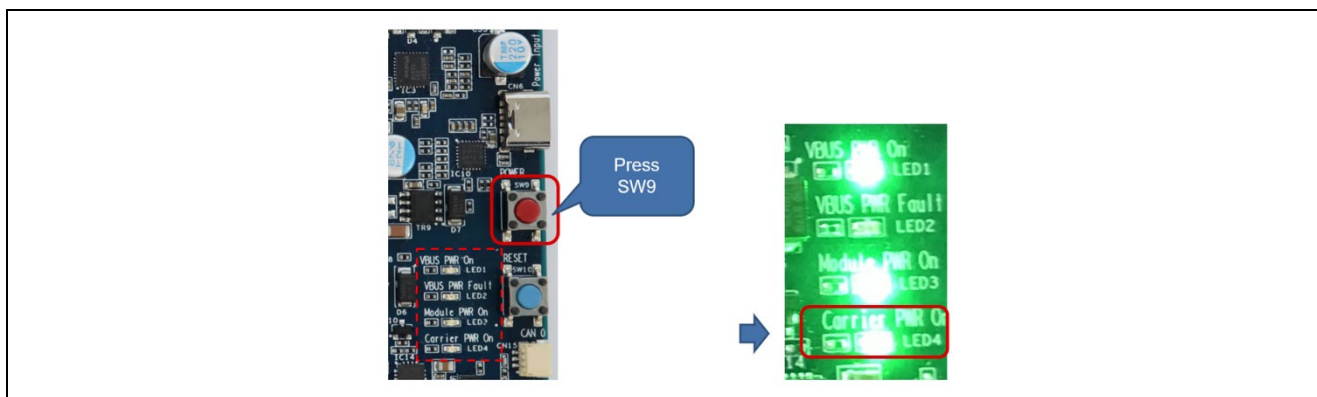


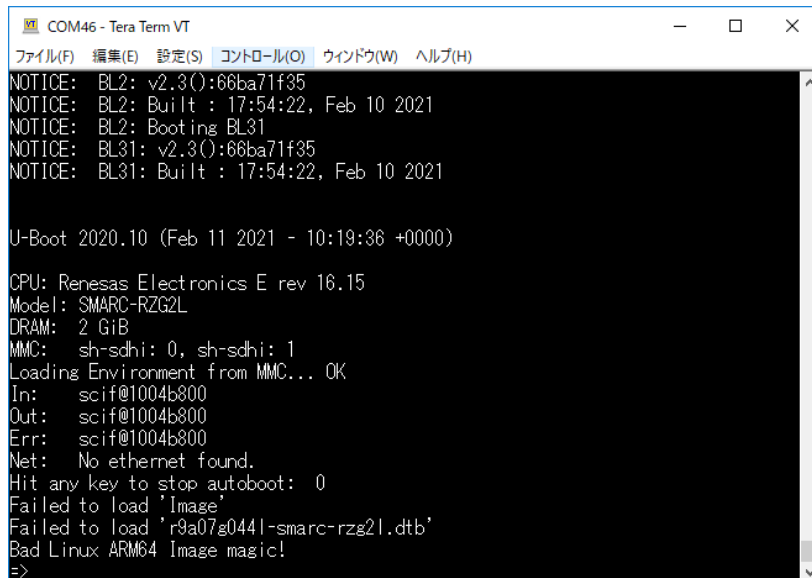
Figure 34. LED Status after Turning on EVK

How to Check the Operation of the Board

First, check the board for problems. There are two ways to do this. Please check with either.

BOOT MODE: QSPI Boot (1.8V) Mode

If U-Boot is written to the serial flash, when the power is turned ON, the following will be output to the console (CN14).



```
COM46 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
NOTICE: BL2: v2.3():66ba71f35
NOTICE: BL2: Built : 17:54:22, Feb 10 2021
NOTICE: BL2: Booting BL31
NOTICE: BL31: v2.3():66ba71f35
NOTICE: BL31: Built : 17:54:22, Feb 10 2021

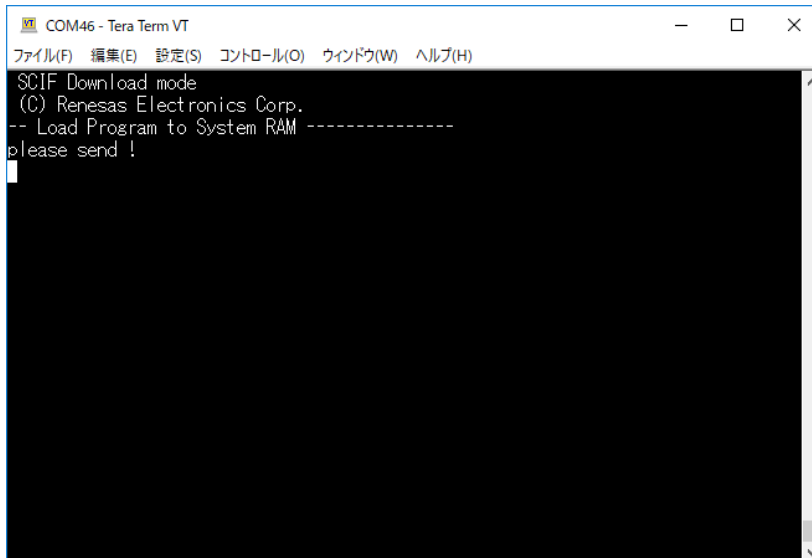
U-Boot 2020.10 (Feb 11 2021 - 10:19:36 +0000)

CPU: Renesas Electronics E rev 16.15
Model: SMARC-RZG2L
DRAM: 2 GiB
MMC: sh-sdhi: 0, sh-sdhi: 1
Loading Environment from MMC... OK
In:  scif@1004b800
Out: scif@1004b800
Err: scif@1004b800
Net:  No ethernet found.
Hit any key to stop autoboot:  0
Failed to load 'Image'
Failed to load 'r9a07g044l-smarc-rzg2l.dtb'
Bad Linux ARM64 Image magic!
=>
```

Figure 35. RZ/G2L BOOT MODE: QSPI Boot (1.8V) Mode

BOOT MODE: SCIF Download Mode

When the power is turned on, the following will be output to the console (CN14).



```
COM46 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
SCIF Download mode
(C) Renesas Electronics Corp.
-- Load Program to System RAM -----
please send !
```

Figure 36. RZ/G2L BOOT MODE: SCIF Download Mode

RZ/G3S SMARC EVK

Below is an example of a typical system configuration.

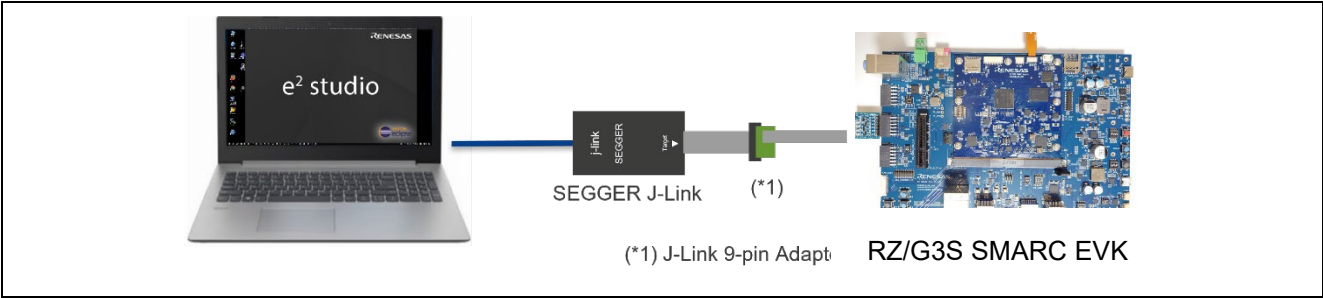


Figure 37. System Configuration Example – RZ/G3S SMARC EVK

3.2.1 Supported Debugger

- SEGGER J-Link

For details on SEGGER J-Link, please see [J-Link Debug Probes by SEGGER – the Embedded Experts](#).

3.2.2 Board Setup

3.2.2.1 Boot MODE

Set the boot mode using the two DIP SWITCHs shown in the figure below.

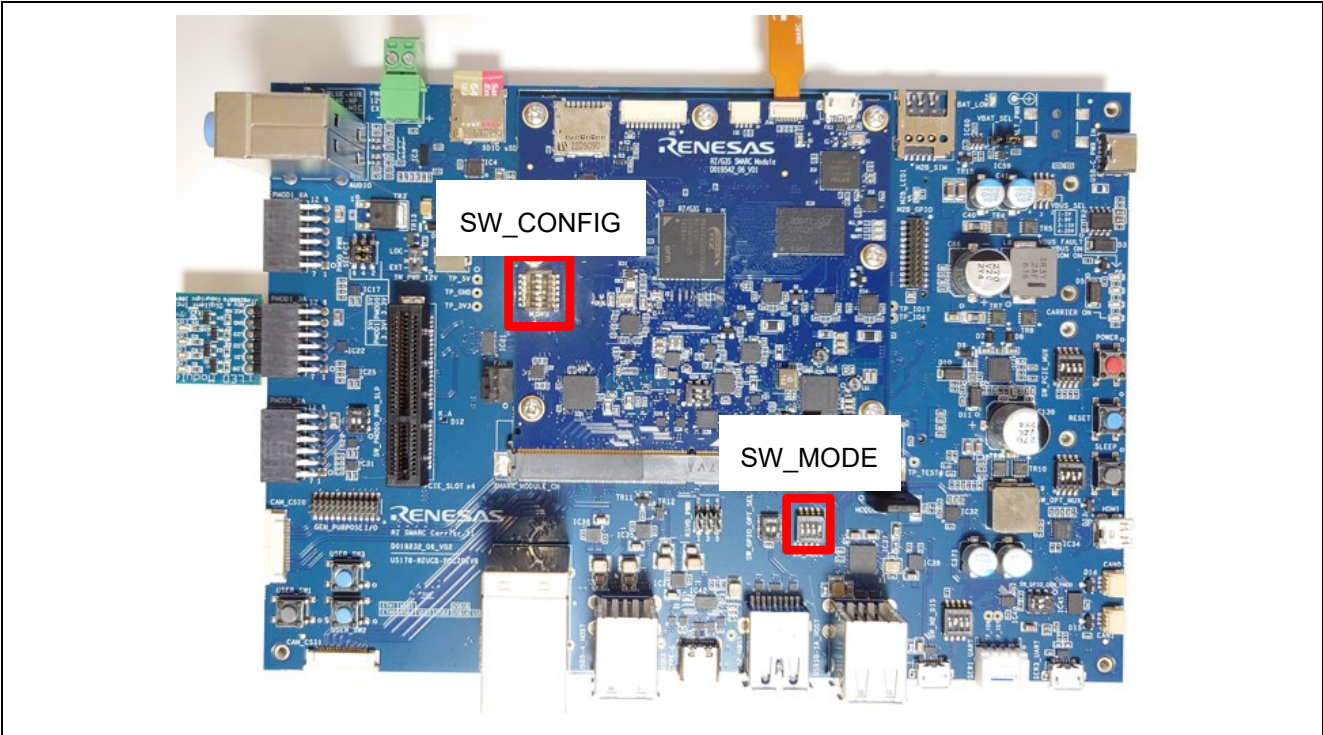


Figure 38. Boot MODE

In SW_CONFIG, select the boot CPU with the following settings.

1	2	3	4	5	6
OFF	OFF	ON	OFF	OFF	ON: CM33 boot OFF: CA55 boot

In SW_MODE, select the boot device with the following settings.

- Boot Mode 1: Booting from eMMC

1	2	3	4
ON	OFF	OFF	ON

- Boot Mode 2: Booting from serial flash memory

1	2	3	4
OFF	OFF	OFF	ON

- Boot Mode 3: Booting from the program downloaded through the serial communications with FIFO (SCIF)

1	2	3	4
OFF	ON	OFF	ON

3.2.2.2 JTAG connection

For the JTAG connection, connect the included “SMARC JTAG ADAPTOR” to the board.

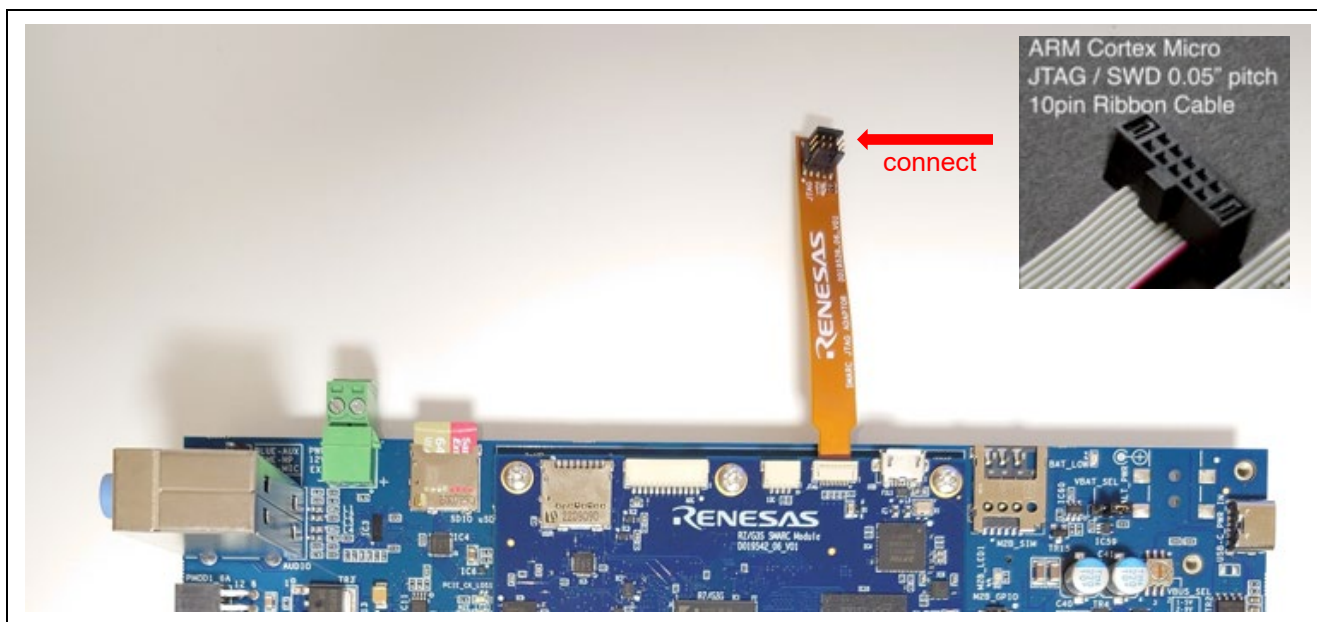


Figure 39. JTAG connection

Please note that RZ/G3S SMARC EVK has a CoreSight 10 connector and therefore, the following adapter is needed to connect Segger J-Link.

<https://www.segger.com/products/debug-probes/j-link/accessories/adapters/9-pin-cortex-m-adapter/>

3.2.2.3 Debug Serial (console output)

Debug serial uses SER3_UART (SCIFA ch0). The baud rate is 115200bps.

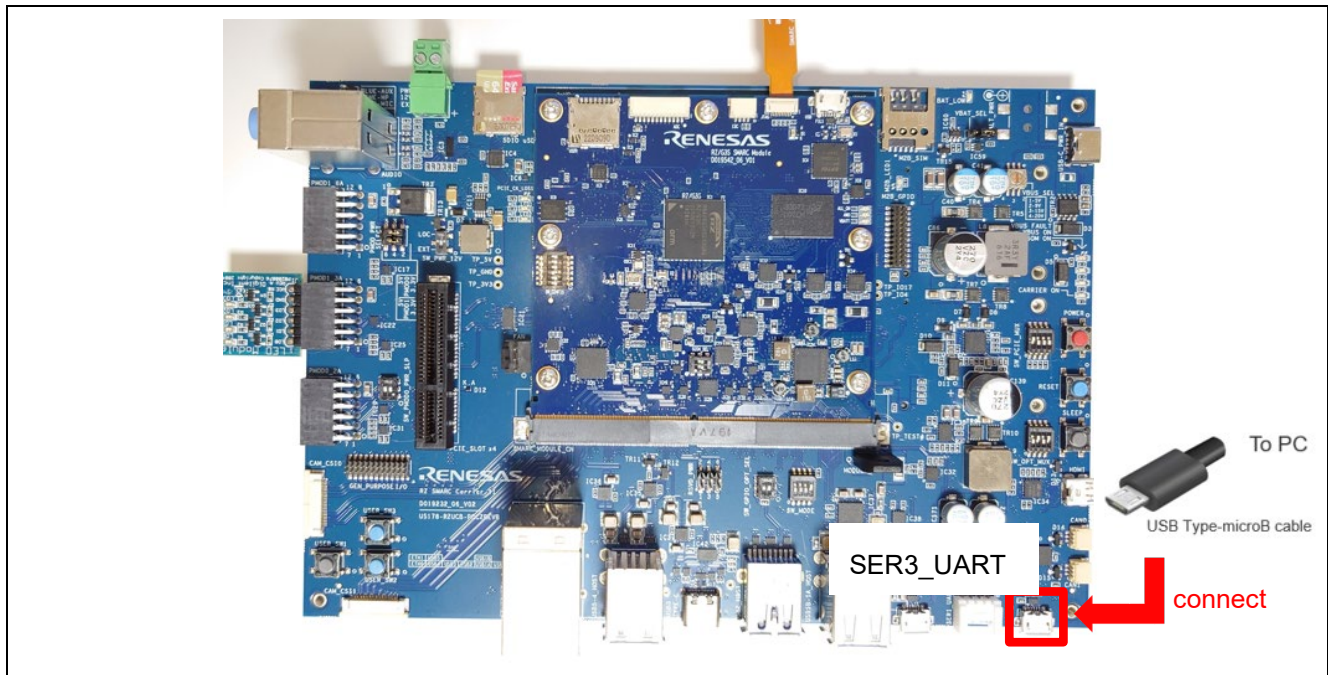


Figure 40. Debug Serial (console output)

Power Supply

Here are the power supply-related items to be used for Renesas development. Please prepare equivalent items for your development.

- USB Type-C cable CB-CD23BK (manufactured by Aukey)
- USB PD Charger Anker PowerPort III 65W Pod (manufactured by Anker)

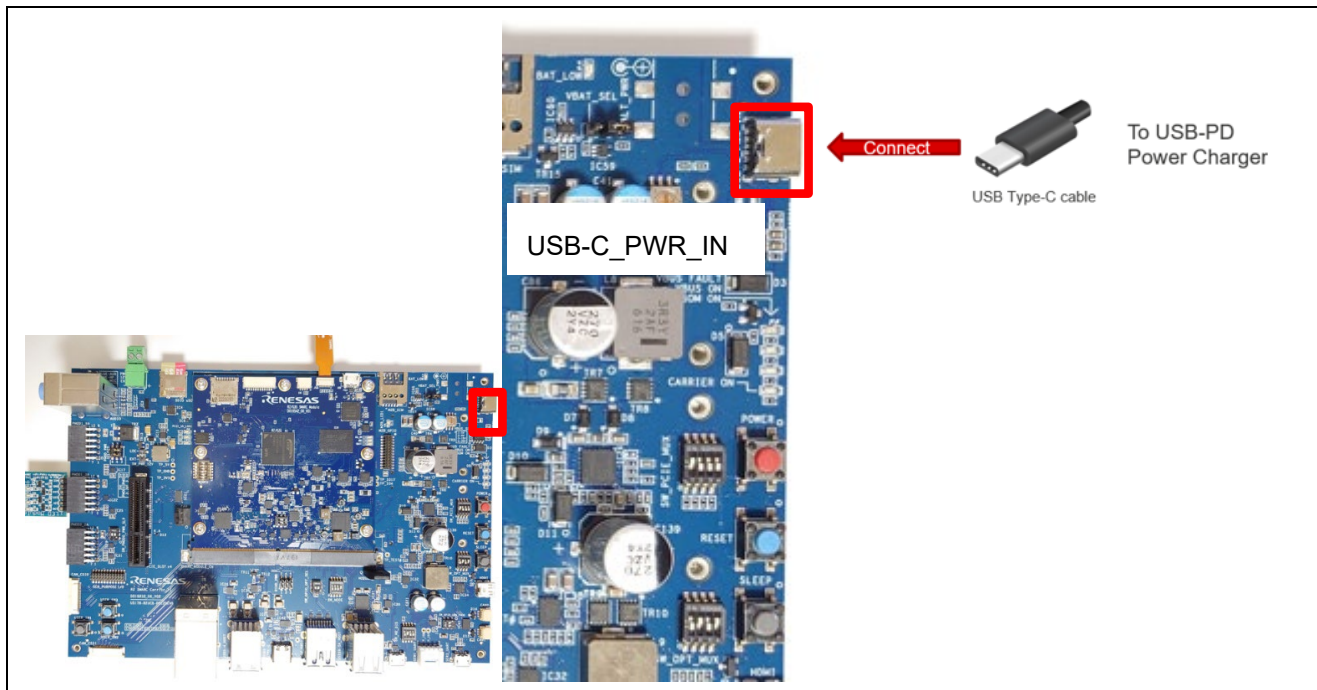


Figure 41. Power Supply

Connect the USB-PD Power Charger to the USB Type-C Connector. Then, VBUS ON and SOM ON light up. Press POWER to turn on the power. Then the CARRIER ON light up.

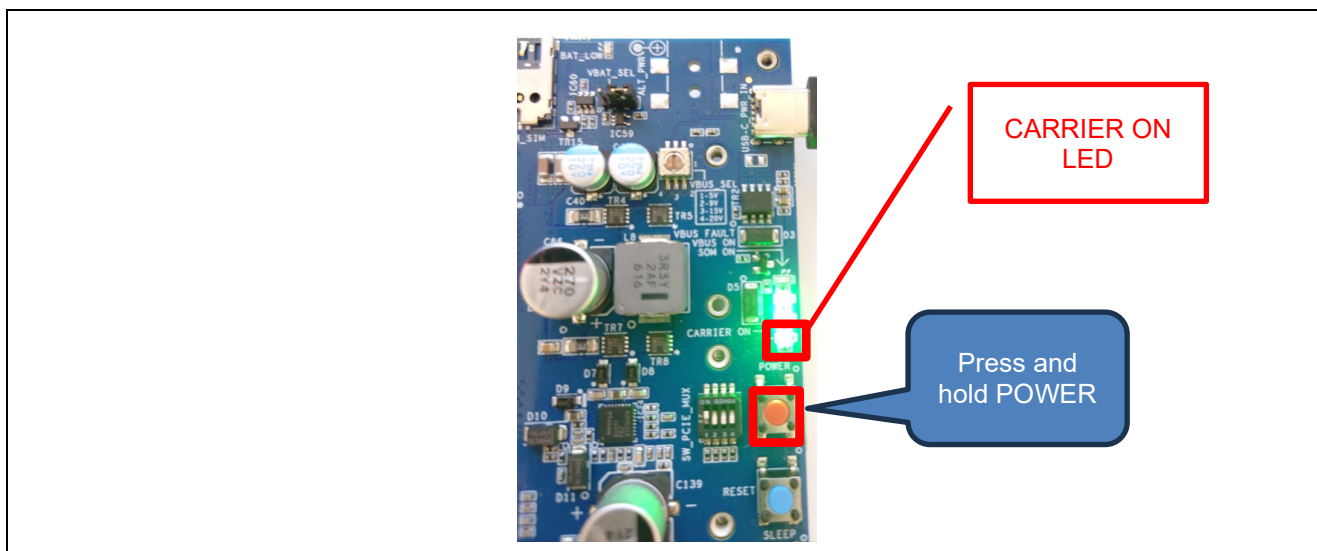


Figure 42. LED Status after Turning on EVK

3.2.2.5 How to Check the Operation of the Board

First, check the board for problems. There are three ways to do this. Please check with any of them.

BOOT MODE 1: Booting from eMMC

If U-Boot is written to the eMMC, when the power is turned on, the following will be output to the console (SER3_UART).

```

COM4 - Tera Term VT
File Edit Setup Control Window KanjiCode Help
NOTICE: BL2: v2.7(release):2.7.0/g3s_1.0.0_rc3
NOTICE: BL2: Built : 14:34:44, Nov  2 2023
NOTICE: BL2: Booting BL31
NOTICE: BL31: v2.7(release):2.7.0/g3s_1.0.0_rc3
NOTICE: BL31: Built : 14:34:44, Nov  2 2023

U-Boot 2021.10 (Oct 25 2023 - 08:58:16 +0000)

CPU:   Renesas Electronics CPU rev 1.0
Model: smarc-rzg3s
DRAM:  896 MiB
MMC:   sd@11c00000: 0, sd@11c10000: 1, sd@11c20000: 2
Loading Environment from MMC... OK
In:     serial@1004b800
Out:    serial@1004b800
Err:    serial@1004b800
Net:
Error: ethernet@11c30000 address not set.
No ethernet found.

Hit any key to stop autoboot:  0
Card did not respond to voltage select! : -110
Card did not respond to voltage select! : -110
Couldn't find partition mmc 1:1
Can't set block device
Card did not respond to voltage select! : -110
Couldn't find partition mmc 1:1
Can't set block device
Bad Linux ARM64 Image magic!
=> ^

```

Figure 43. RZ/G3S BOOT MODE 1: Booting from eMMC

BOOT MODE 2: Booting from serial flash memory

If U-Boot is written to the serial flash, when the power is turned on, the following will be output to the console (SER3_UART).

```

COM4 - Tera Term VT
File Edit Setup Control Window KanjiCode Help
NOTICE: BL2: v2.7(release):2.7.0/g3s_1.0.0_rc3
NOTICE: BL2: Built : 14:34:44, Nov  2 2023
NOTICE: BL2: Booting BL31
NOTICE: BL31: v2.7(release):2.7.0/g3s_1.0.0_rc3
NOTICE: BL31: Built : 14:34:44, Nov  2 2023

U-Boot 2021.10 (Oct 25 2023 - 08:58:16 +0000)

CPU:   Renesas Electronics CPU rev 1.0
Model: smarc-rzg3s
DRAM:  896 MiB
MMC:   sd@11c00000: 0, sd@11c10000: 1, sd@11c20000: 2
Loading Environment from MMC... OK
In:     serial@1004b800
Out:    serial@1004b800
Err:    serial@1004b800
Net:
Error: ethernet@11c30000 address not set.
No ethernet found.

Hit any key to stop autoboot:  0
Card did not respond to voltage select! : -110
Card did not respond to voltage select! : -110
Couldn't find partition mmc 1:1
Can't set block device
Card did not respond to voltage select! : -110
Couldn't find partition mmc 1:1
Can't set block device
Bad Linux ARM64 Image magic!
=> ^

```

Figure 44. RZ/G3S BOOT MODE 2: Booting from serial flash memory

BOOT MODE 3: Booting from the program downloaded through the serial communications with FIFO (SCIF)

When the power is turned on, the following will be output to the console (SER3_UART).

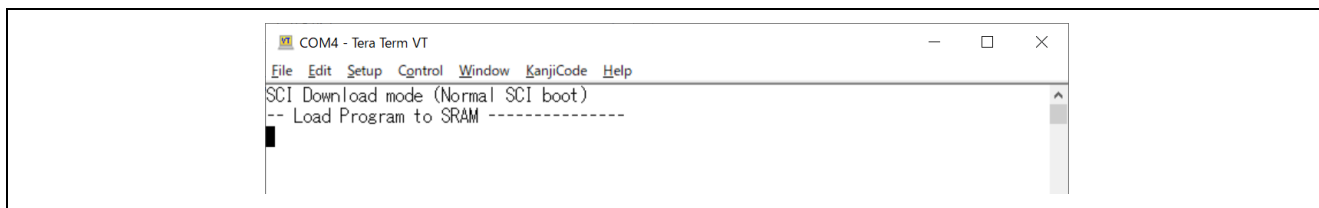


Figure 45. RZ/G3S BOOT MODE 3: Booting from the program downloaded through SCIF

3.3 RZ/G3E SMARC EVK

Below is an example of a typical system configuration.

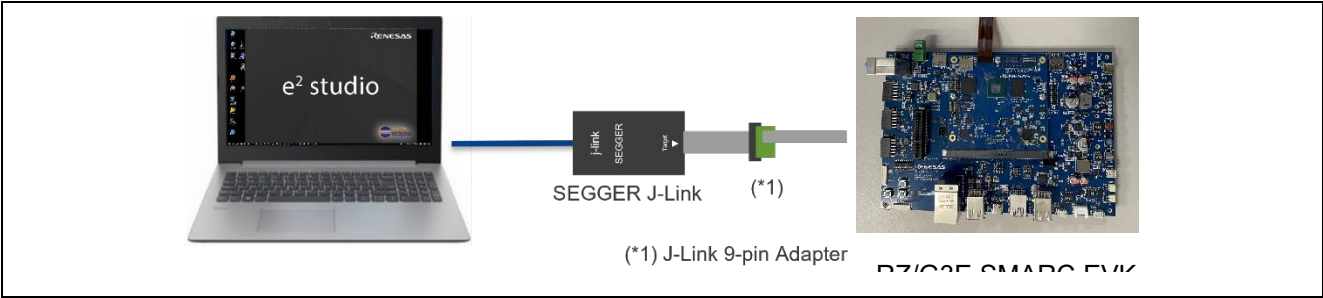


Figure 46. System Configuration Example – RZ/G3E SMARC EVK

3.3.1 Supported Debugger

- SEGGER J-Link

For details on SEGGER J-Link, please see [J-Link Debug Probes by SEGGER – the Embedded Experts](#).

3.3.2 Board Setup

3.3.2.1 Boot MODE

Set the boot mode using the two DIP SWITCHs shown in the figure below.

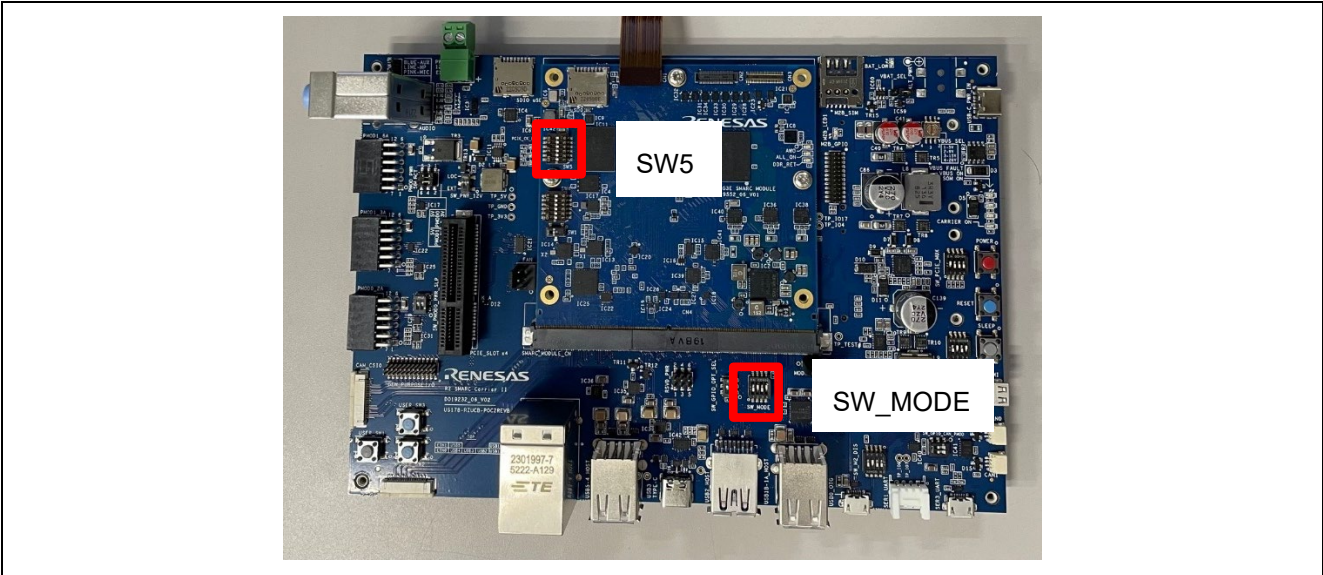


Figure 47. Boot MODE

In SW5, select the boot CPU with the following settings.

1	2	3	4	5	6
OFF	ON: CM33 boot OFF: CA55 boot	ON	OFF	OFF	OFF

In SW_MODE, select the boot device with the following settings.

- Boot Mode 3: Booting from SCIF download

1	2	3
OFF	ON	OFF

- Boot Mode 4: Booting from USB download

1	2	3
ON	ON	ON

- Boot Mode 5: Booting from eMMC 1.8 V

1	2	3
ON	OFF	OFF

- Boot Mode 6: Booting from a serial flash memory connected to the xSPI bus space 1.8 V

1	2	3
OFF	ON	OFF

3.3.2.2 JTAG connection

For the JTAG connection, connect the included “Breakout board” to the board.

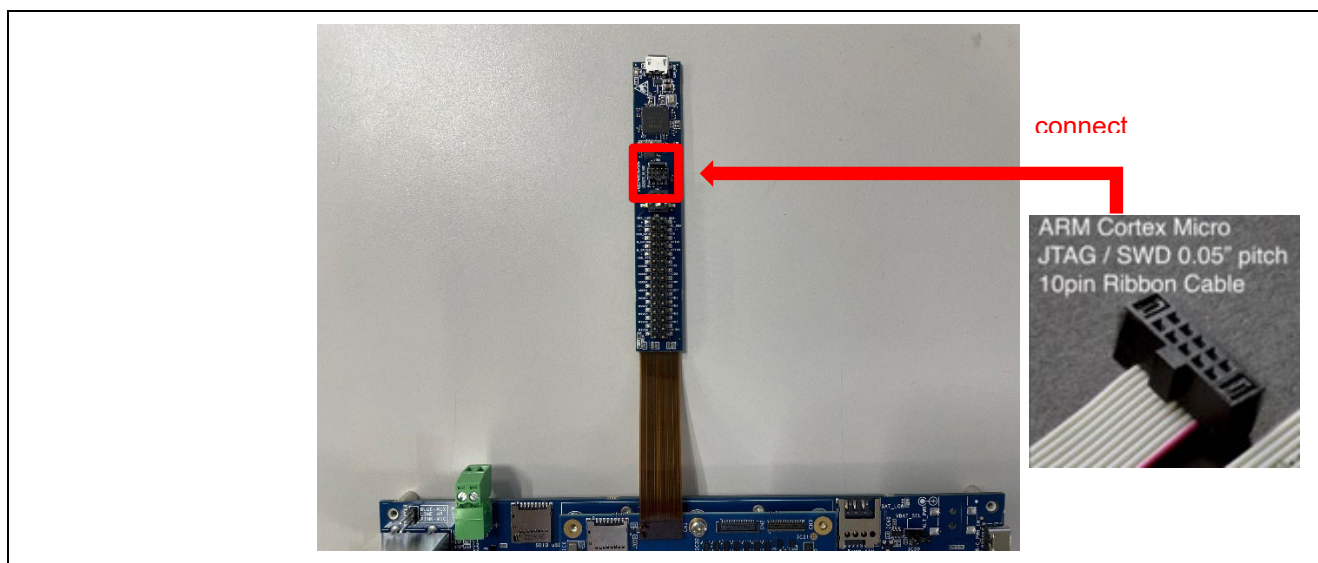


Figure 48. JTAG connection

Note 1: RZ/G3E SMARC EVK has a CoreSight 10 connector.

Therefore, the following adapter must be used to connect to the Segger J-Link.

<https://www.segger.com/products/debug-probes/j-link/accessories/adapters/9-pin-cortex-m-adapter/>

Note 2: It is strongly recommended that you do not detach the breakout board once it is connected to the CN1 connector on the module board.

3.3.2.3 Debug Serial (console output)

Debug serial uses Debug_UART (SCIFA ch0). The baud rate is 115200bps.

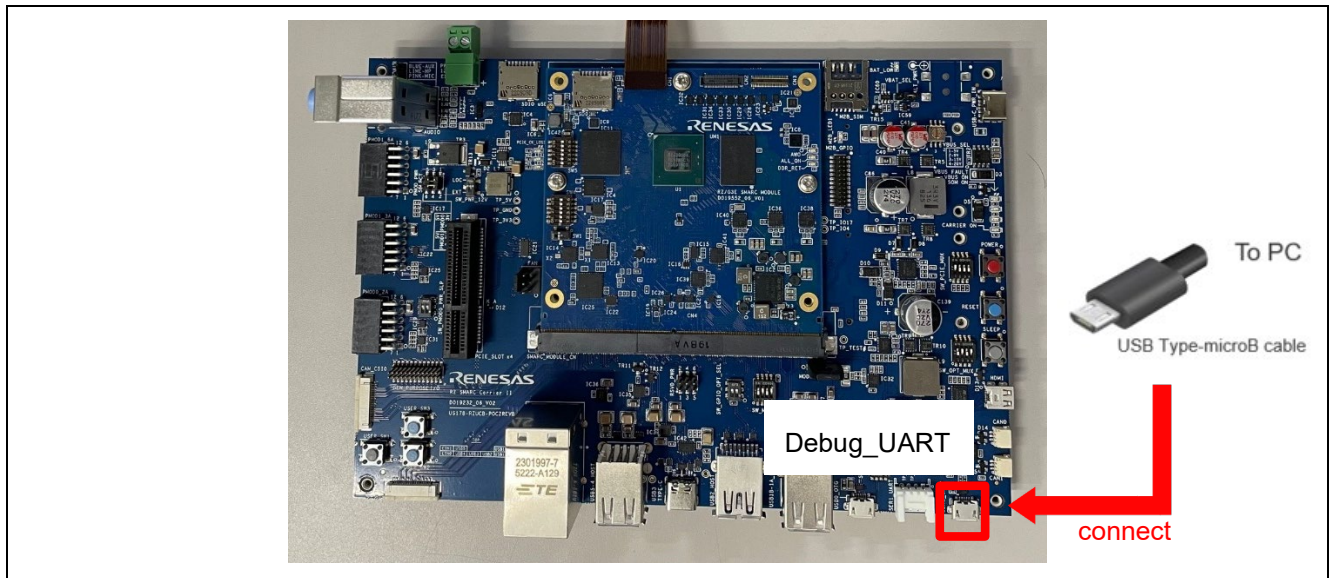


Figure 49. Debug Serial (console output)

Power Supply

Here are the power supply-related items to be used for Renesas development. Please prepare equivalent items for your development.

- USB Type-C cable CB-CD23BK (manufactured by Aukey)
- USB PD Charger Anker PowerPort III 65W Pod (manufactured by Anker)

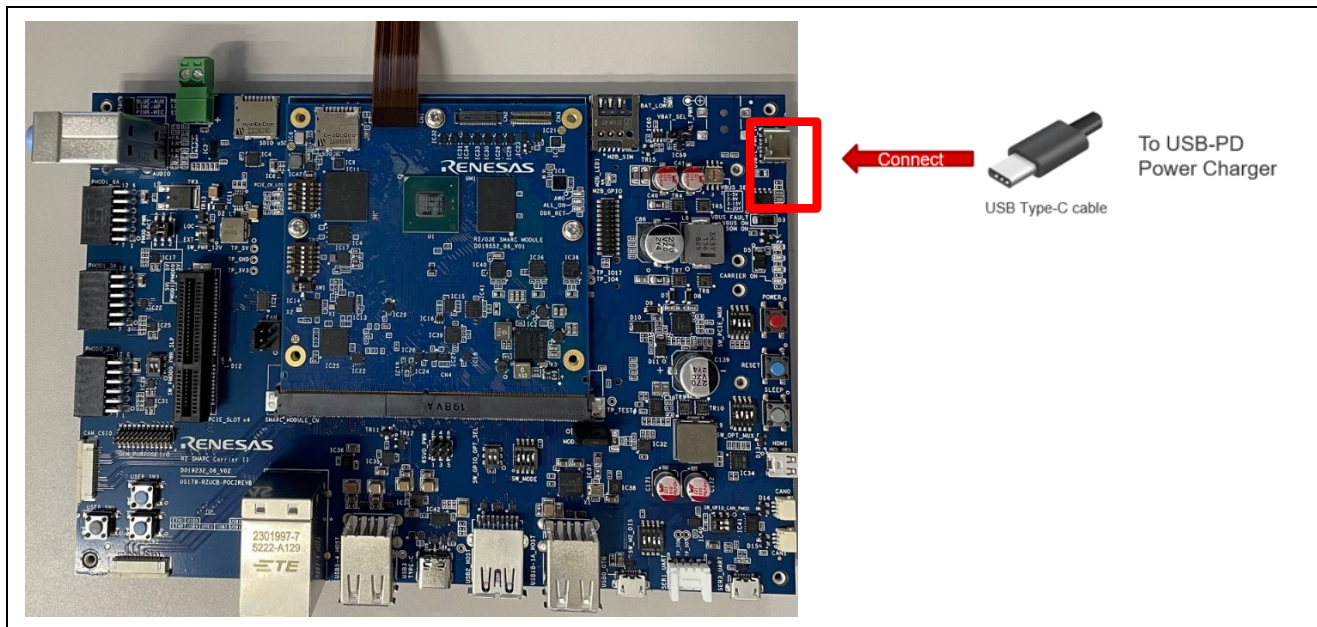


Figure 50. Power Supply

Connect the USB-PD Power Charger to the USB Type-C Connector. Then, VBUS ON and SOM ON light up. Press POWER to turn on the power. Then the CARRIER ON light up.

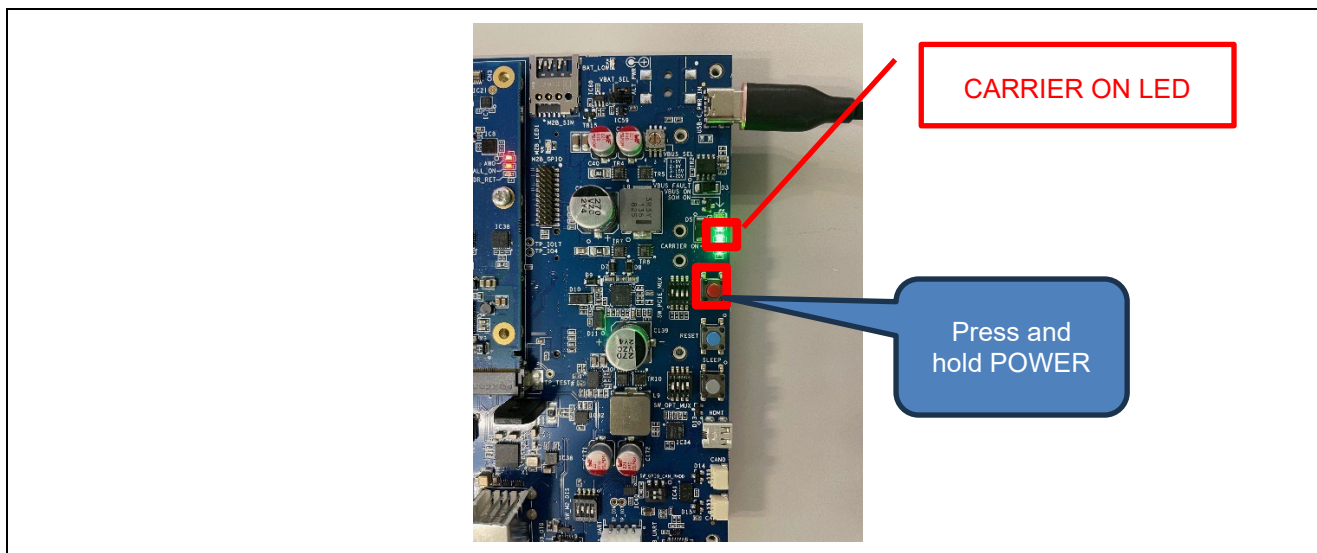


Figure 51. LED Status after Turning on EVK

3.3.2.5 How to Check the Operation of the Board

First, check the board for problems.

BOOT MODE 3: Booting from the program downloaded through the serial communications with FIFO (SCIF)

When the power is turned on, the following will be output to the console (SER3_UART).

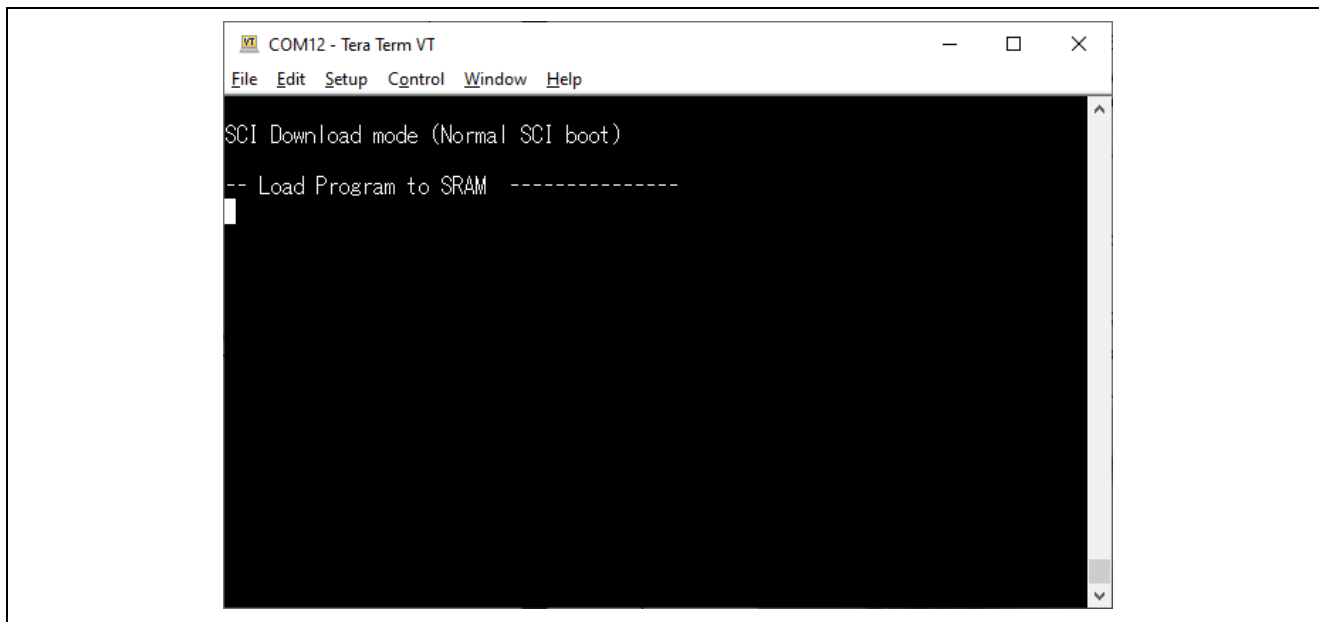


Figure 52. RZ/G3E BOOT MODE 3: Booting from the program downloaded through SCIF

3.4 RZ/G3L SMARC EVK

Below is an example of a typical system configuration.

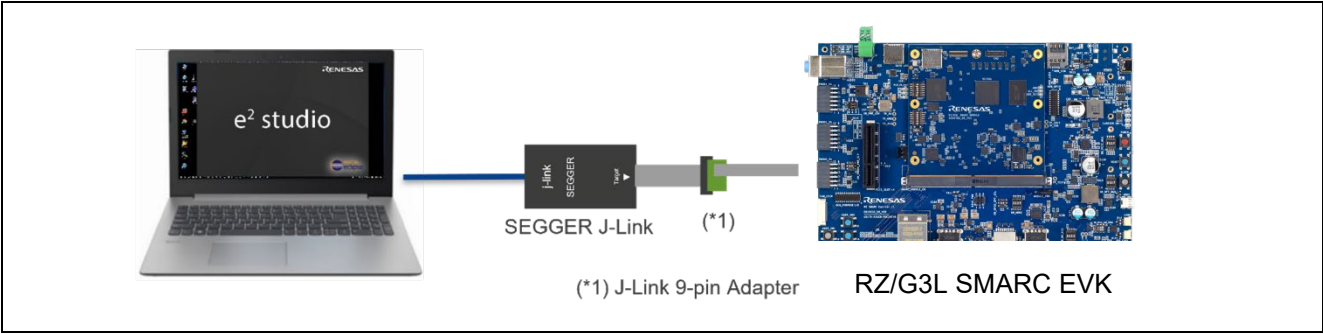


Figure 53. System Configuration Example – RZ/G3L SMARC EVK

3.4.1 Supported Debugger

- SEGGER J-Link

For details on SEGGER J-Link, please see [J-Link Debug Probes by SEGGER – the Embedded Experts](#).

3.4.2 Board Setup

3.4.2.1 Boot MODE

Set the boot mode using the two DIP SWITCHS shown in the figure below.

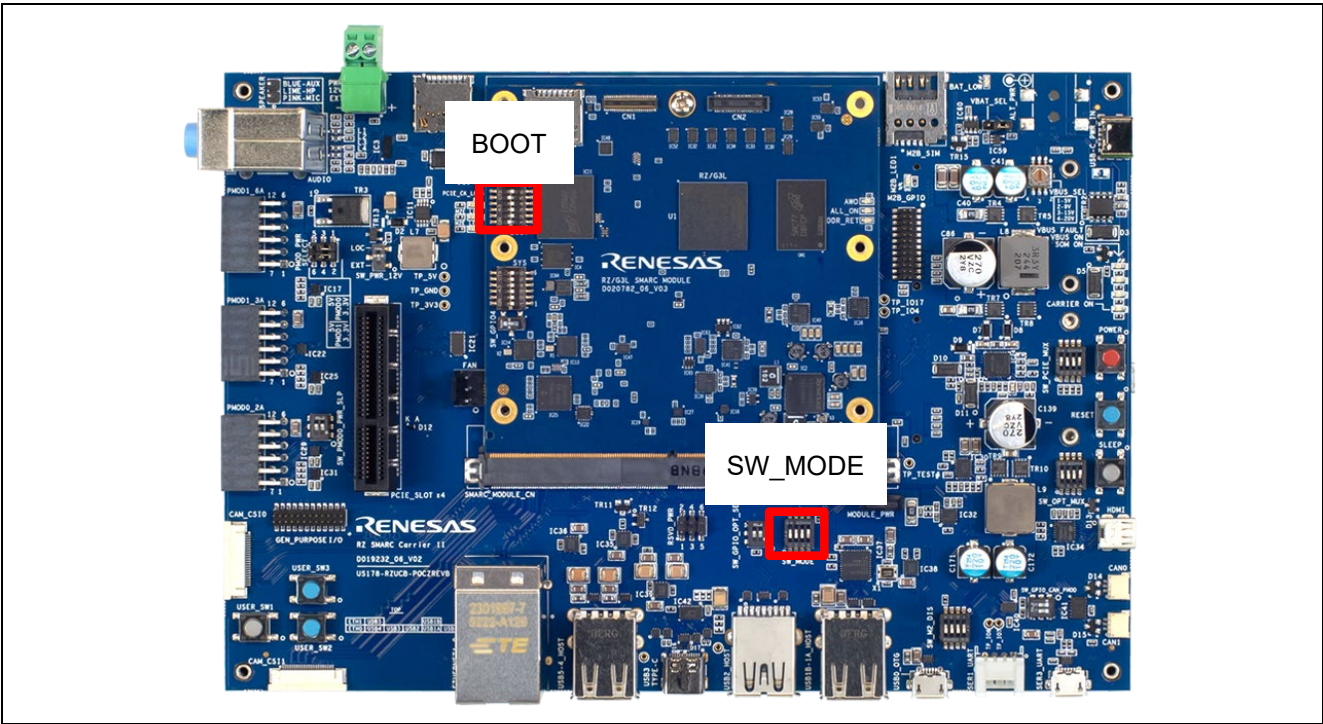


Figure 54. Boot MODE

In the BOOT switch, select the boot CPU with the following settings.

1	2	3	4	5	6
OFF	ON: CM33 boot OFF: CA55 boot	OFF	OFF	OFF	OFF

In SW_MODE, select the boot device with the following settings.

- Boot Mode 3: Booting from SCIF download

1	2	3	4
OFF	ON	OFF	ON

- Boot Mode 4: Booting from USB download

1	2	3	4
ON	ON	ON	ON

- Boot Mode 5: Booting from eMMC 1.8V

1	2	3	4
ON	OFF	OFF	ON

- Boot Mode 6: Booting from serial flash memory connected to the xSPI bus space 1.8 V

1	2	3	4
OFF	OFF	OFF	ON

3.4.2.2 JTAG connection

For the JTAG connection, connect the included “Breakout board” to the board.

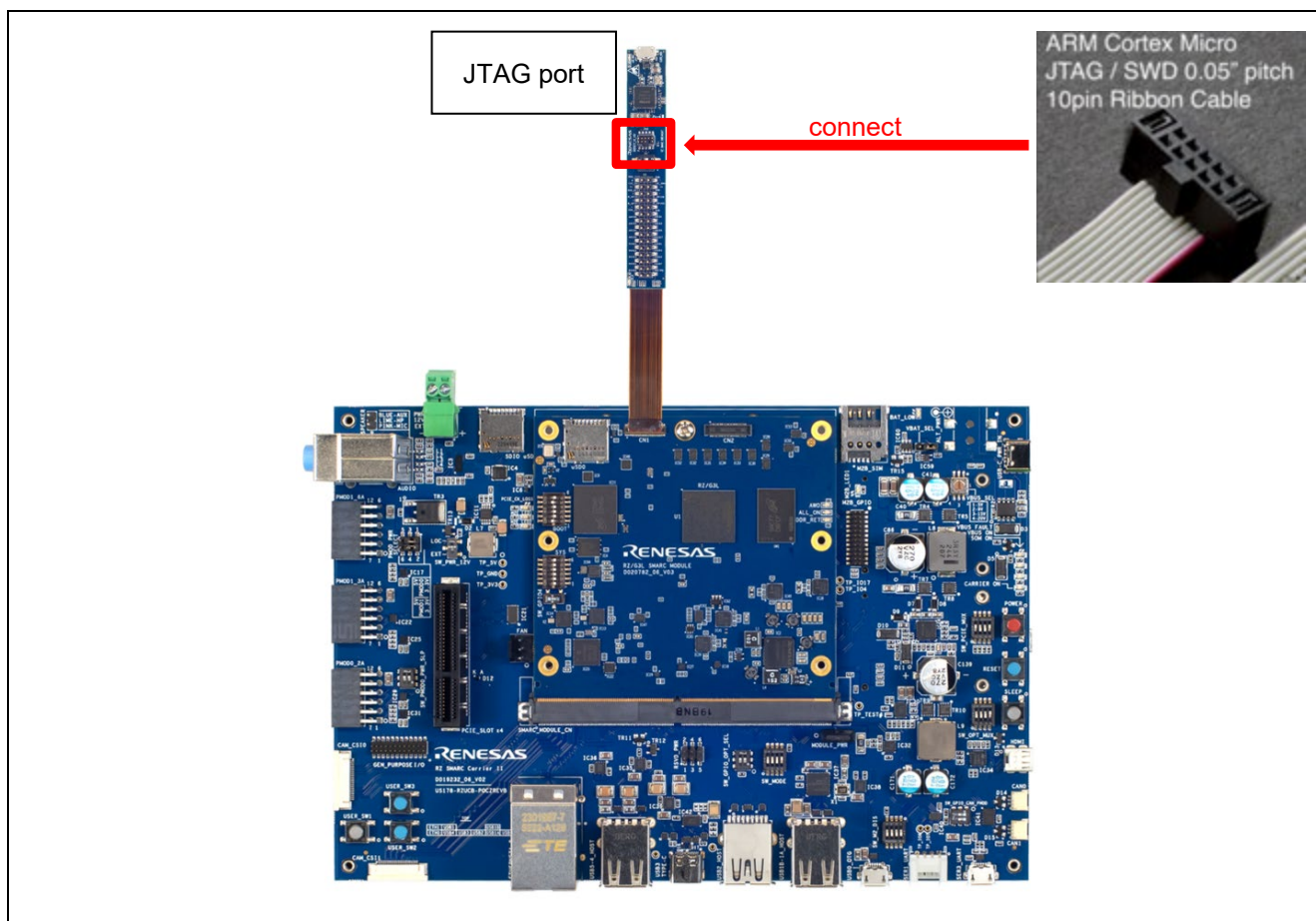


Figure 55. JTAG connection

Note 1: RZ/G3L SMARC EVK has a CoreSight 10 connector. Therefore, the following adapter must be used to connect to the Segger J-Link.

<https://www.segger.com/products/debug-probes/j-link/accessories/adapters/9-pin-cortex-m-adapter/>

Note 2: It is strongly recommended that you do not detach the breakout board once it is connected to the CN1 connector on the module board.

3.4.2.3 Debug Serial (console output)

Debug serial uses SER3_UART (SCIFA ch0). The baud rate is 115200bps.

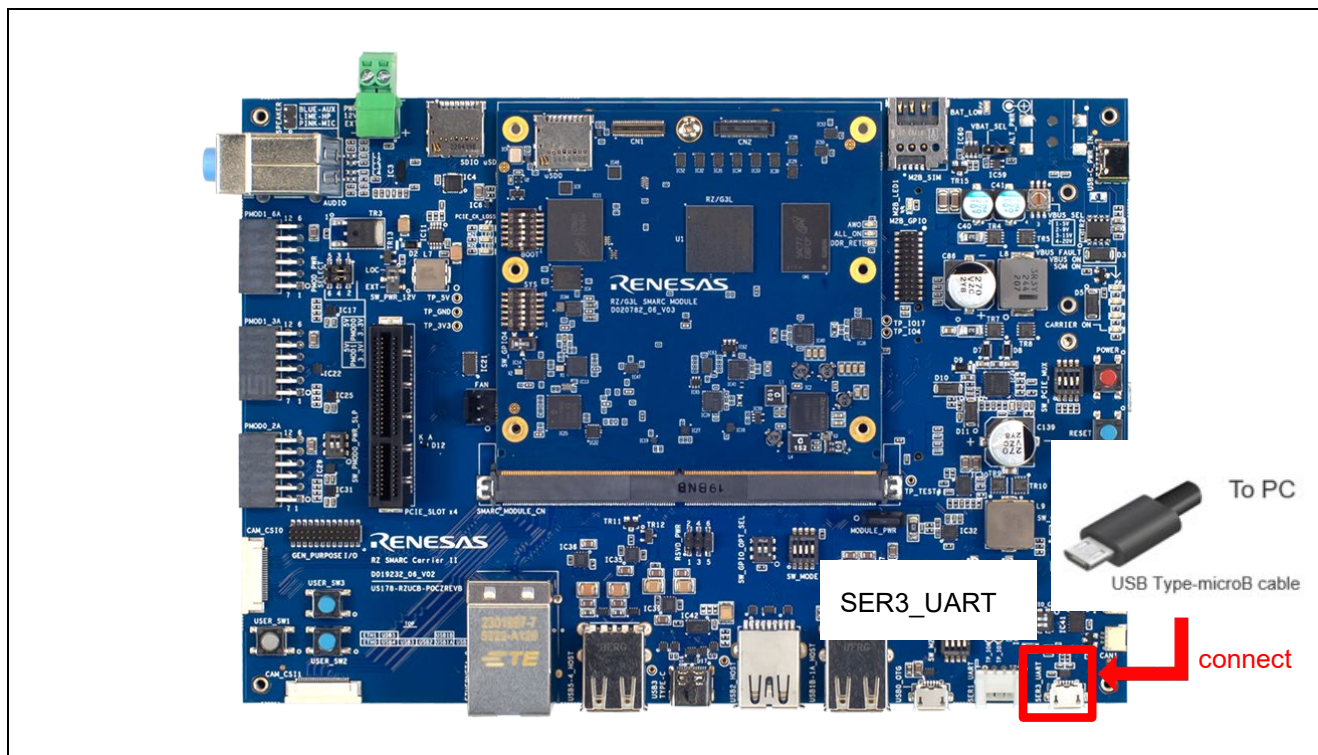


Figure 56. Debug Serial (console output)

3.4.2.4 Power Supply

Here are the power supply-related items to be used for Renesas development. Please prepare equivalent items for your development.

- USB Type-C cable CB-CD23BK (manufactured by Aukey)
- USB PD Charger Anker PowerPort III 65W Pod (manufactured by Anker)

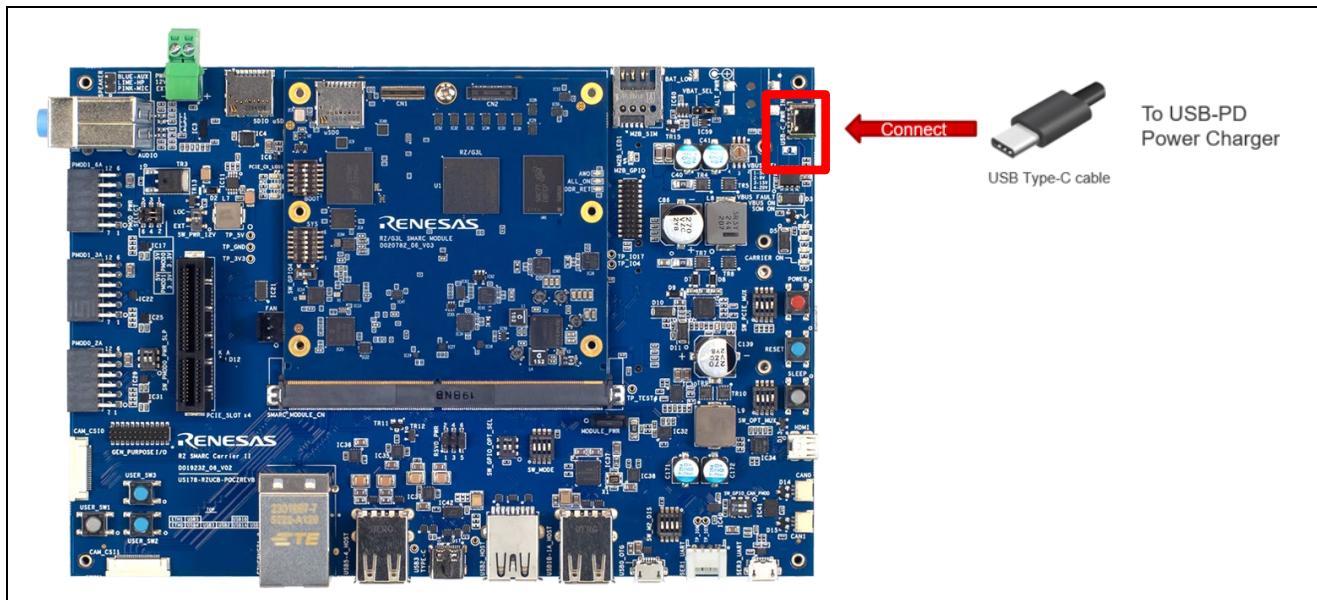


Figure 57. Power Supply

Connect the USB-PD Power Charger to the USB Type-C Connector. Then, VBUS ON and SOM ON light up. Press and hold the POWER button for up to 3 seconds to power on the board. Then the CARRIER ON lights up.

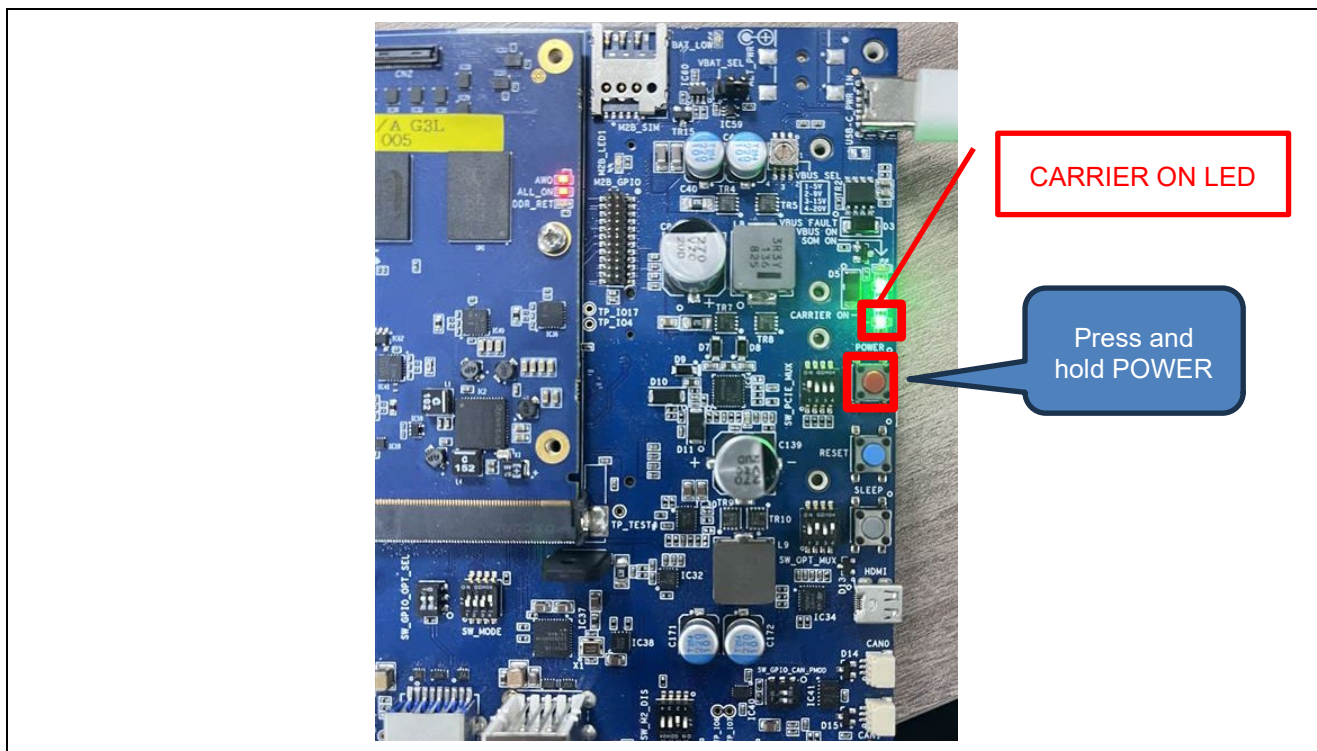


Figure 58. LED Status after Turning on EVK

3.4.2.5 How to Check the Operation of the Board

Before starting development or debugging, verify that the board is operating correctly. This check confirms that the board can boot successfully and that the serial console communication is functioning properly.

The board can be verified using either of the following boot modes:

BOOT MODE 3: Booting from the program downloaded through the serial communications with FIFO (SCIF)

When the power is turned on, the following will be output to the console (SER3_UART).

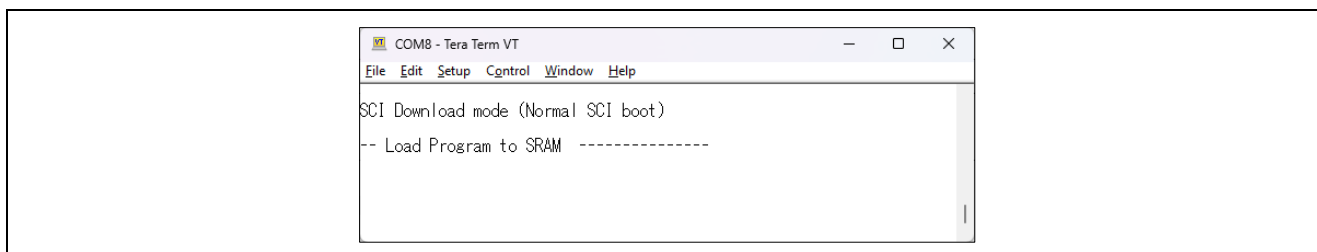


Figure 59. RZ/G3L BOOT MODE 3: Booting from the program downloaded through SCIF

BOOT MODE 5: Booting from eMMC 1.8V

If U-Boot is written to the eMMC, the following messages are displayed on the console (SER3_UART) when the power is turned on. The appearance of the U-Boot log indicates that the board is operating correctly. Some error messages may be displayed in the console output. These messages are expected and can be ignored because the flash memory is empty by default.

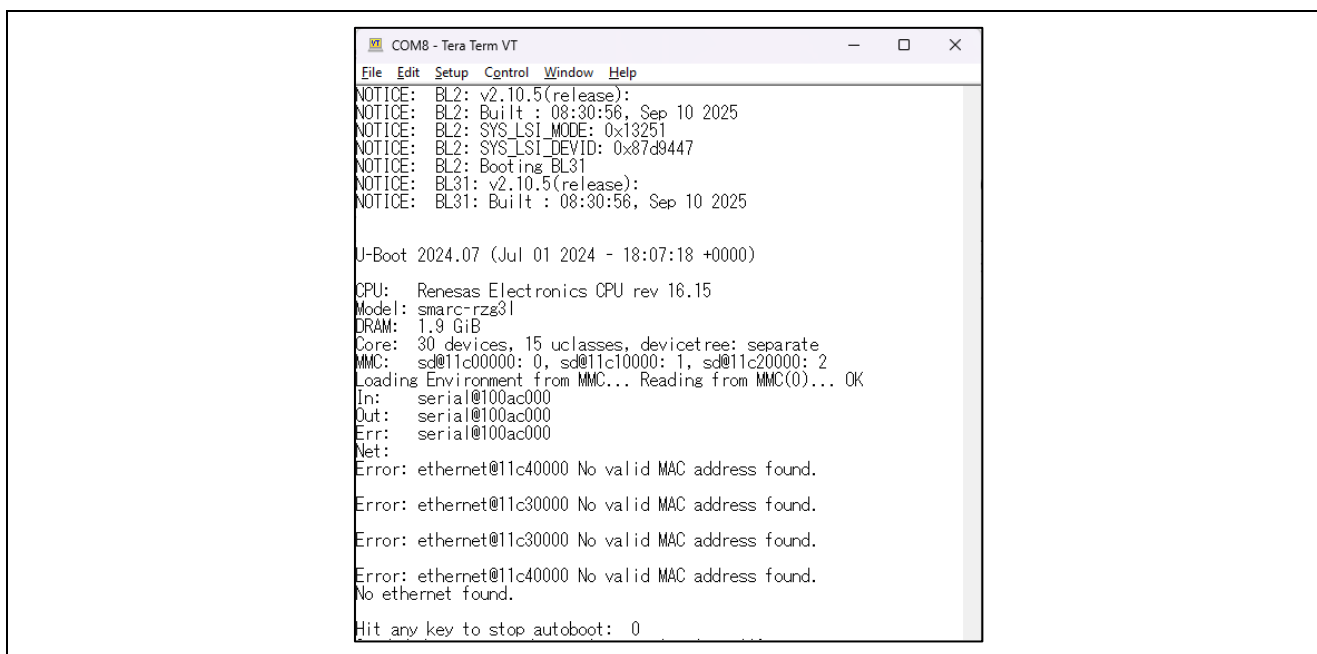


Figure 60. RZ/G3L BOOT MODE 5: Booting from eMMC 1.8V

4. Tutorial: Your First RZ MPU Project - Blinky

4.1 Tutorial Blinky

The goal of this tutorial is to quickly get acquainted with the Flexible Software Package by moving through the steps of creating a simple application using e² studio and running that application on an RZ MPU board.

4.2 What Does Blinky Do?

The application used in this tutorial is Blinky, traditionally the first program run in a new embedded development environment.

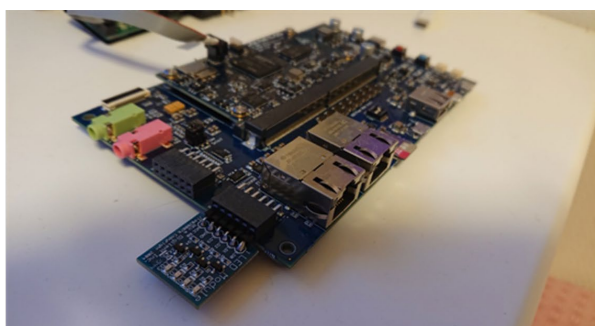
Blinky is the "Hello World" of microprocessors. If the LED blinks, you know that:

- The toolchain is set up correctly and builds a working executable image for your chip.
- The debugger has been installed with working drivers and is properly connected to the board.
- The board is powered up, and its jumper and switch settings are probably correct.
- The microprocessor is alive, the clocks are running, and the memory is initialized.
- Timer (GTM) interrupt is intentionally fired, and GPIO is properly controlled.

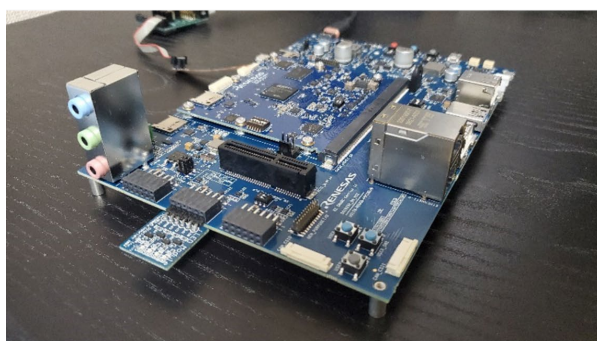
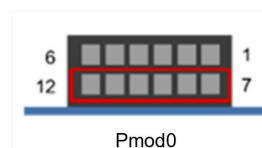
Note: The SMARC EVK board does not have any LEDs. Thus, the Blinky sample application used in this tutorial is designed to use the Pmod module described below, alternatively:

- Pmod LED (Four High-brightness LEDs): <https://reference.digilentinc.com/pmod/pmodled/start>

This module is not included on the SMARC EVK board, and so, please prepare it beforehand.



RZ/G2L SMARC EVK



RZ/G3S SMARC EVK

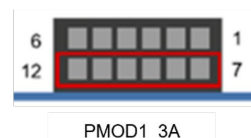


Figure 61. Connection Pmod LED module to RZ/G2L or RZ/G3S

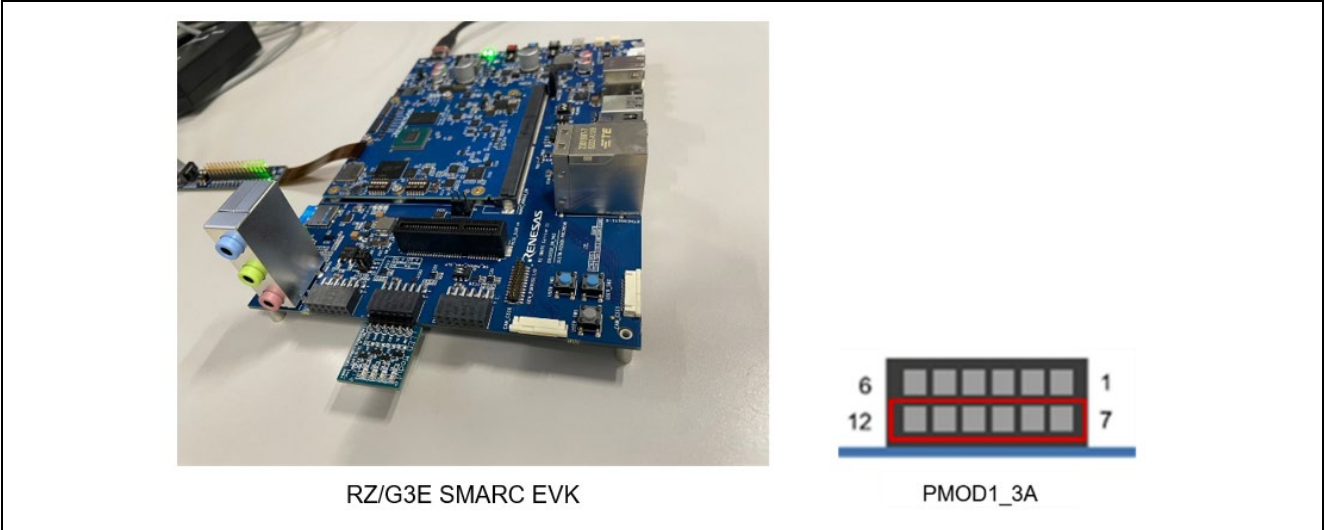


Figure 62. Connection Pmod LED module to RZ/G3E

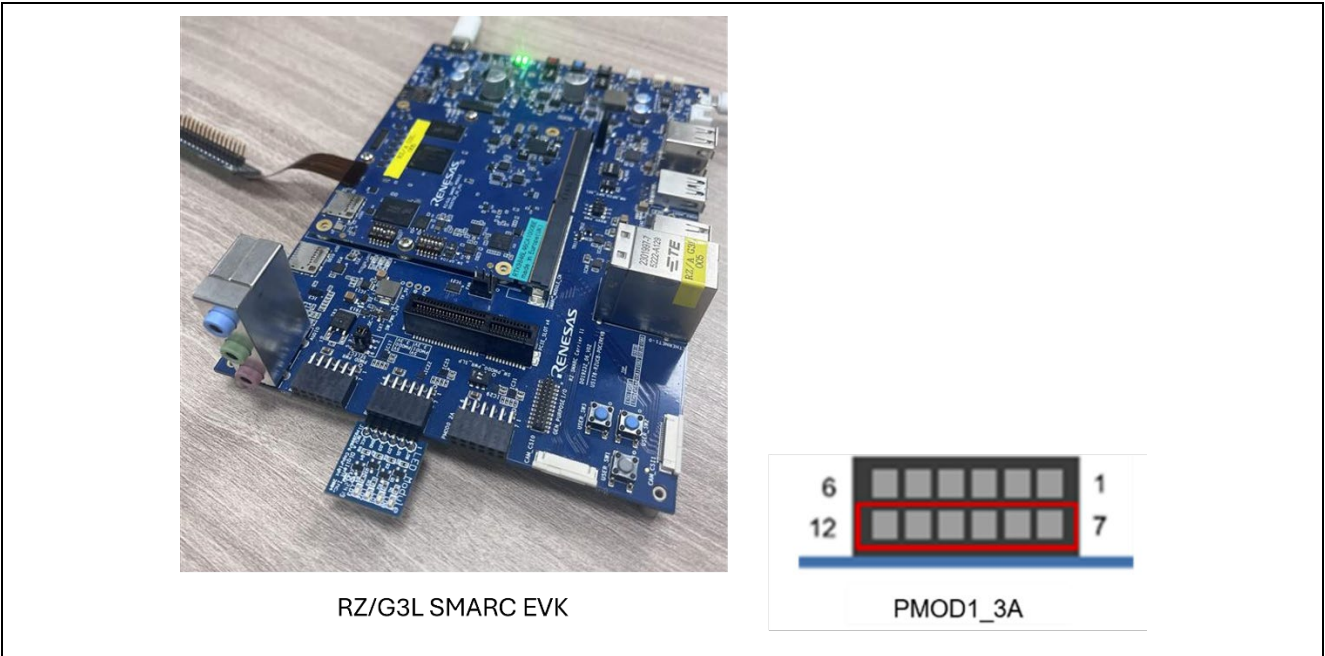


Figure 63. Connection Pmod LED module to RZ/G3L

4.3 Create a New Project for Blinky

The creation and configuration of an RZ C/C++ FSP Project is the first step in the creation of an application. The base RZ pack for RZG devices includes a pre-written Blinky example application.

Follow these steps to create an RZ MPU project:

1. In e² studio, click File > New > C/C++ Project.

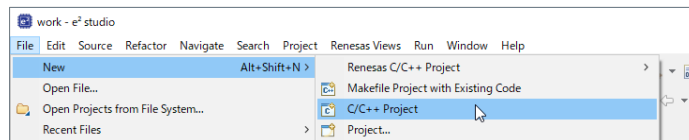


Figure 64. New C/C++ Project

2. Select [Renesas RZ] > [Renesas RZ C/C++ FSP Project] and click the [Next >] button.

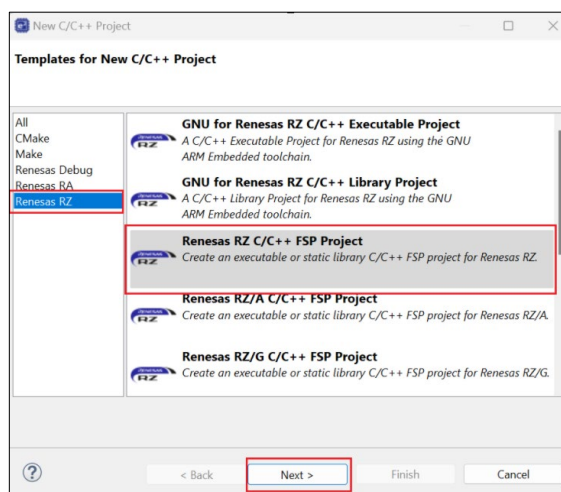


Figure 65. Renesas RZ C/C++ FSP Project

3. Assign a name for this new project. Blinky is a good name to use for this tutorial.

- Click the **[Next >]** button. The **Project Configuration** window shows your selection.

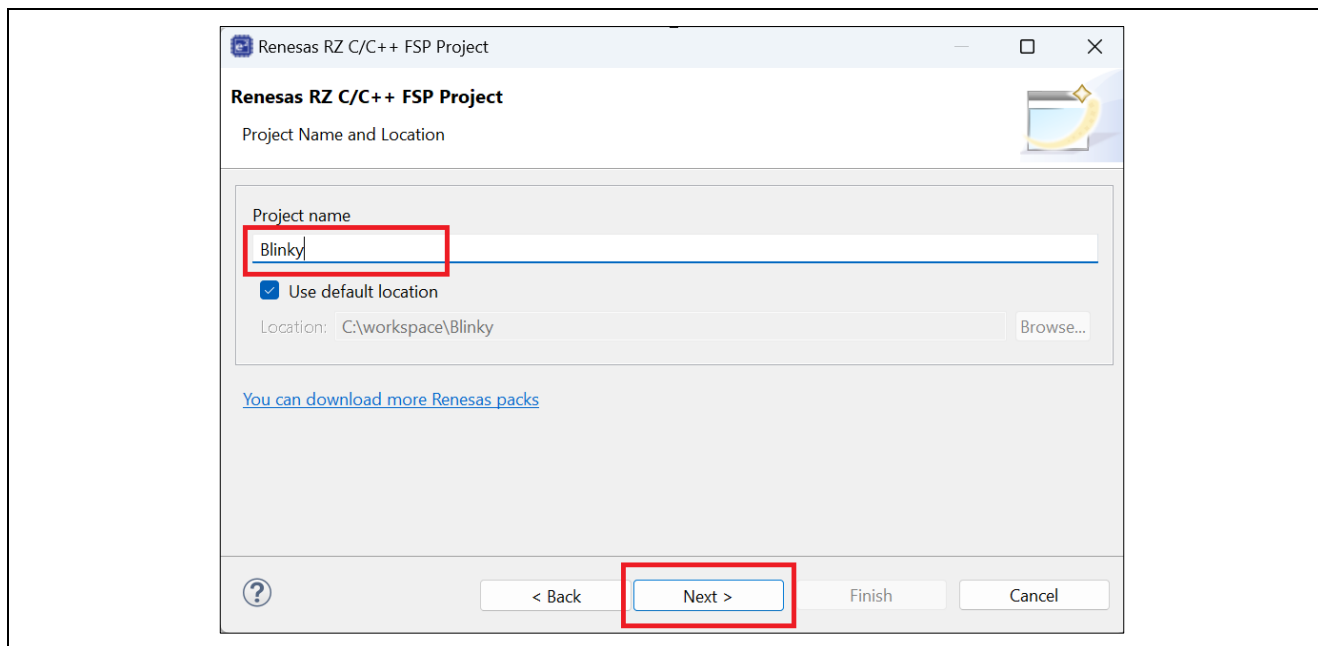


Figure 66. e² studio Project Configuration window (part 1)

- Select the board support package by selecting the name of your board from the Device Selection drop-down list. Select **GNU ARM Embedded** in Toolchains, and the version is **13.3.1 arm-13-24**, and click the **[Next >]** button.

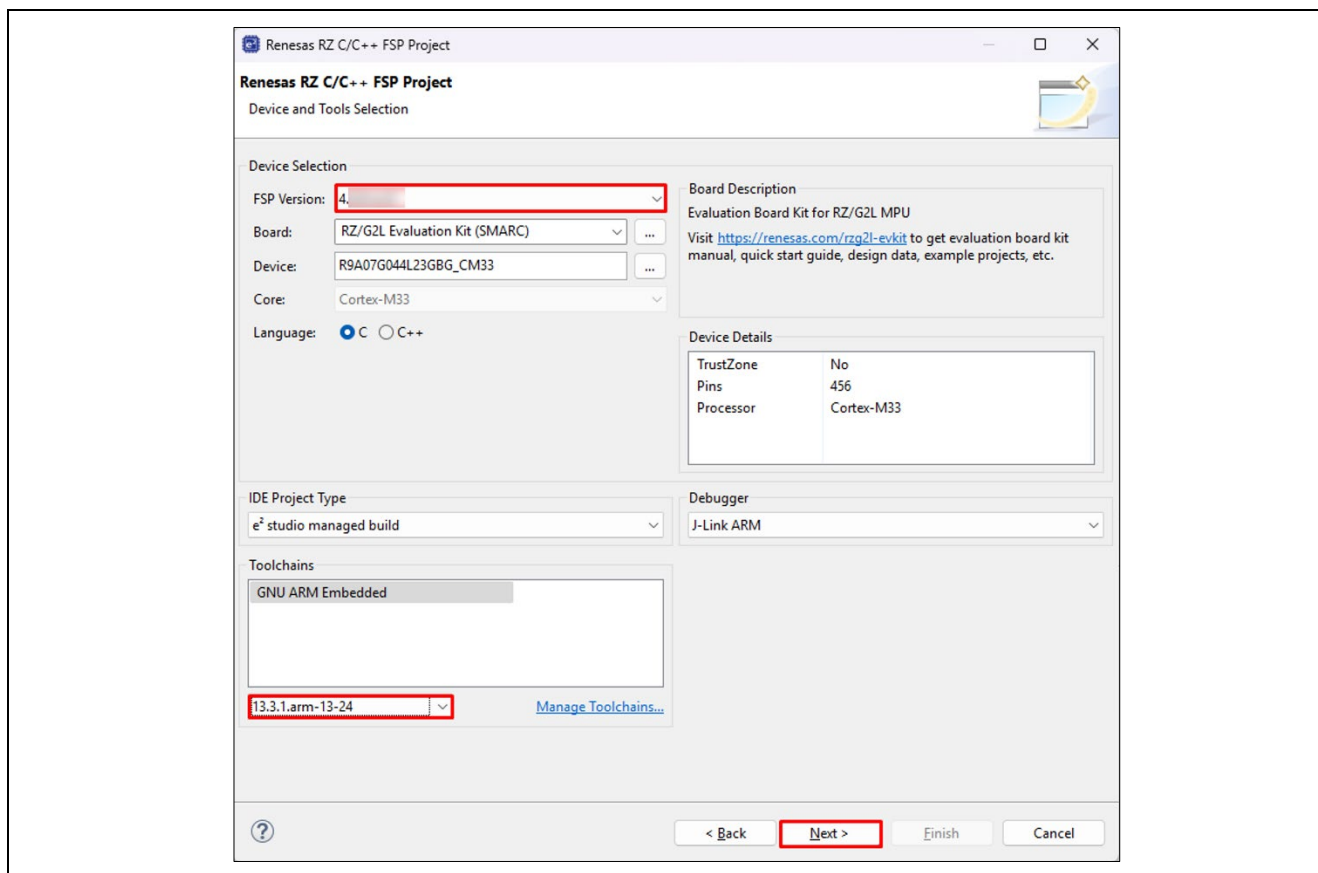


Figure 67. e² studio Project Configuration window (part 2)

6. (Optional) When creating an RZ/G3E or RZ/G3L project, support for CM33 cold boot is also available. For further information, refer to the [RZ/G Multi-OS Package](#) documentation.

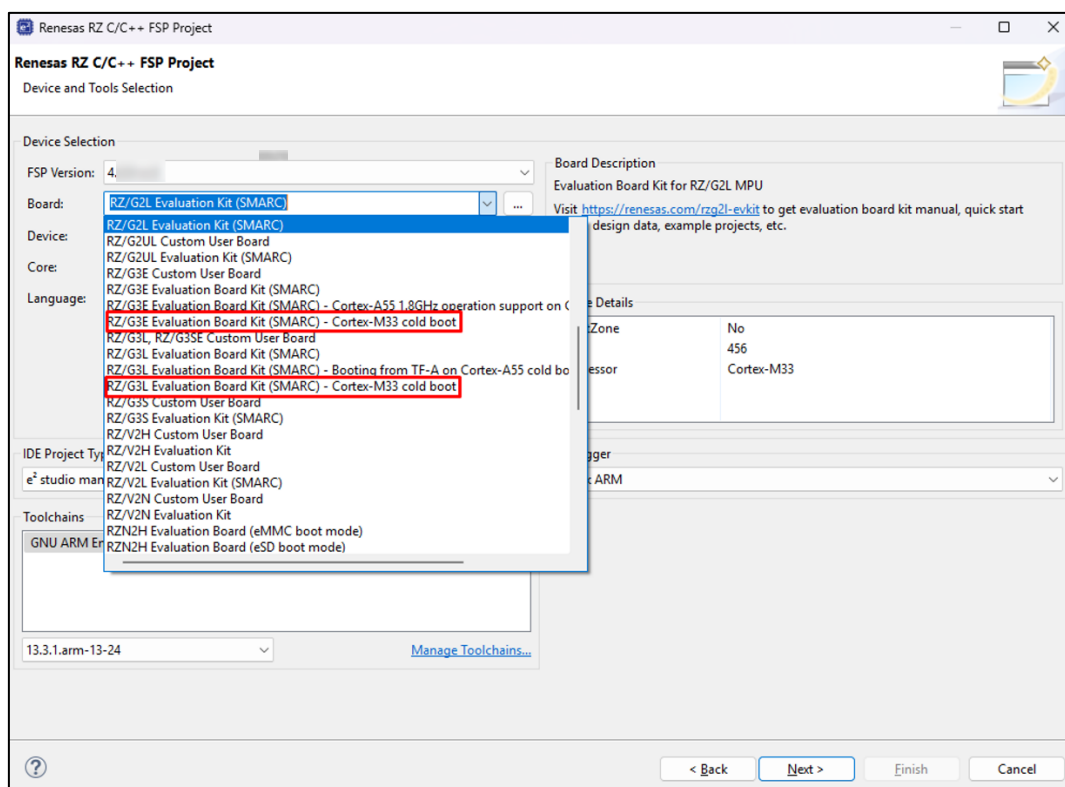


Figure 68. e² studio Project Configuration window (part 3)

7. (Optional) When creating an RZ/G Multi-Core project, choose the right bundled project as the **Preceding Project**, and click the **[Next >]** button.

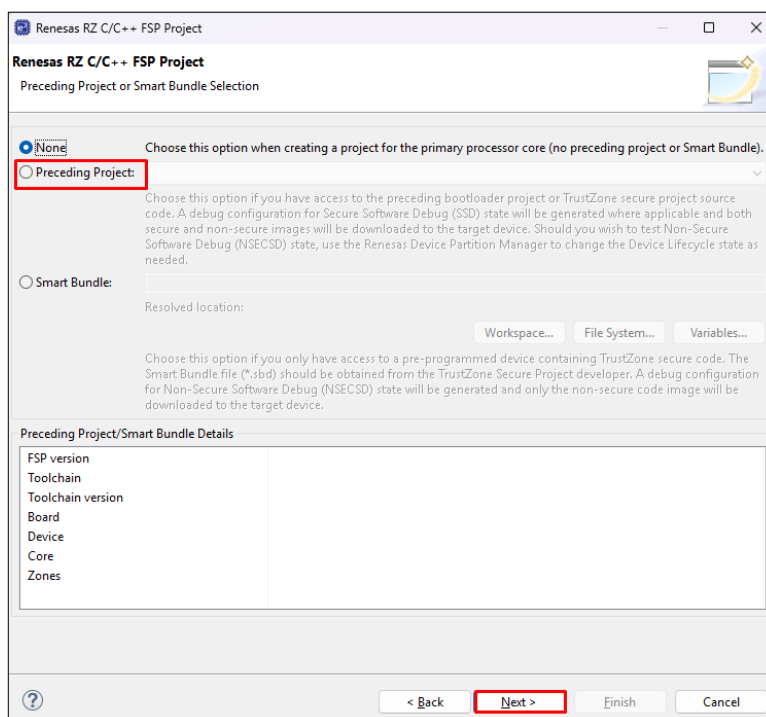


Figure 69. e² studio Project Configuration window (part 4)

8. Select the build artifact and RTOS. Be sure that Secure must be chosen at the Sub-core start state on the current version. Otherwise, the created project can't be built successfully.

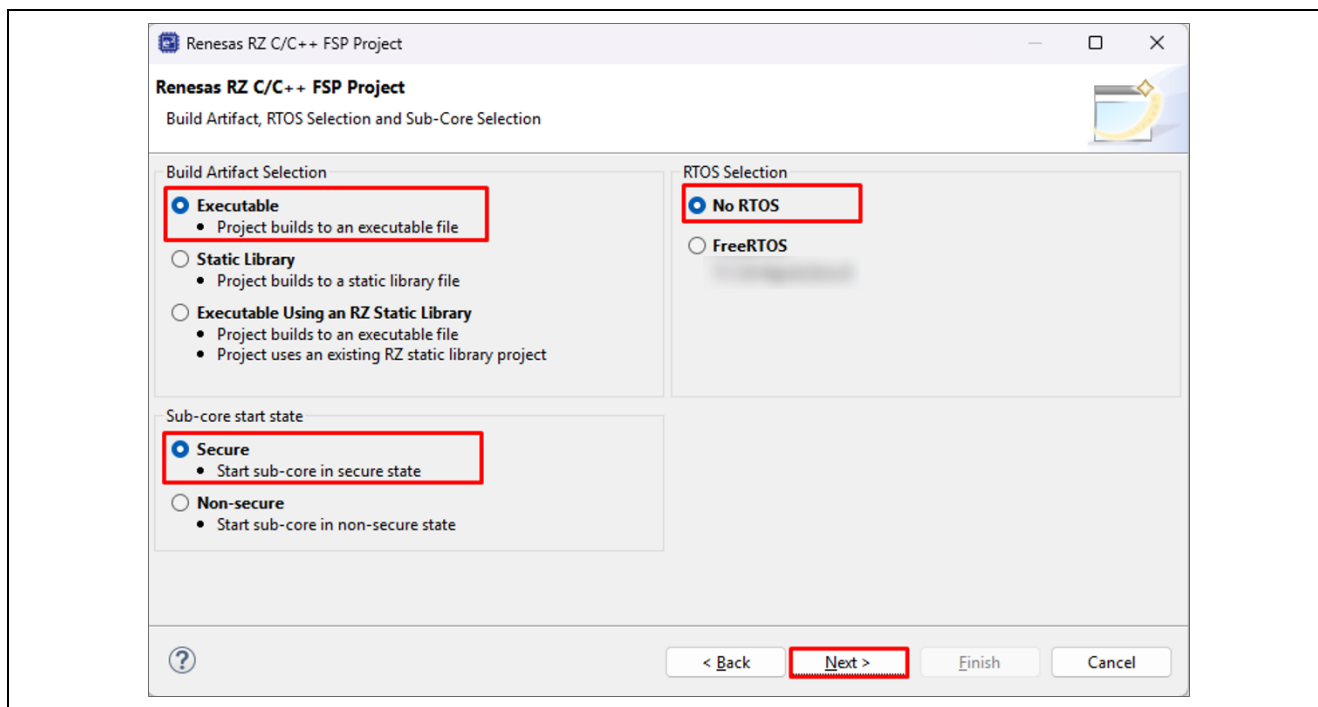


Figure 70. e² studio Project Configuration window (part 4)

9. Select the **Blinky** template for your board and click the [Finish] button.

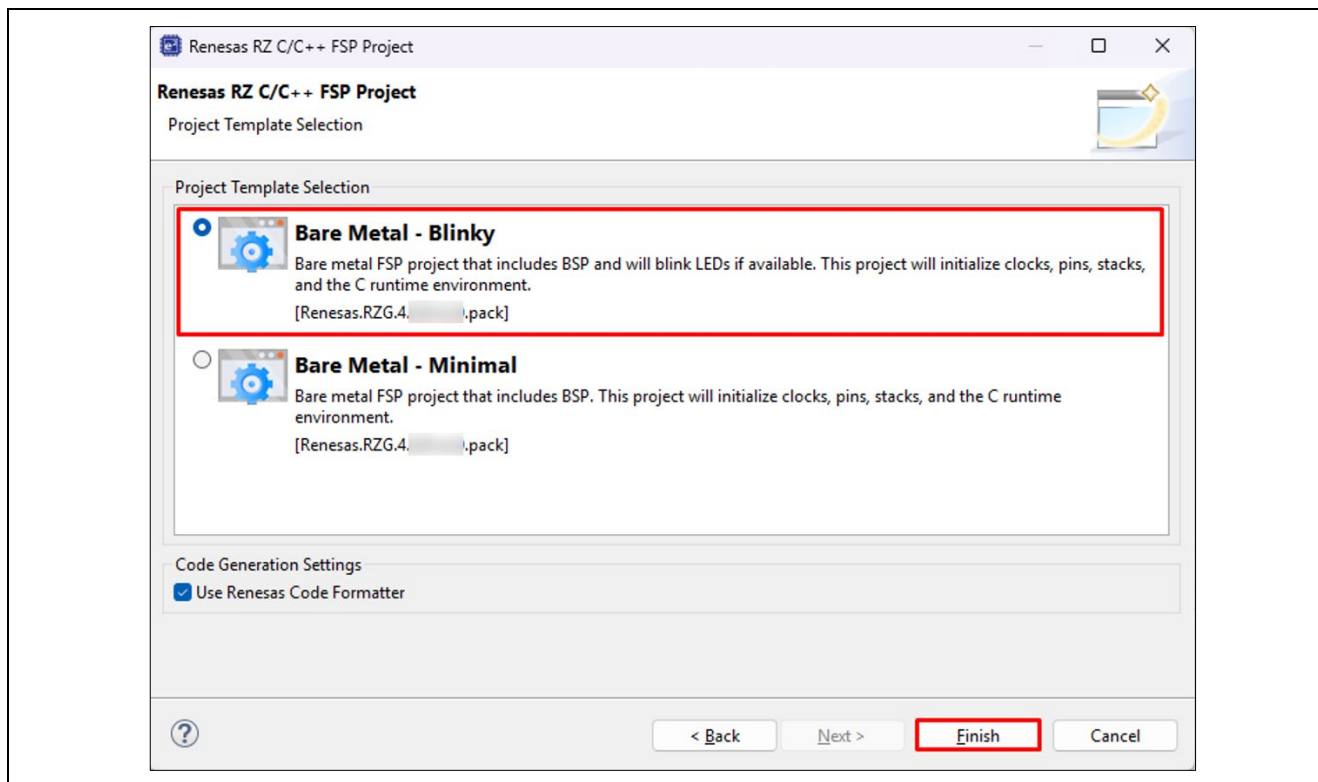


Figure 71. e² studio Project Configuration window (part 4)

Once the project has been created, the name of the project will show up in the **Project Explorer** window of e² studio. Now, click the **[Generate Project Content]** button in the top right corner of the **Project Configuration** window to generate your board-specific files.

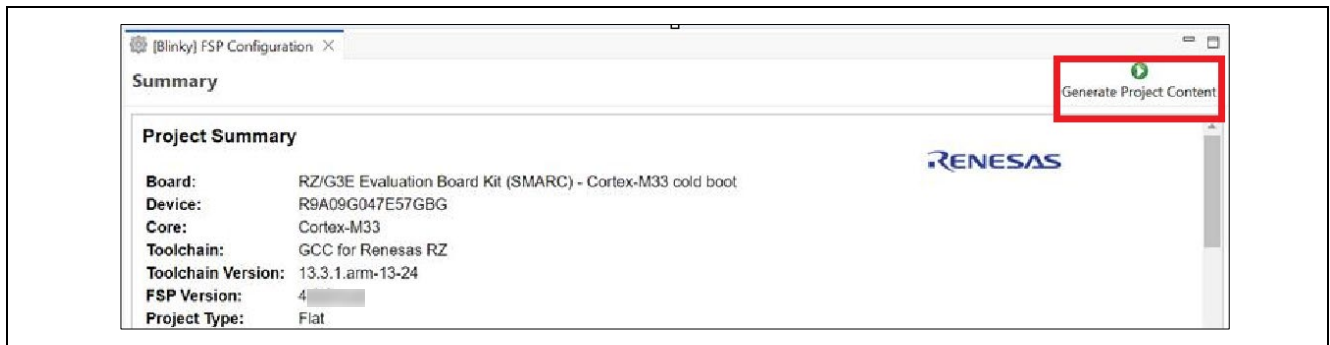


Figure 72. e² studio Project Configuration tab

Your new project is now created, configured, and ready to build.

4.3.1 Details about the Blinky Configuration

The Generate Project Content button creates configuration header files, copies source files from templates, and generally configures the project based on the state of the Project Configuration screen.

For example, if you check a box next to a module in the Components tab and click the Generate Project Content button, all the files necessary for the inclusion of that module into the project will be copied or created. If that same check box is then unchecked, those files will be deleted.

4.3.2 Configuring the Blinky Clocks

By selecting the Blinky template, the clocks are configured by e² studio for the Blinky application. The clock configuration tab (see 5.2.3 Configuring Clocks) shows the Blinky clock configuration. The Blinky clock configuration is stored in the BSP clock configuration file.

4.3.3 Configuring the Blinky Pins

By selecting the Blinky template, the GPIO pins used to toggle the LED1 are configured by e² studio for the Blinky application. The pin configuration tab shows the pin configuration for the Blinky application (see 5.2.4. Configuring Pins). The Blinky pin configuration is stored in the BSP configuration file.

4.3.4 Configuring the Parameters for Blinky Components

The Blinky project automatically selects the following HAL components in the Components tab:

- r_gtm
- r_ioport

To see the configuration parameters for any of the components, check the Properties tab in the HAL window for the respective driver (see 5.2.8. Adding and Configuring HAL Drivers).

4.3.5 Where is main()?

The main function is located in <project>/rz_gen/main.c. It is one of the files that are generated during the project creation stage and only contains a call to hal_entry(). For more information on generated files, see Adding and Configuring HAL Drivers.

4.3.6 Blinky Example Code

The blinky application is stored in the hal_entry.c file. This file is generated by e² studio when you select the Blinky Project template and is located in the project's src/ folder.

The application performs the following steps:

1. Get the LED information for the selected board from the bsp_leds_t structure.
2. Set the configuration of the Timer (GTM) and the callback function that is called when an interrupt is fired.
3. Define the output level HIGH for the GPIO pins controlling the LEDs for the selected board.
4. Toggle the LEDs by writing to the GPIO pin with "R_BSP_PinWrite((bsp_io_port_pin_t) pin, pin_level)" in the callback function of GTM that is called with the specified interval.

4.4 Build the Blinky Project

Highlight the new project in the Project Explorer window by clicking on it and building it.

There are three ways to build a project:

1. Click on Project in the menu bar and select Build Project.
2. Click on the hammer icon.
3. Right-click on the project and select Build Project.

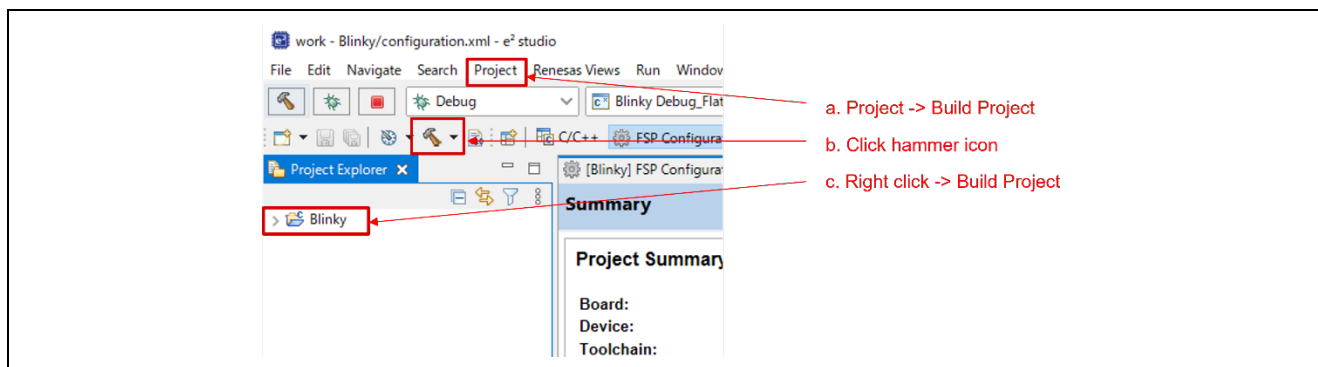


Figure 73. e² studio Project Explorer window

Once the build is complete, a message is displayed in the Build Console window that displays the final image file name and section sizes in that image.

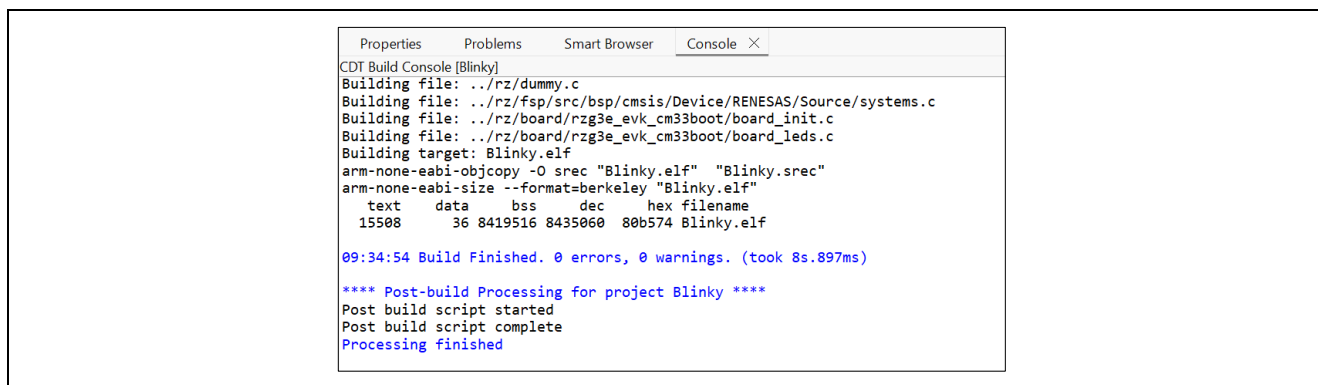


Figure 74. e² studio Project Build console

4.5 Debug the Blinky Project

4.5.1 Debug prerequisites

To debug the project on a board, you need

- The board to be connected to e² studio
- The debugger needs to be configured to talk to the board
- The application is to be programmed for the microprocessor

Applications run from the internal RAM or external RAM of your microprocessor. To run or debug the application, the application must first be programmed to RAM by a JTAG debugger. The SMARC EVK board has a JTAG header and requires an external JTAG debugger to connect to the header.

4.5.2 Debug Steps

To debug the Blinky application, follow these steps:

1. Configure the debugger for your project by clicking **Run > Debugger Configurations**.

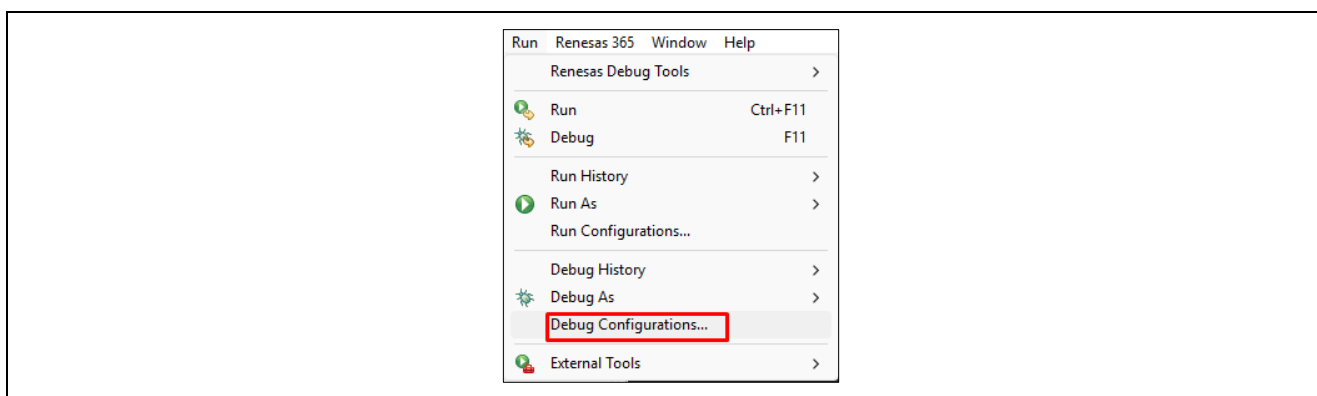


Figure 75. e² studio Debug icon

Or by selecting the drop-down menu next to the bug icon and selecting **Debugger Configurations ...**

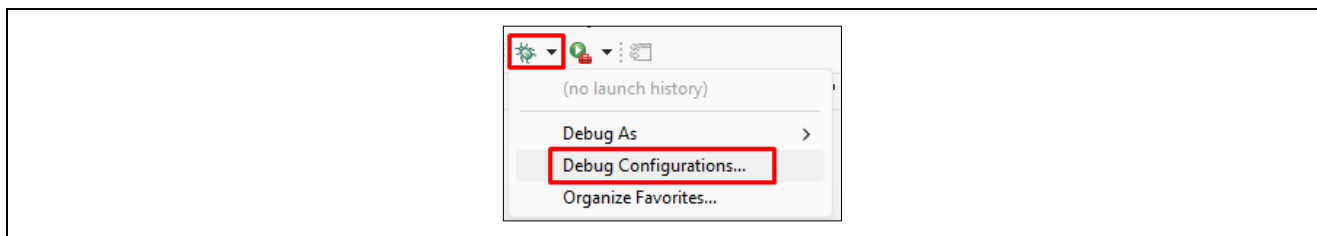


Figure 76. e² studio Debugger Configurations selection option

2. Select your debugger configuration in the window. If it is not visible, then it must be created by clicking the New icon in the top left corner of the window (see red boxes in Figure 69). Once selected, the **Debug Configuration** window displays the **Debug configuration** for your **Blinky** project.

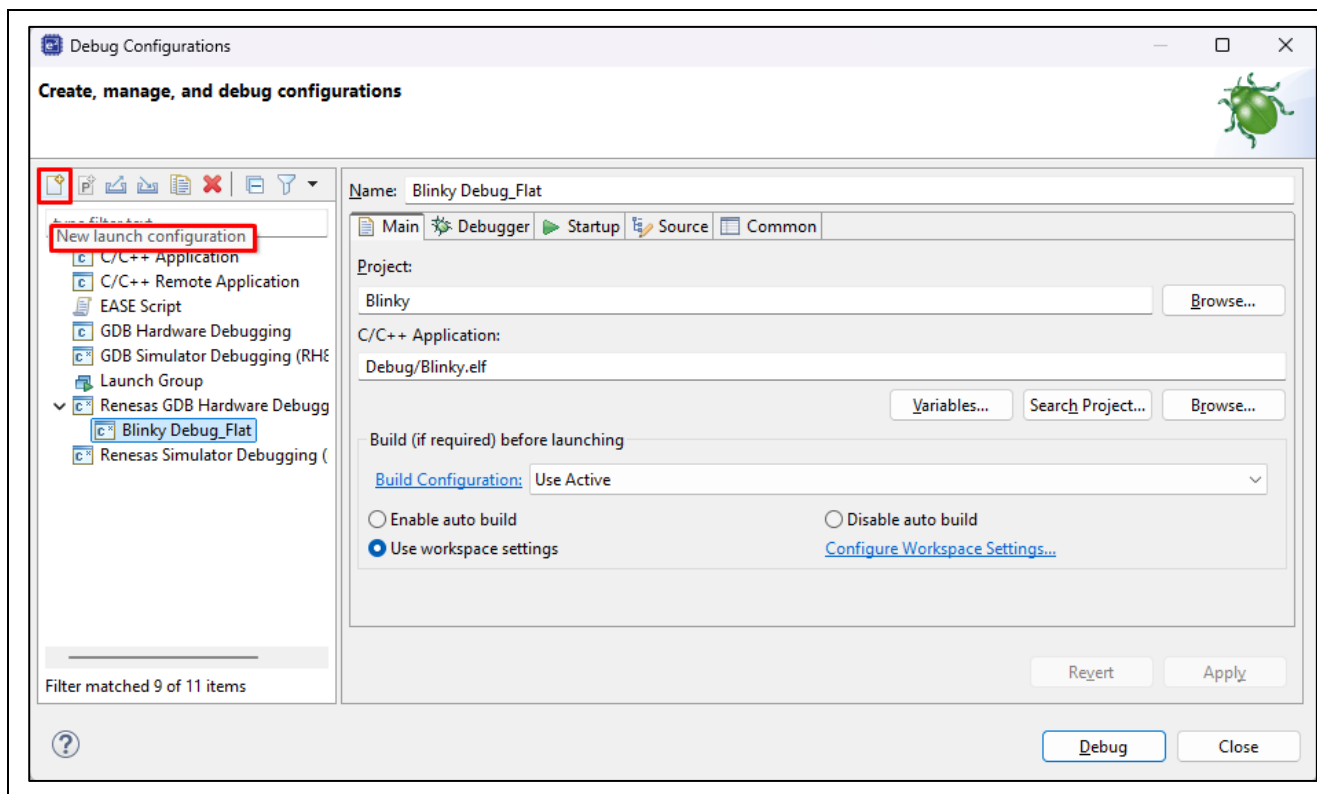


Figure 77. e² studio Debugger Configurations window with Blinky project (1)

3. Select the debug configuration for the generated project and select the **Debugger** tab.

Click the **[Debug]** button to begin debugging the application, then wait for **RZ Debug** to finish launching the debug session.

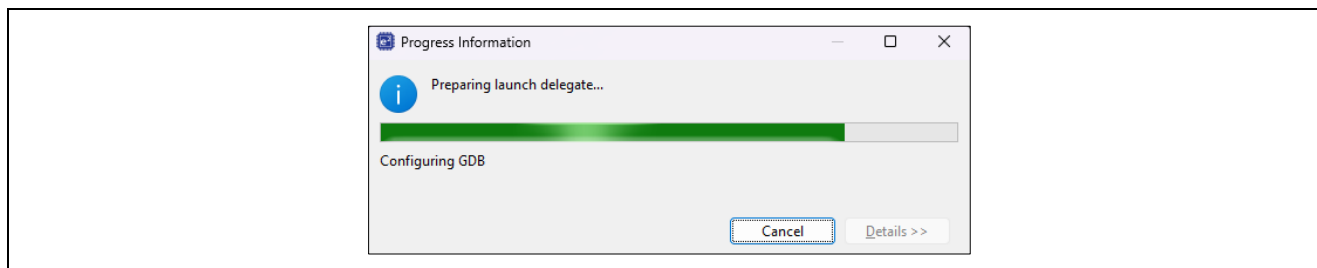


Figure 78. e² studio Debugger Configurations window with Blinky project (2)

4.5.2.1 Debug multi-core steps

To debug both the RZ/G3S CM33 core and the RZ/G3S CM33_FPU core simultaneously, follow these steps:

1. Create a separate e² studio workspace for each core. For example, use **workspace_cm33** for the CM33 core and **workspace_cm33_fpu** for the CM33_FPU core.

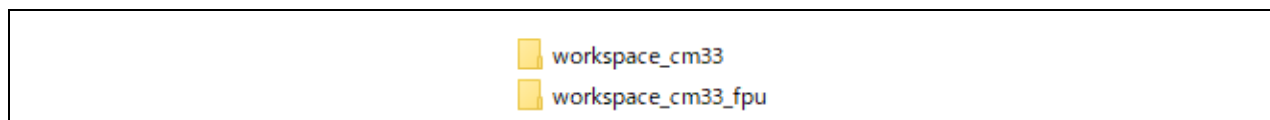


Figure 79. Workspace creation

- Launch e² studio and select the workspace for the CM33 core.

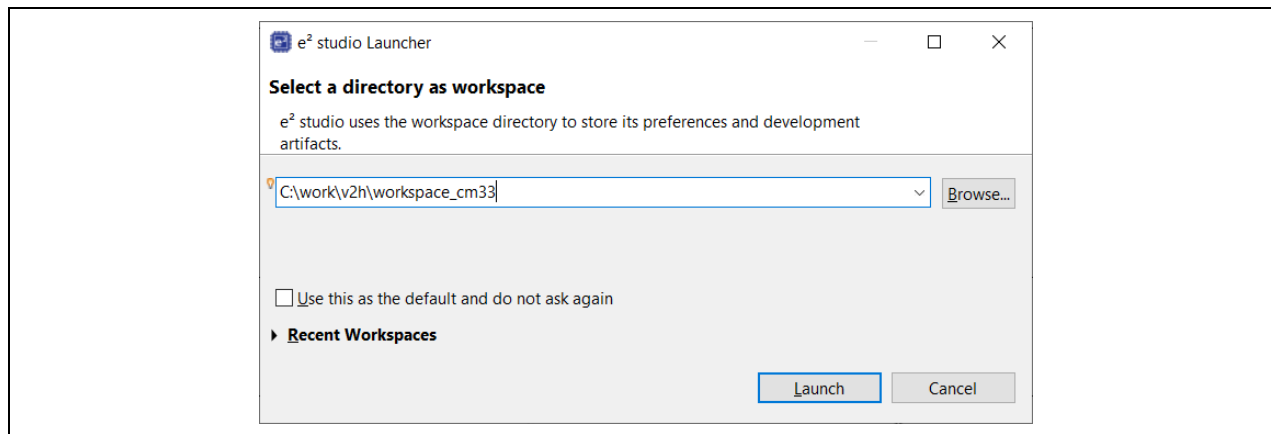


Figure 80. Launch e² studio (for CM33 core)

Create an FSP project for the CM33 core. In the configuration window, select the appropriate **Core** and **Project Template Selection** as shown in the figure below.

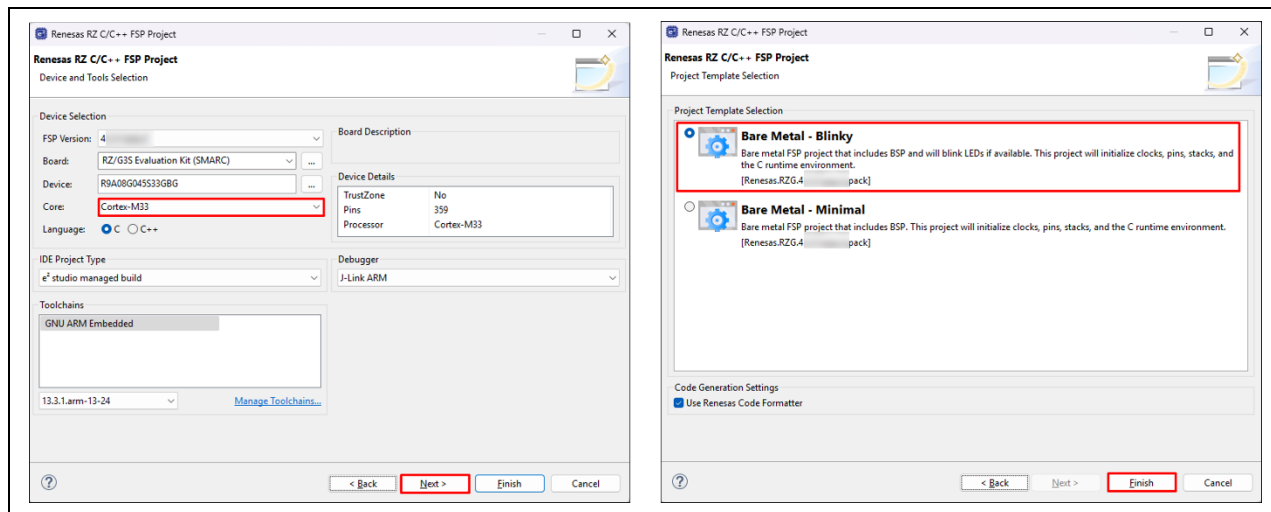


Figure 81. CM33 Core Project Creation

- Build the FSP project for the CM33 core.

5. Create an FSP project for the CM33_FPU core. In the configuration window, select the appropriate **Core** and **Project Template Selection** as shown in the figure below.

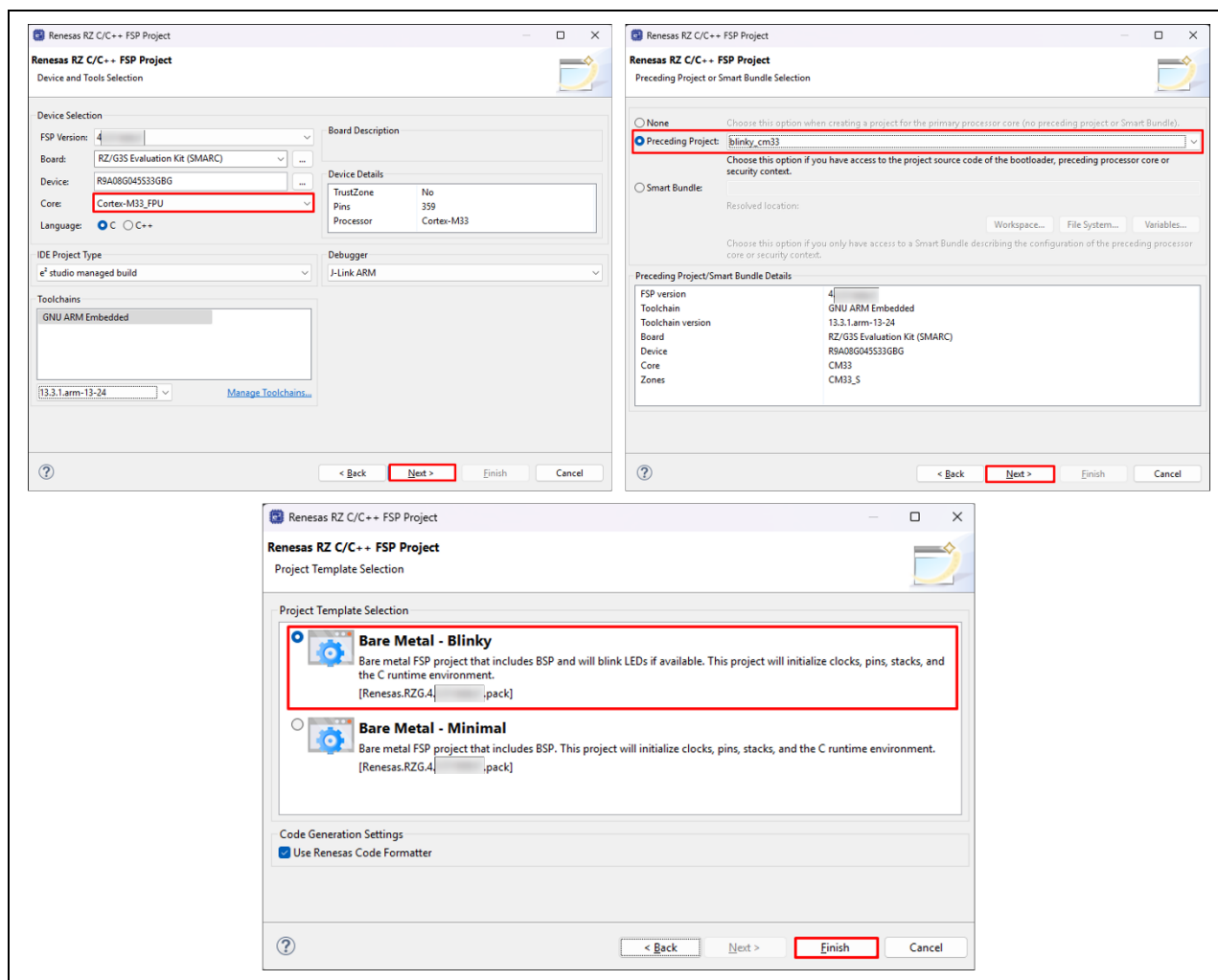


Figure 82. CM33_FPU Core Project Creation

6. Build the FSP project for the CM33_FPU core.
7. Copy the two projects created in the CM33 core workspace into the CM33_FPU core workspace.

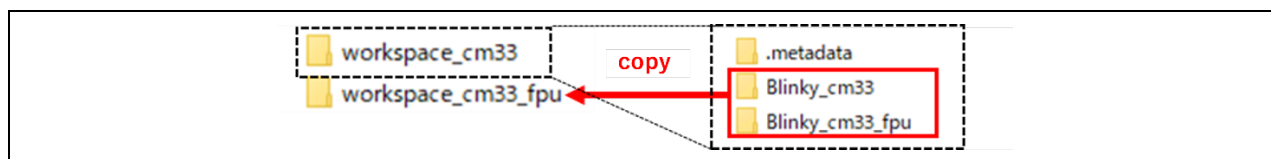


Figure 83. Project Copy

8. Click the **Debug Configuration** in the workspace for the CM33 core, then click **Debug**.

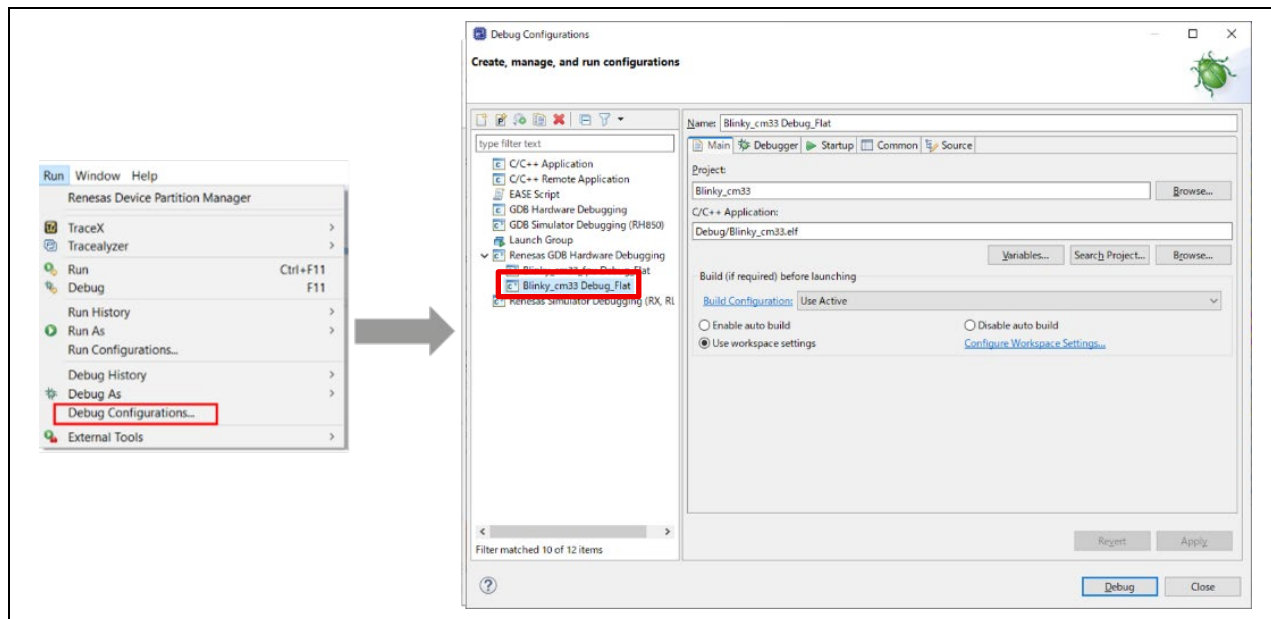


Figure 84. CM33 core Debug Configuration

9. Launch a new e² studio and select the workspace for the CM33_FPU core.

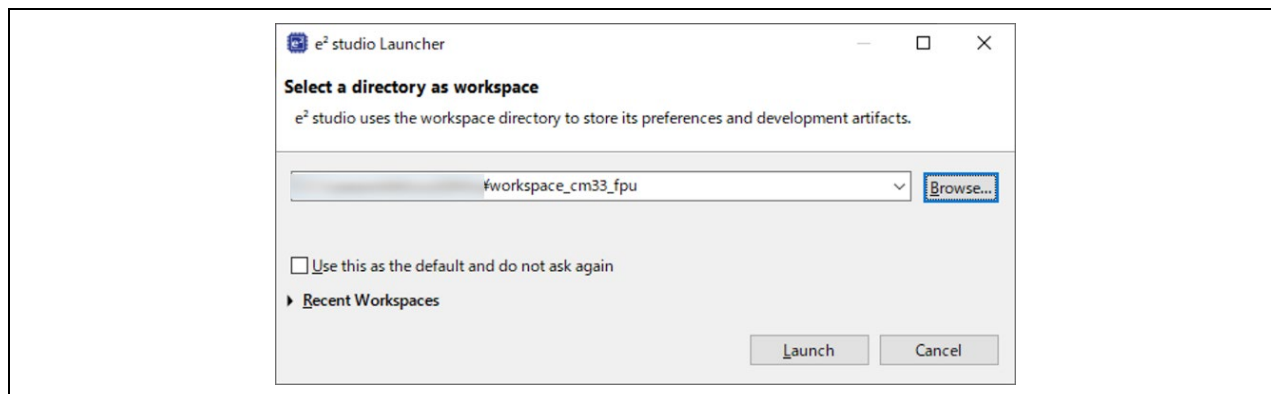


Figure 85. Launch e² studio (for CM33_FPU core)

10. Import the project for the CM33_FPU core.

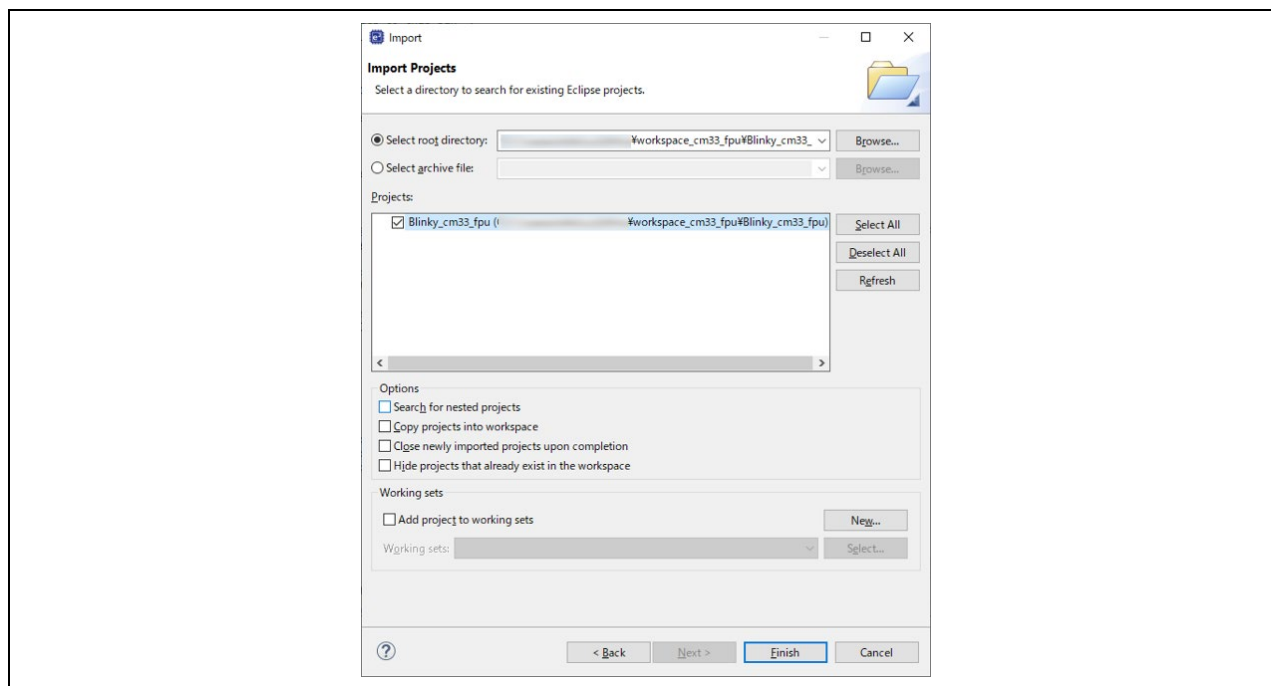


Figure 86. Import CM33_FPU Core Project

11. In the CM33_FPU core workspace, click **Debug Configuration** and then click **Debug**.

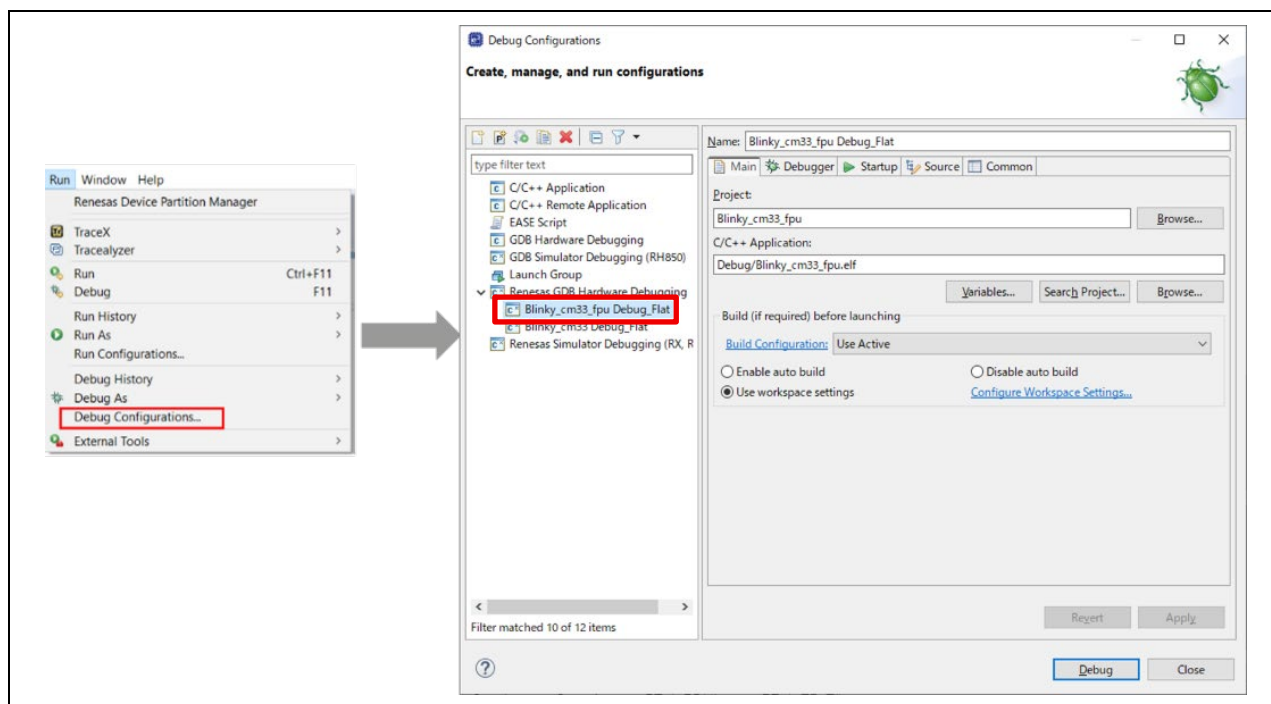


Figure 87. CM33_FPU core Debug Configuration

12. This will enable the debugger functions for each core in their respective e² studio workspaces for the CM33 core and the CM33_FPU core.

4.5.3 Details about the Debug Process

In debug mode, e² studio executes the following tasks:

1. Downloading the application image to the microprocessor and programming the image to the internal and/or external memory.
2. Setting a breakpoint at main().
3. Setting the stack pointer register to the stack.
4. Loading the program counter register with the address of the reset vector.
5. Displaying the startup code where the program counter points to.

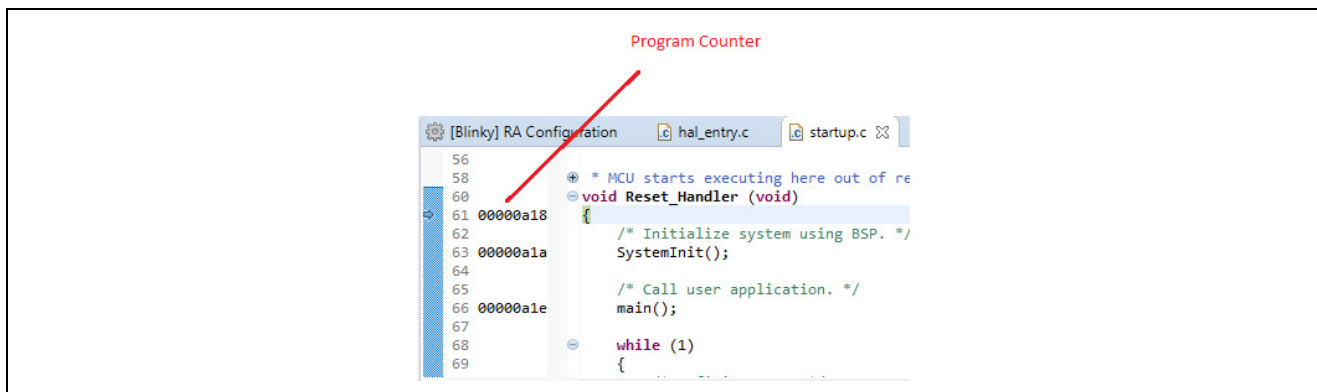


Figure 88. e² studio Debugger memory window

4.5.4 Run the Blinky Project

While in Debug mode, click **Run > Resume** or click on the **Play** icon twice.

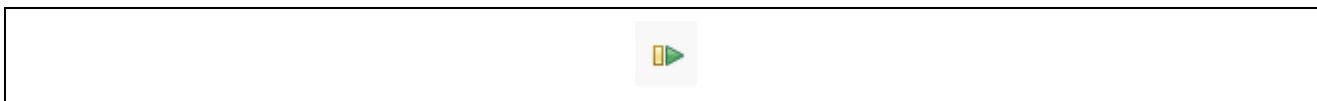


Figure 89. e² studio Debugger Play icon

The LED on the Pmod LED should now be blinking.

5. FSP Application Launch with e² studio

5.1 Creating a Project

5.1.1 What is a Project?

In e² studio, all FSP applications are organized in RZ MPU projects. Setting up an RZ MPU project involves:

1. **Creating a Project**
2. **Configuring a Project**

These steps are described in detail in the next two sections. When you have existing projects already, after you launch e² studio and select a workspace, all projects previously saved in the selected workspace are loaded and displayed in the **Project Explorer** window. Each project has an associated configuration file named **configuration.xml**, which is located in the project's root directory.

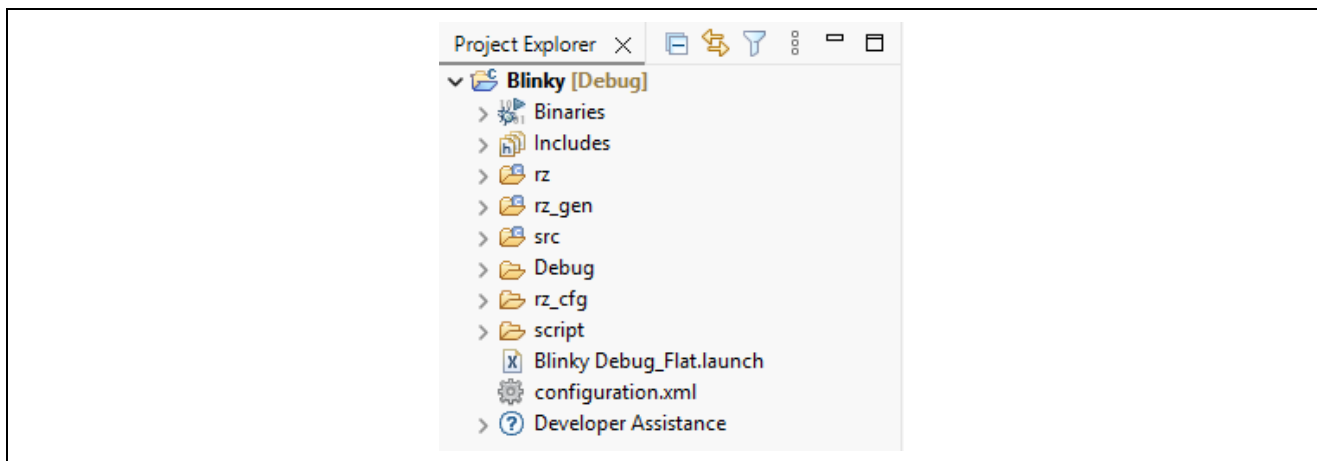


Figure 90. e² studio Project Configuration file

Double-click on the configuration.xml file to open the RZ MPU Project Editor. To edit the project configuration, make sure that the **FSP Configuration** perspective is selected in the upper right-hand corner of the e² studio window. Once selected, you can use the editor to view or modify the configuration settings associated with this project.

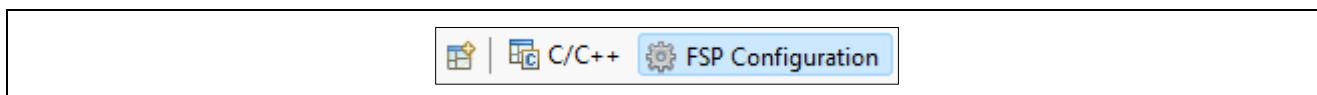


Figure 91. e² studio FSP Configuration Perspective

Note: Whenever the RZ project configuration (that is, the **configuration.xml** file) is saved, a verbose RZ Project Report file (**rz_cfg.txt**) with all the project settings is generated. The format allows differences to be easily viewed using a text comparison tool. The generated file is located in the project root directory.

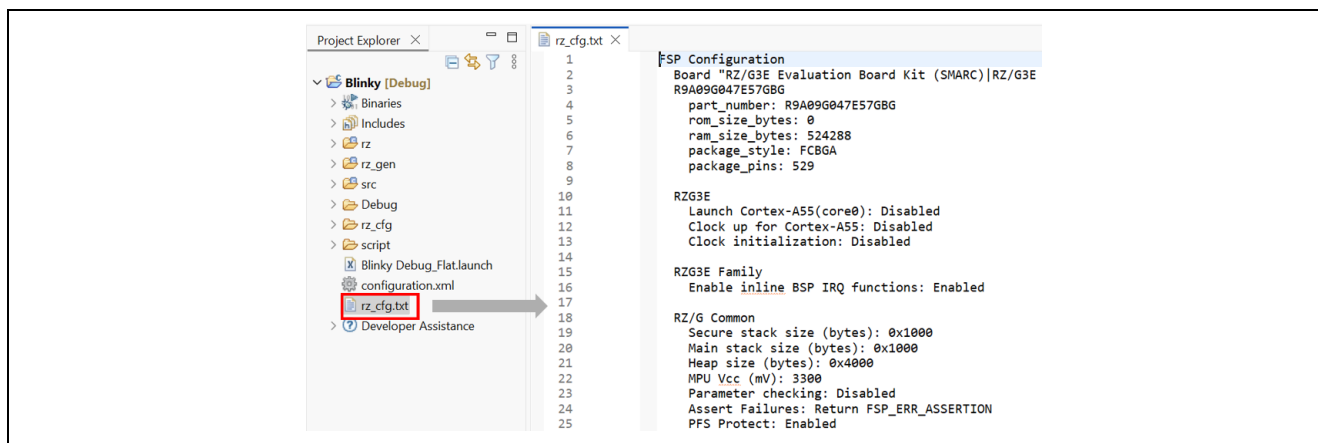


Figure 92. RZ Project Report

The RZ Project Editor has several tabs. The configuration steps and options for individual tabs are discussed in the following sections.

Note: The tabs available in the RZ Project Editor depend on the e² studio version, and the layout may vary slightly, the functionality should be easy to follow.

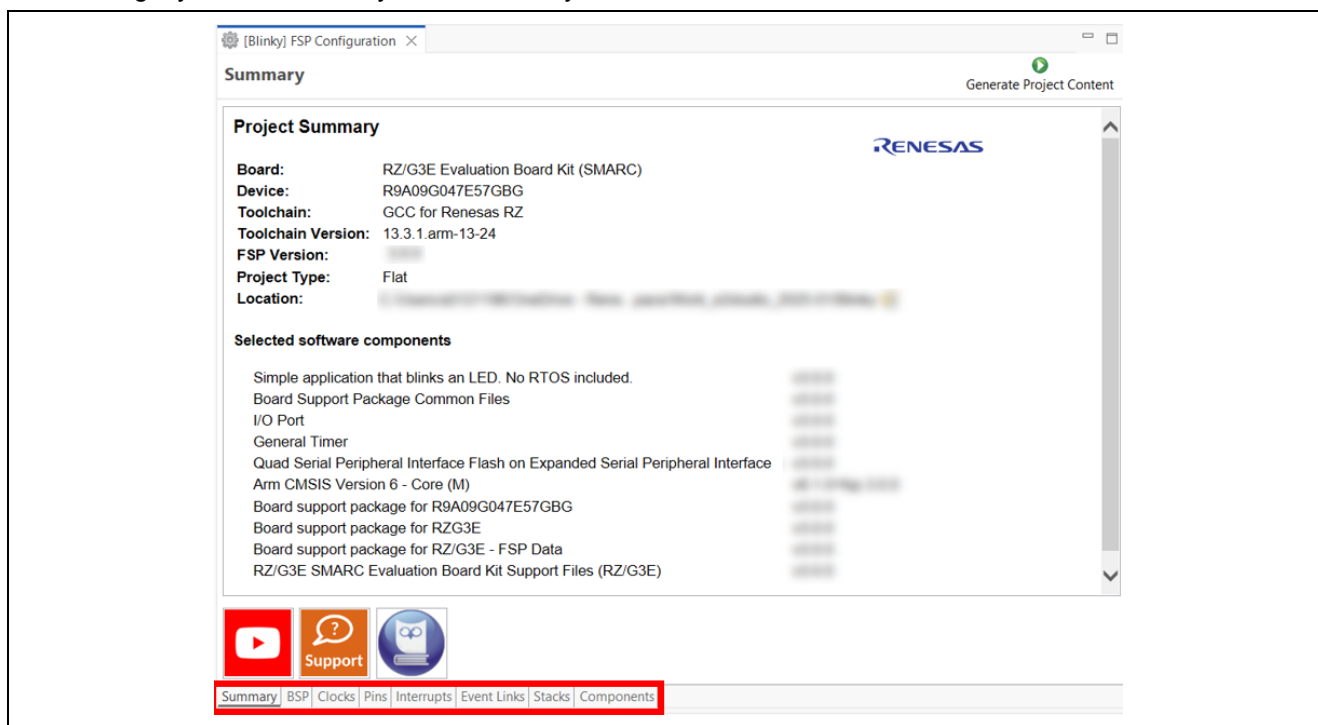


Figure 93. RZ Project Editor tabs

5.1.2 Creating a New Project

For RZ MPU applications, generate a new project using the following steps:

1. Click on File > New > C/C++ Project.

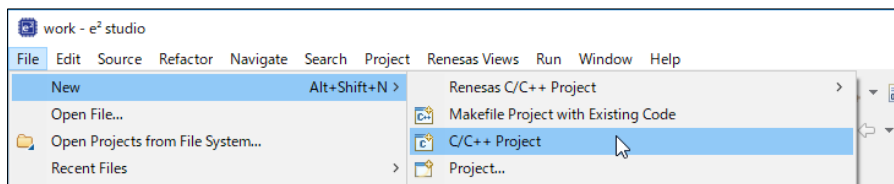


Figure 94. New RZ MPU Project

2. Then click on the **Renesas RZ C/C++ FSP Project** template for the type of project you are creating.

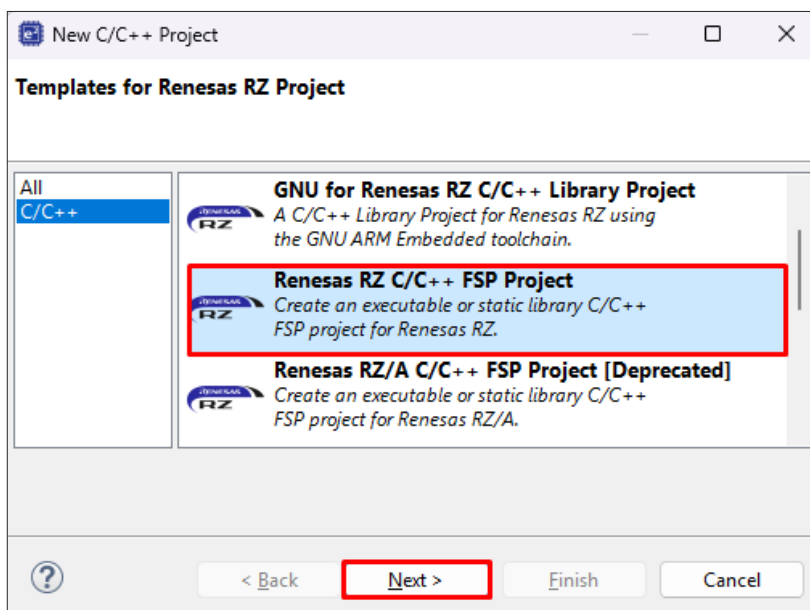


Figure 95. New Project Templates

3. Select a project name and location. Then click the **[Next >]** button.

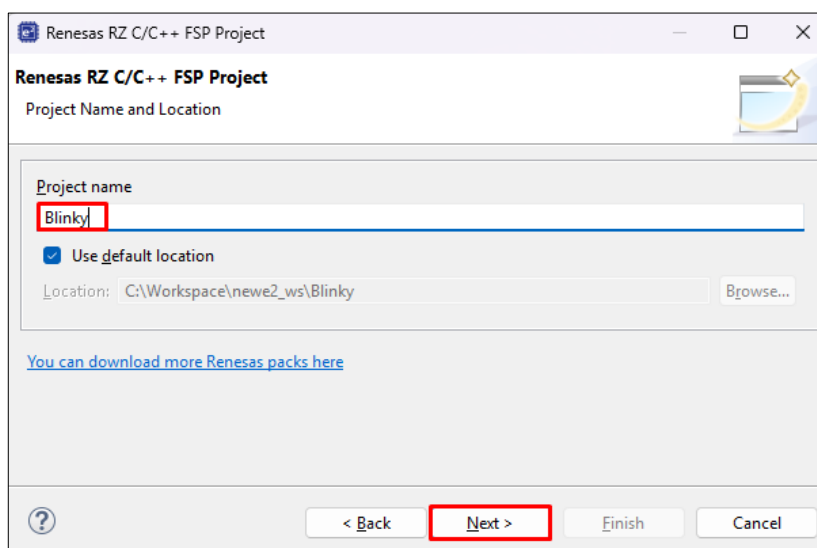


Figure 96. RZ MPU Project Generator (Screen 1)

5.1.2.1 Selecting a Board and Toolchain

In the Project Configuration window, select the hardware and software environment:

1. Select the **FSP version**.
2. Select the **Board** for your application. You can select an existing RZ MPU Evaluation Kit or select a **Custom User Board** for any of the RZ MPU devices with your own BSP definition.
3. Select the **Device**. The **Device** is automatically populated based on the **Board** selection. Only change the **Device** when using the **Custom User Board** for the board selection.
4. Select the **Core**. You can select Core 1(CM33) or Core 2(CM33_FPU) if you selected RZ/G3S for the **Device**.
5. To add threads, select **RTOS** or **No RTOS** if an RTOS is not being used.
6. The **Toolchain** selection defaults to **GNU Arm Embedded**.
7. Select the **Toolchain version**. This should default to the installed toolchain version.
8. Select the **Debugger**. The J-Link Arm Debugger is preselected.
9. Click the [**Next >**] button.

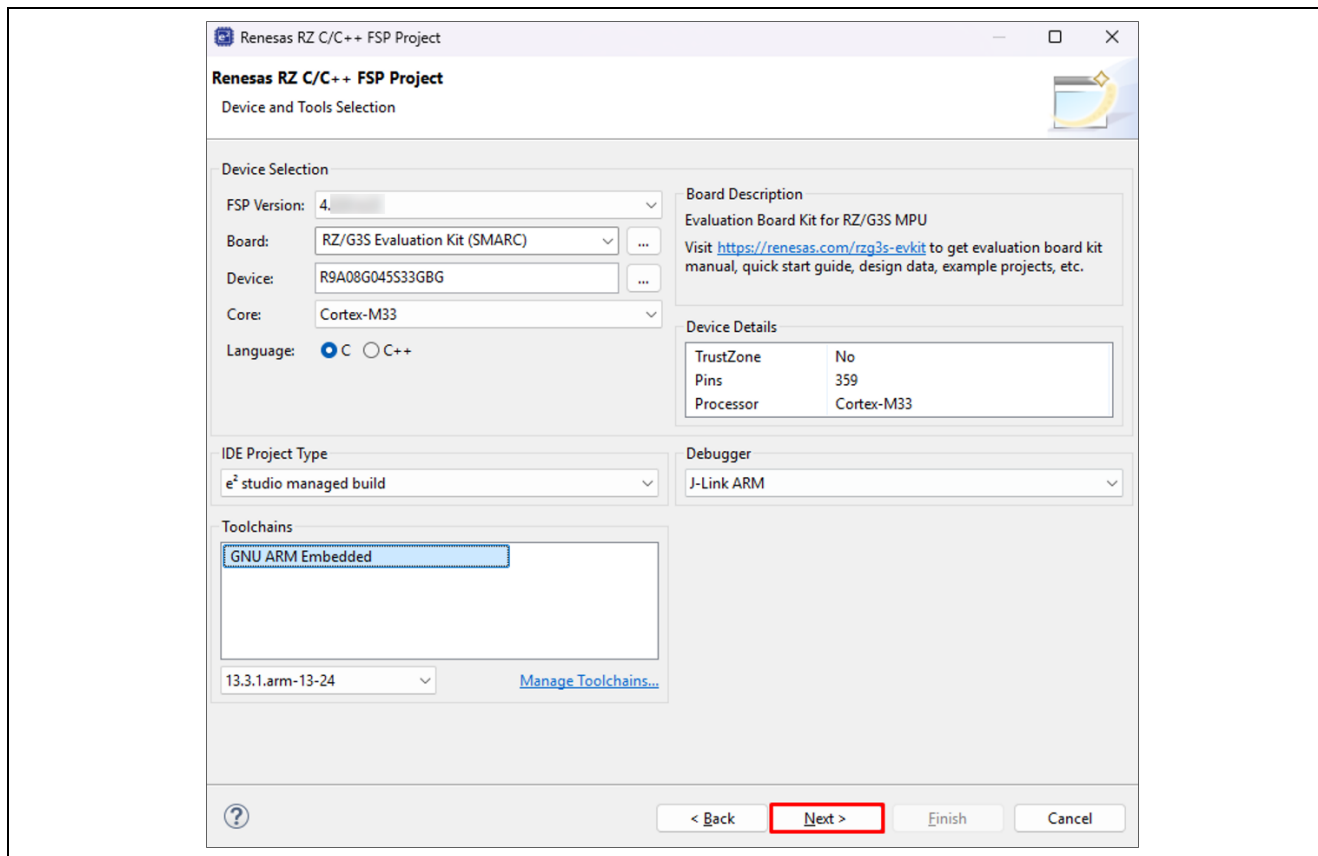


Figure 97. RZ MPU Project Generator (Screen 2)

If Core 2(CM33_FPU) is selected in **procedure 4**, you need to select the preceding project. To select the preceding project when creating the Core 2(CM33_FPU) project, it is required to prepare Core 1(CM33) before creating the Core 2(CM33_FPU) project.

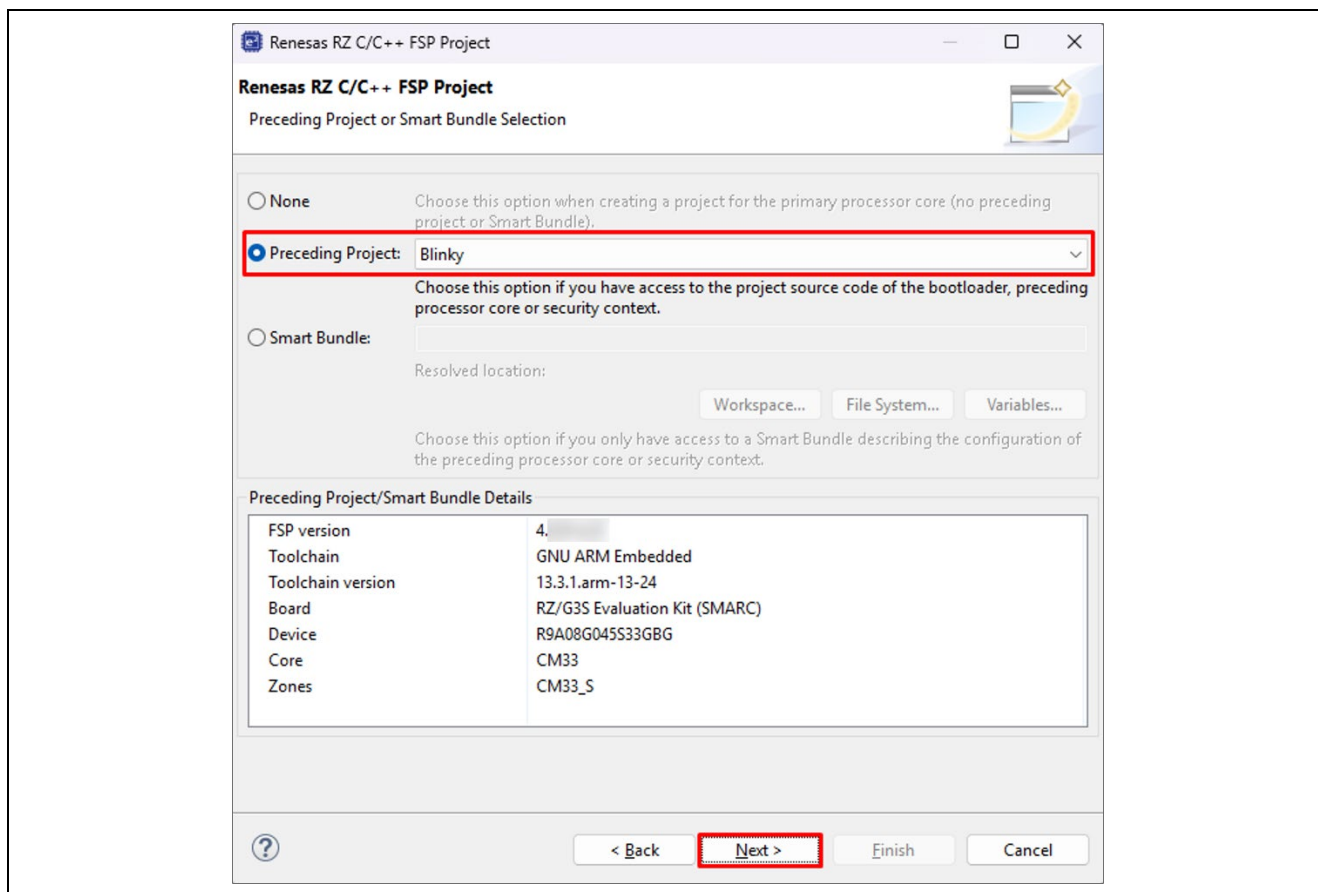


Figure 98. RZ MPU Project Generator (Screen 3)

5.1.2.2 Selecting a Project Template

In the next window, select the **Build artifact**, **Sub-core start state**, and **RTOS**. Be sure that you select **Secure** as the **Sub-core start state** in the current version.

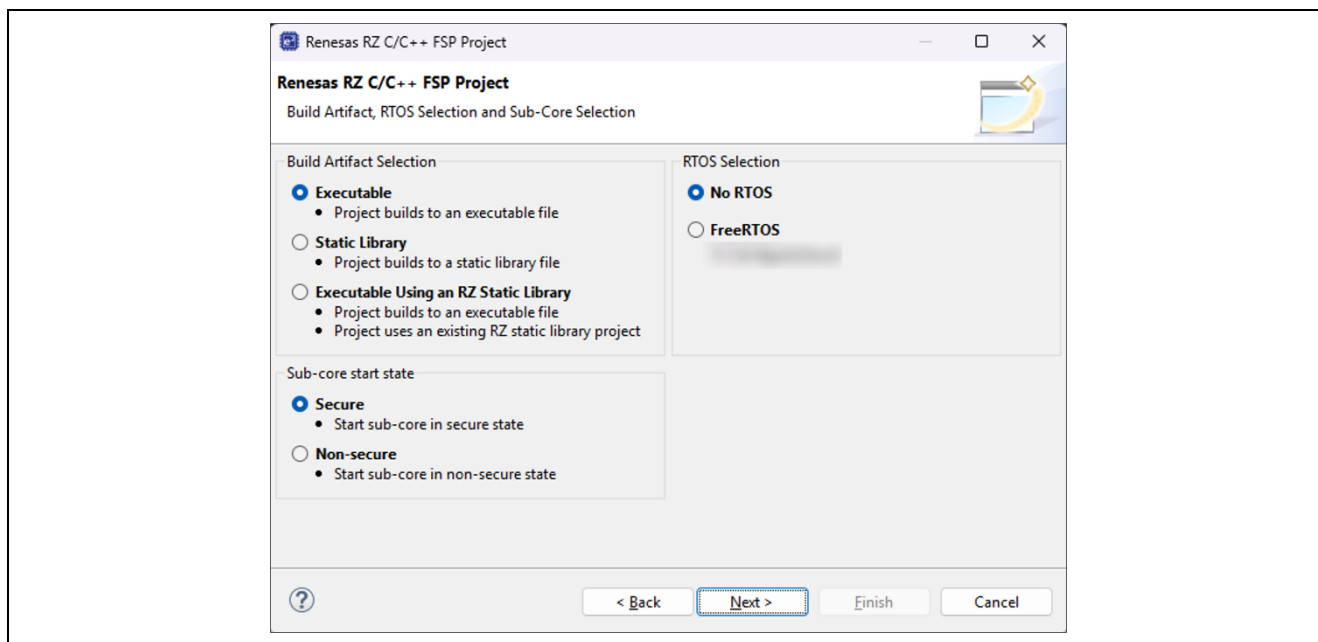


Figure 99. RZ MPU Project Generator (Screen 4)

In the next window, select a project template from the list of available templates. By default, this screen shows the templates that are included in your current RZ MPU Pack. Once you have selected the appropriate template, click the **[Finish]** button.

Note: If you want to develop your own application, select the basic template for your board, **Bare Metal - Minimal** or **FreeRTOS - Minimal - Static Allocation**.

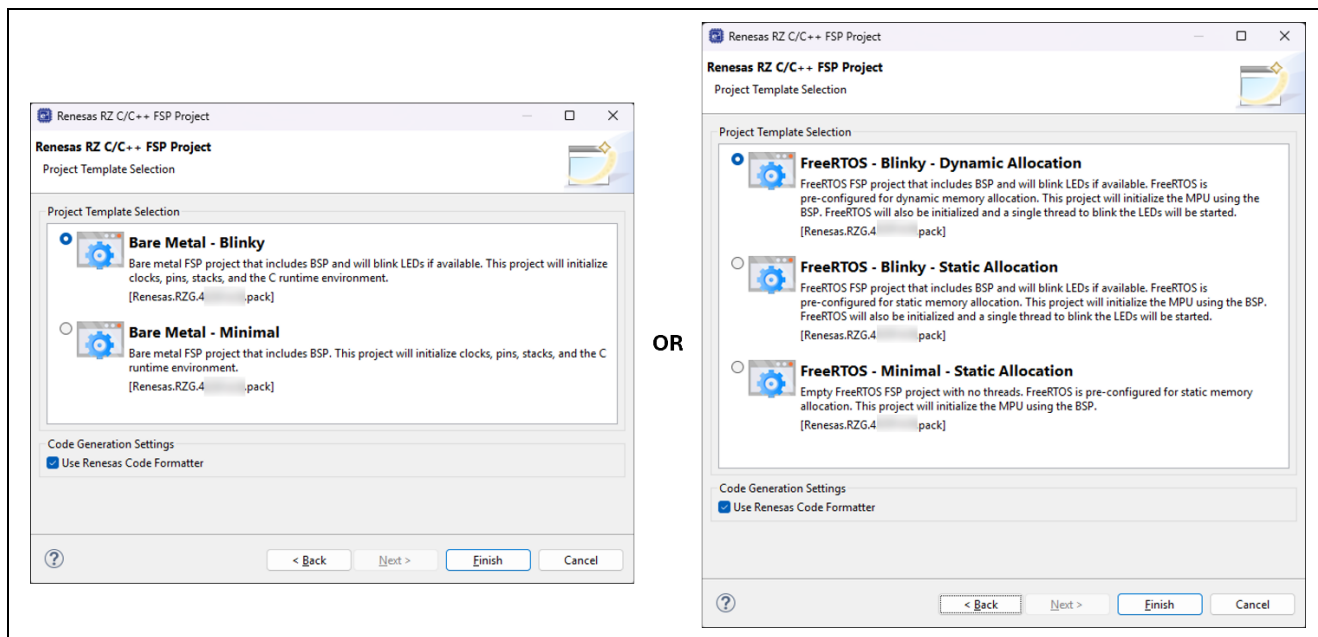


Figure 100. RZ MPU Project Generator (Screen 5)

When the project is created, e² studio displays a summary of the current project configuration in the RZ MPU Project Editor.

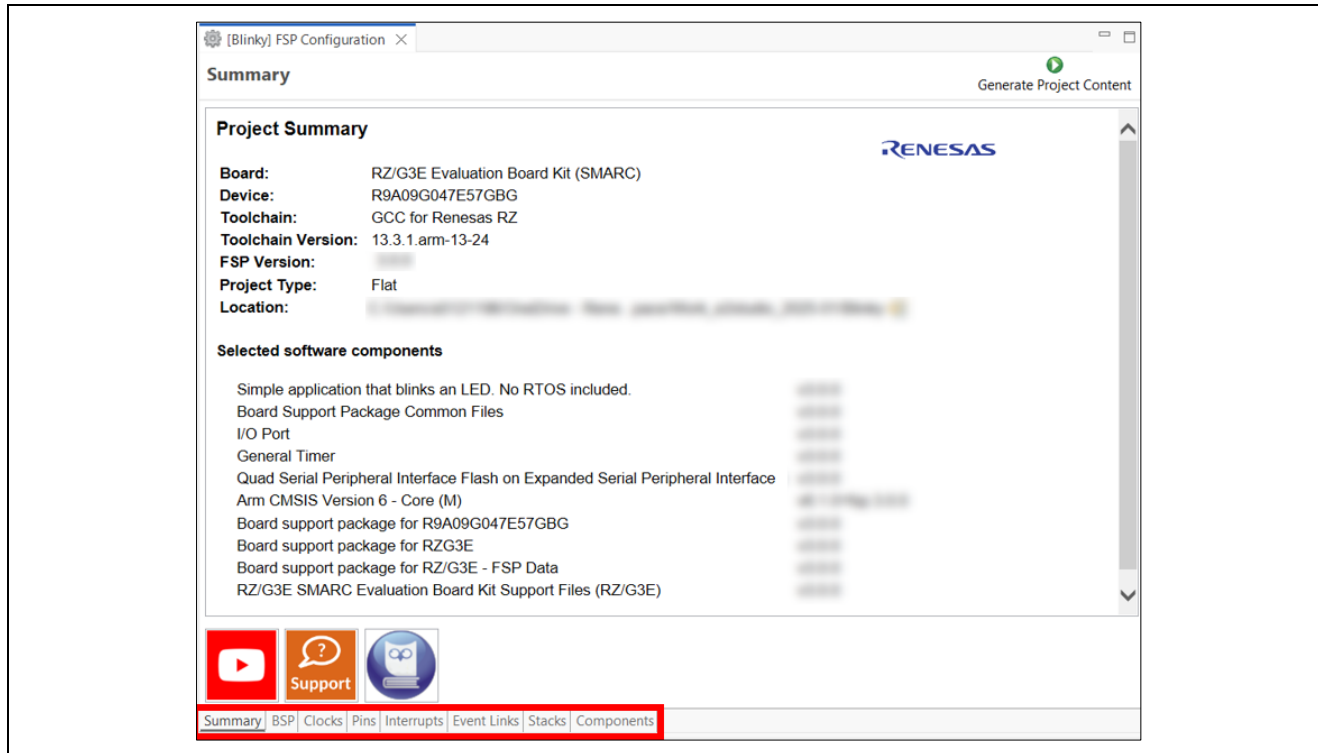


Figure 101. RZ MPU Project Editor and available editor tabs

At the bottom of the RZ MPU Project Editor view, you can find the tabs for configuring multiple aspects of your project:

- With the **Summary** tab, you can see all the key characteristics of the project: board, device, toolchain, and more.
- With the **BSP** tab, you can change board-specific parameters from the initial project selection.
- With the **Clocks** tab, you can refer to the MPU clock settings for your project. In the case of CM33 cold boot, you can configure the MPU clock settings for your project.
- With the **Pins** tab, you can configure the electrical characteristics and functions of each port pin.
- With the **Interrupts** tab, you can add new user events/interrupts.
- With the **Event Links** tab, you can configure events used by the Event Link Controller.
- With the **Stacks** tab, you can add and configure FSP modules. For each module selected in this tab, the **Properties** window provides access to the configuration parameters and interrupt selections.
- The **Components** tab provides an overview of the selected modules. Although you can also add drivers for specific FSP releases and application sample code here, this tab is normally only used for reference.

The functions and use of each of the supported tabs are explained in detail in the next section.

Note: RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/G3S, and RZ/G3L don't support the **Event Links** tab.

5.1.3 Duplication of Resources

In the case of the RZ/G3S Core 2(CM33_FPU) project, duplicate resources are indicated as a red character in the **Stacks** tab when using resources that are used in the linked Core 1(CM33) project.

The following image is an example of how both the Core 1(CM33) and Core 2(CM33_FPU) projects were created with the Blinky template. The duplication of r_gtm is indicated in the **Stacks** tab. To avoid this duplication, please change the channel resource in the **Properties** of r_gtm.

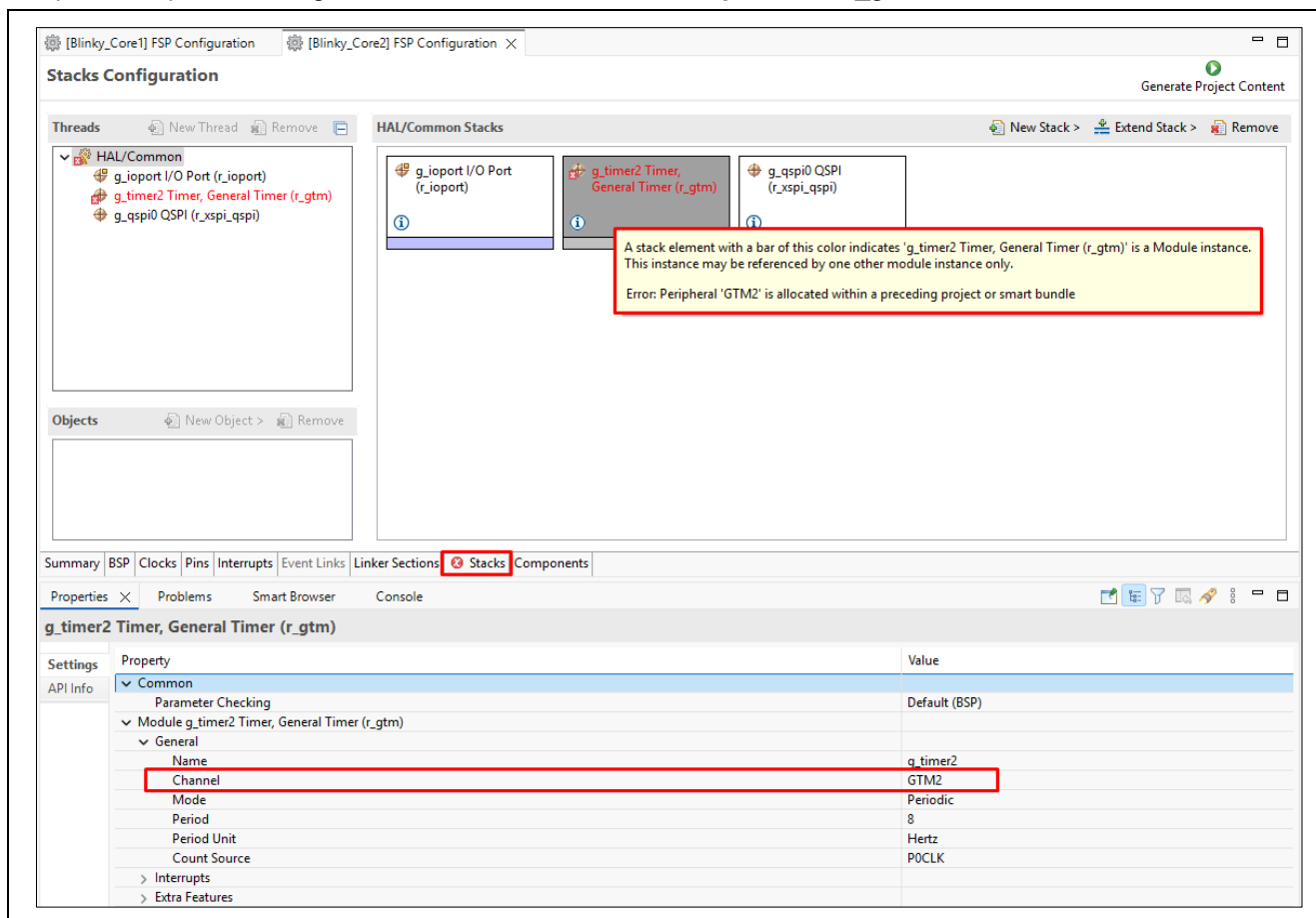


Figure 102. Duplication of resource between Core 1(CM33) and Core 2(CM33_FPU) projects

5.2 Configuring a Project

Each of the configurable elements in an FSP project can be edited using the appropriate tab in the RZ Configuration editor window. Importantly, the initial configuration of the MPU after reset and before any user code is executed is set by the configuration settings in the **BSP** tab. When you select a project template during project creation, e² studio configures default values that are appropriate for the associated board. You can change those default values as needed. The following sections detail the process of configuring each of the project elements for each of the associated tabs.

5.2.1 Summary Tab

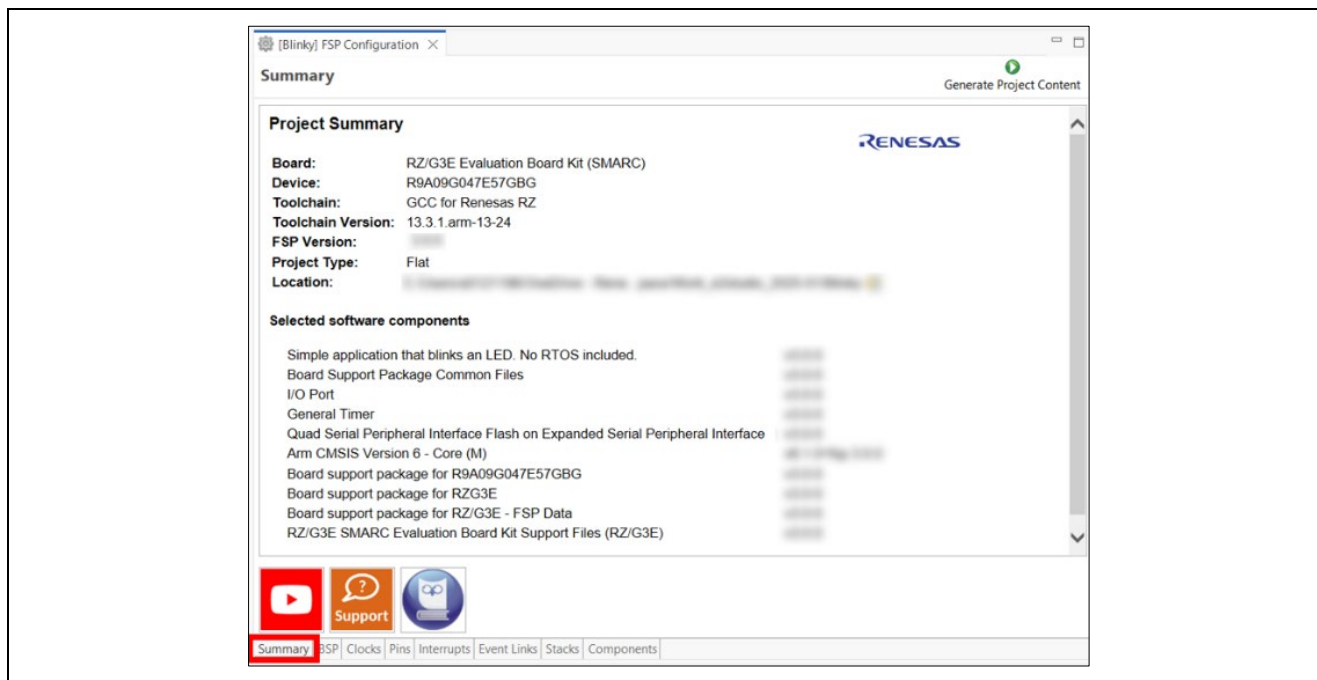


Figure 103. Configuration Summary tab

The **Summary** tab, seen in the above figure, identifies all the key elements and components of a project. It shows the target board, the device, the toolchain, and the FSP version. Additionally, it provides a list of all the selected software components and modules used by the project. This is a more convenient summary view when compared to the **Components** tab.

5.2.2 Configuring the BSP

The **BSP** tab shows the currently selected board (if any) and device. The Properties view is in the lower left of the Project Configurations view, as shown below.

Note: If the Properties view is not visible, click **Window > Show View > Properties** in the top menu bar.

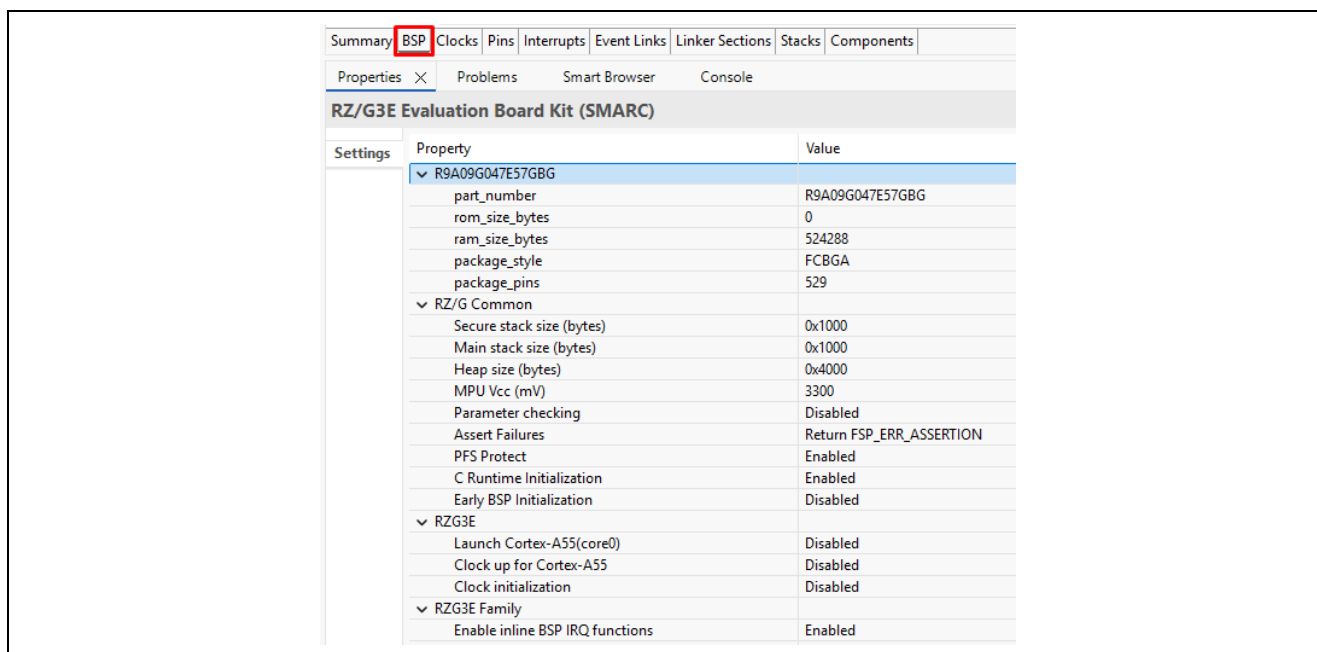


Figure 104. Configuration BSP tab

The **Properties** view shows the configurable options available for the BSP. These can be changed as required. The BSP is the FSP layer above the MPU hardware. e² studio checks the entry fields to flag invalid entries. For example, only valid numeric values can be entered for the stack size.

When you click the **[Generate Project Content]** button, the BSP configuration contents are written to `rz_cfg/fsp_cfg/bsp/bsp_cfg.h`. This file is created if it does not already exist.

Warning: Do not edit this file as it is overwritten whenever the Generate Project Content button is clicked.

5.2.3 Configuring Clocks

The **Clocks** tab presents a graphical view of the MPU's clock tree, and each HAL driver uses the settings for dedicated numerical calculation. For example, the `scif_uart` driver calculates the communication rate from the settings in the Clocks tab. Please note that the clock configuration is carried out on the main core (CA55) in advance when CM33 works as a sub-core. Thus, clocks configuration here must align with the settings on CA55.

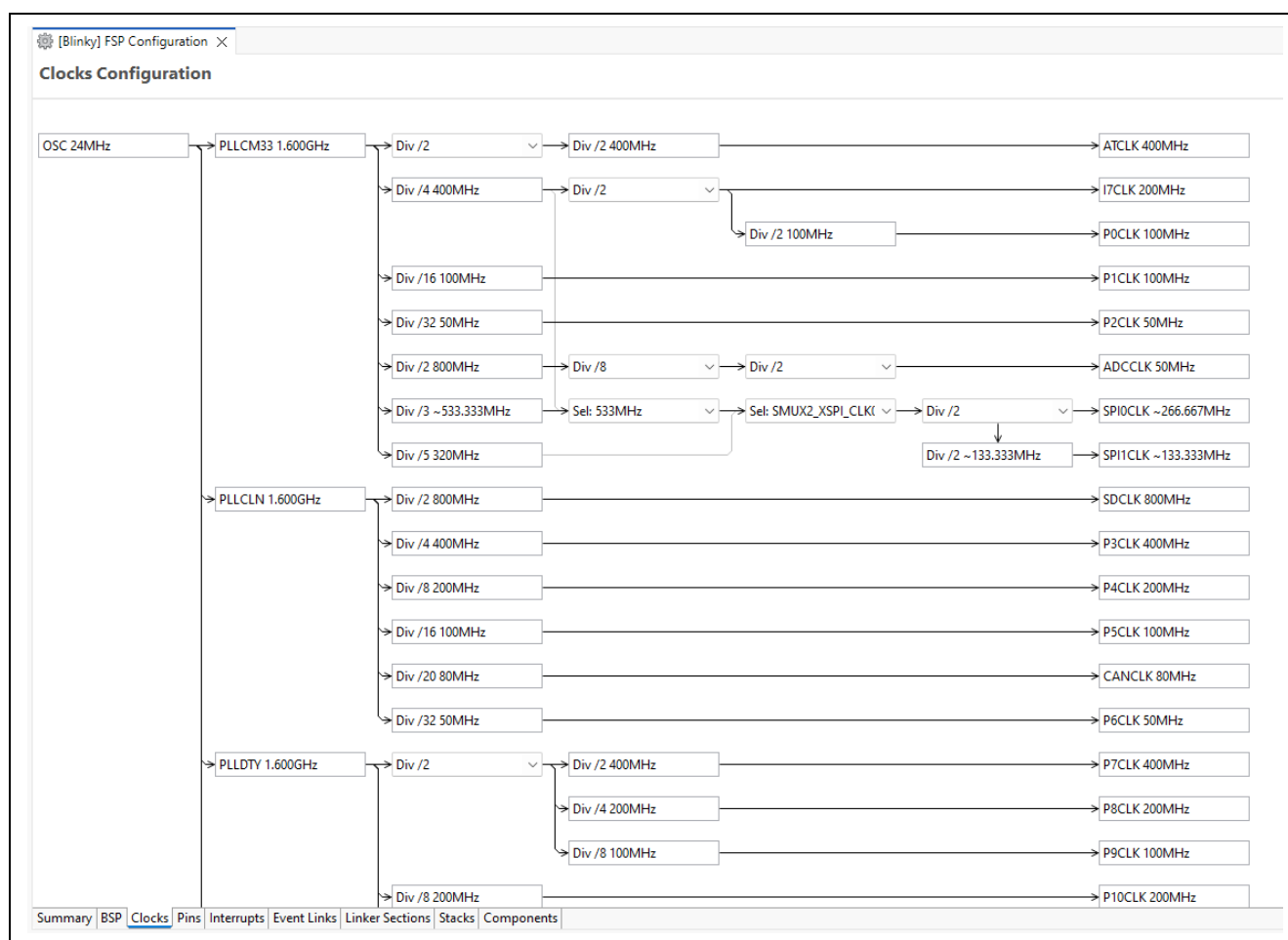


Figure 105. Configuration Clocks tab

When you click the **[Generate Project Content]** button, the clock configuration contents are written to `rz_gen/bsp_clock_cfg.h`. This file will be created if it does not already exist.

Warning: Do not edit this file as it is overwritten whenever the **[Generate Project Content]** button is clicked.

5.2.4 Configuring Pins

The **Pins** tab provides a flexible configuration of the MPU's pins. As many pins can provide multiple functions, they can be configured on a peripheral basis. For example, selecting a serial channel via the SCIF peripheral offers multiple options for the location of the receive and transmit pins for that module and channel. The location and function of the pins are shown in the **FSP Visualization** view. For more information on the function and color coding of the pins, please check the Legend in the **FSP Visualization** view.

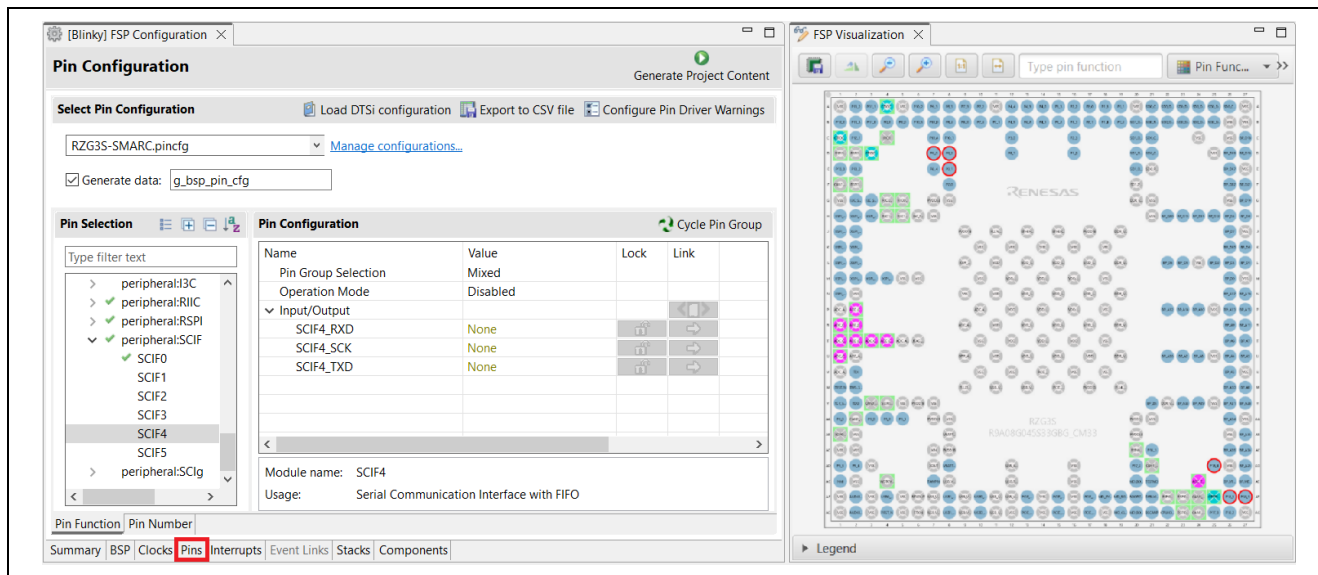


Figure 106. Pin Configuration

The pin configurator includes a built-in conflict checker. So, if the same pin is allocated to another peripheral or I/O function, the pin will be shown as red in the **FSP Visualization** view and with a white cross in a red square in the **Pin Selection** pane and **Pin Configuration** pane in the main **Pins** tab.

In the example shown below, port P13_1 is already used by the GPT, and the attempt to connect this pin to the Serial Communication Interface with FIFO (SCIF) results in a dangling connection error. To fix this error, select another port from the pin drop-down list or disable the GPT.

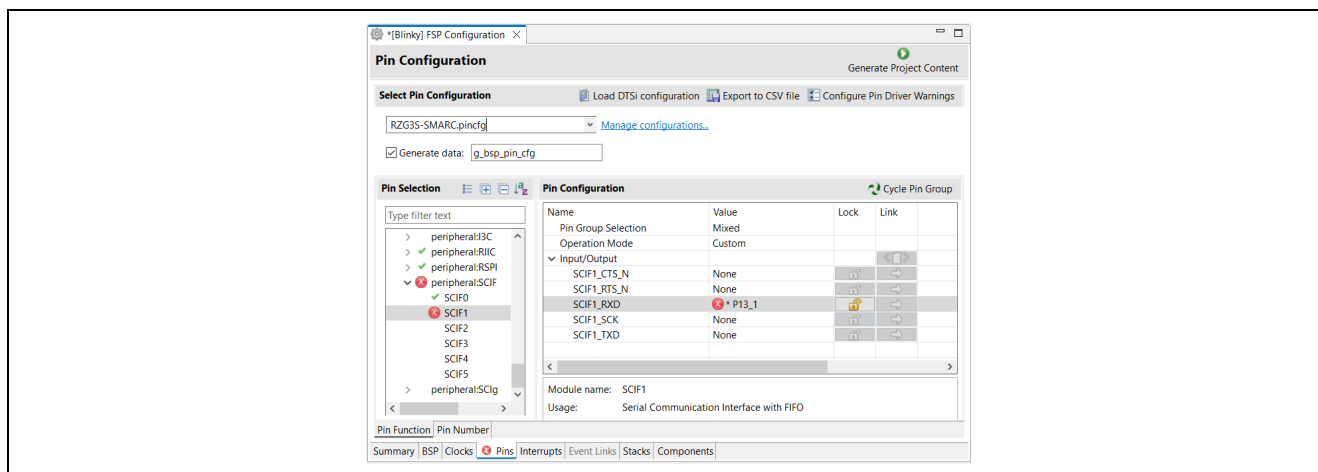


Figure 107. e2 studio Pin Configurator

When you click the **[Generate Project Content]** button, the pin configuration contents are written to: rz_gen\pin_data.c. This file will be created if it does not already exist.

Warning: Do not edit this file as it is overwritten whenever the **[Generate Project Content]** button is clicked.

In the case of versions earlier than RZ/G FSP v2.0.0, it does not support the Pins tab, and if the user would like to use the I/O port, the I/O Port setting should be applied to "src\pin_data.c" manually. For details on the

I/O Port setting and how to apply the setting of “src/pin_data.c” to the **Pins** tab, please refer to [Setting GPIO with Flexible Software Package](#).

5.2.5 Configuring Interrupts from the Stacks Tab

You can use the **Properties** view in the **Stacks** tab to enable interrupts by setting the interrupt priority. Select the driver in the **Stacks** pane to view and edit its properties.

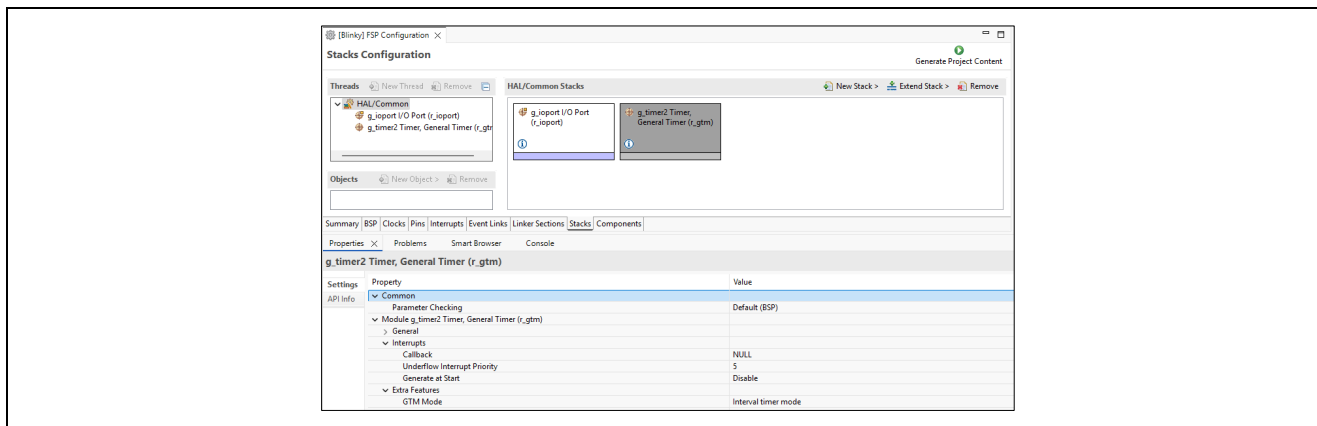


Figure 108. Configuring Interrupts in the Stacks tab

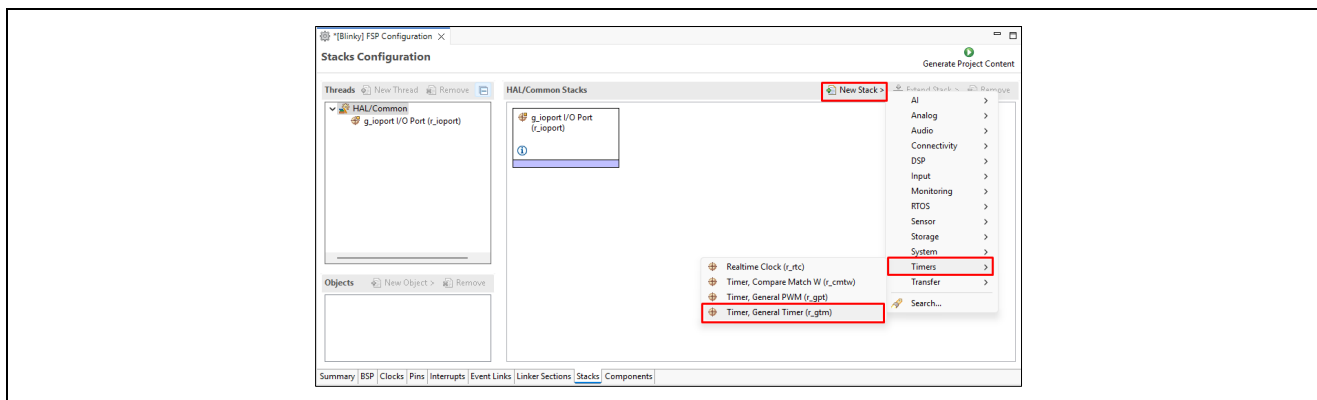


Figure 109. Add new stack Timer (GTM)

5.2.6 Creating Interrupts from the Interrupts Tab

On the **Interrupts** tab, the interrupts of the driver that the user selected in the **Stacks** tab are registered.

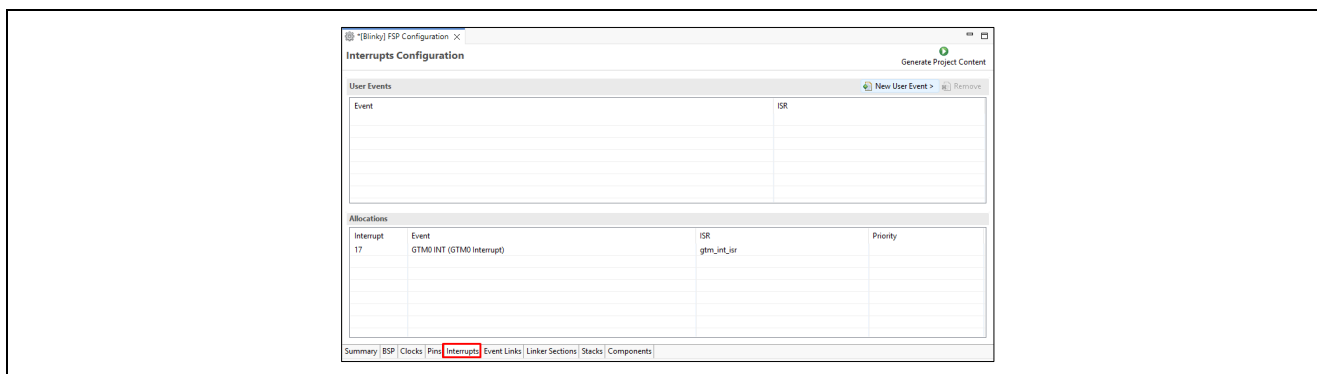


Figure 110. Configuring an interrupt in the Interrupt Tab

Also, on the **Interrupts** tab, the user can add their own peripheral interrupts. This can be achieved by adding a new event via the **[New User Event]** button.

5.2.7 Viewing Event Links

The **Event Links** tab can be used to view the Event Link Controller events. The events are sorted by peripheral to make it easy to find and verify them.

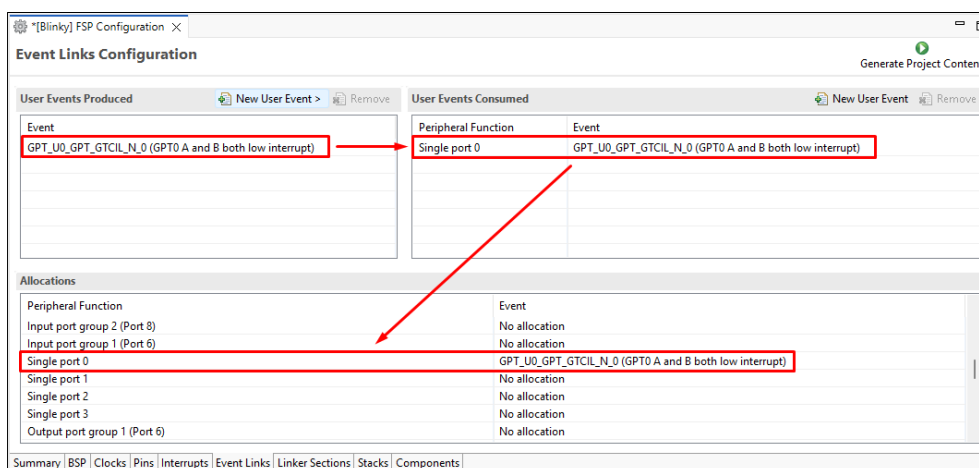


Figure 111. e2 studio Project configurator – Viewing Event Links

Like the Interrupts tab, user-defined event sources and destinations (producers and consumers) can be defined by clicking the relevant **[New User Event]** button. Once a consumer is linked to a producer, the link will appear in the Allocations section at the bottom.

Note 1: When selecting an ELC event to receive for a module (or when manually defining an event link), only the events that are made available by the modules configured in the project will be shown.

Note 2: RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/G3S, and RZ/G3L don't support the **Event Links** tab.

5.2.8 Adding and Configuring HAL Drivers

For applications that run outside or without the RTOS, you can add additional HAL drivers to your application using the HAL/Common thread. To add drivers, follow these steps:

1. Click on the **HAL/Common** icon in the **Stacks** pane. The Modules pane changes to **HAL/Common Stacks**.
2. Click **New Stack** to see a drop-down list of HAL-level drivers available in the FSP.
3. Select a driver from the menu **New Stack > Timer > Timer, General Timer (r_gtm)**.

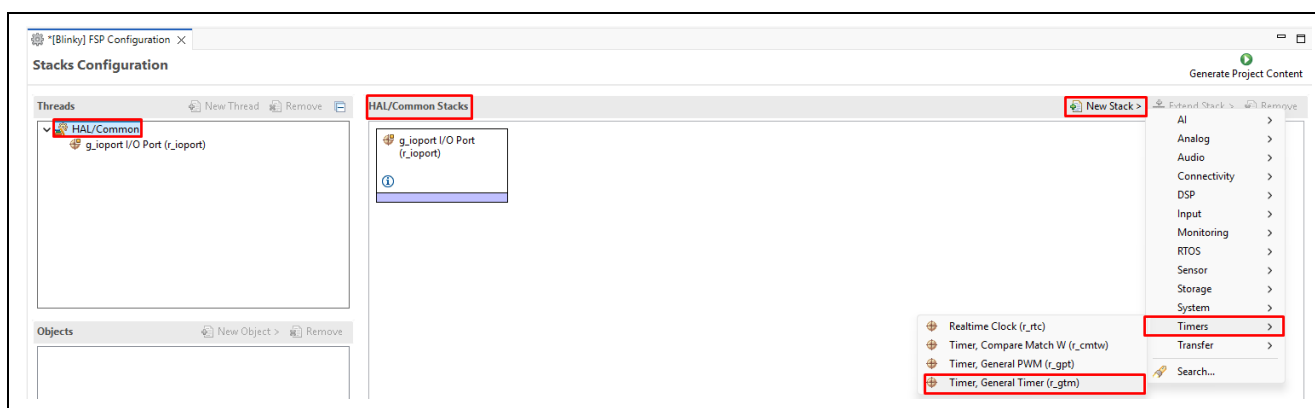


Figure 112. e2 studio Project configurator - Adding drivers

4. Select the driver module in the **HAL/Common Stacks** pane and configure the driver properties in the **Properties** view.

e2 studio adds the following files when you click the **[Generate Project Content]** button:

- The selected driver module and its files to the rz/fsp directory
- The main() function and configuration structures and header files for your application as shown in the table below.

File	Contents	Overwritten by Generate Project Content?
rz_gen/main.c	Contains main() calling generated and user code. When called, the BSP has already initialized the MPU.	Yes
rz_gen/hal_data.c	Configuration structures for HAL Driver only modules.	Yes
rz_gen/hal_data.h	Header file for HAL driver only modules.	Yes
src/hal_entry.c	User entry point for HAL Driver only code. Add your code here.	No

The configuration header files for all included modules are created or overwritten in this folder: rz_cfg/fsp_cfg

5.3 Reviewing and Adding Components

The **Components** tab enables the individual modules required by the application to be included or excluded. Modules common to all RZ/G MPU projects are preselected. All modules that are necessary for the modules selected in the **Stacks** tab are included automatically. You can include or exclude additional modules by ticking the box next to the required component.

Component	Version	Description	Variant
- BSP - Renesas - BSP - Board - custom - custom - custom - custom - custom - custom - custom - custom - custom_ddr - custom_octal_xip - custom_qspi_xip - rza3m_ek_nand - rza3m_ek_nor - rza3ul_smarc_octal_xip - rza3ul_smarc_qspi - rza3ul_smarc_qspi_xip - rzg2l_smarc - rzg2lc_smarc - rzg2ul_smarc - rzg3e_evk - rzg3e_evk_ca55clockup - rzg3e_evk_cm33coldboot - rzg3l_evk - rzg3l_evk_cm33coldboot - rzg3l_evk_tfboot - rzg3s_smarc - rnz2_custom		Custom Board Support Files for RZ/G2L Custom Board Support Files for RZ/G2UL Custom Board Support Files for RZ/G3S Custom Board Support Files for RZ/G3E Custom Board Support Files for RZ/G3L Custom Board Support Files for RZ/V2L Custom Board Support Files for RZ/V2H Custom Board Support Files for RZ/V2N Custom User Board QSPI Boot(Exec with DDR SDRAM) Support Files Custom Board OCTAL Boot (eXecute-In-Place) Support Files Custom Board QSPI Boot (eXecute-In-Place) Support Files RZ/A3M Evaluation Board NAND Boot (Exec with DDR SDRAM) Board Support Files RZ/A3M Evaluation Board NOR Boot (Exec with DDR SDRAM) Board Support Files RZ/A3UL Evaluation Board Kit OCTAL Edition (eXecute-In-Place) Board Support Files RZ/A3UL Evaluation Board Kit QSPI Edition (Exec with DDR SDRAM) Board Support Files RZ/A3UL Evaluation Board Kit QSPI Edition (eXecute-In-Place) Board Support Files Evaluation Kit RZ/G2L Support Files (RZ/G2L) Evaluation Kit RZ/G2LC Support Files (RZ/G2LC) Evaluation Kit RZ/G2L Support Files (RZ/G2UL) RZ/G3E SMARC Evaluation Board Kit Support Files (RZ/G3E) RZ/G3E SMARC Evaluation Board Kit Support Files (RZ/G3E) for Cortex-A55 clockup dur... RZ/G3E SMARC Evaluation Board Kit Support Files (RZ/G3E) for Cortex-M33 cold boot RZ/G3L SMARC Evaluation Board Kit Support Files (RZ/G3L) RZ/G3L SMARC Evaluation Board Kit Support Files (RZ/G3L) for Cortex-M33 cold boot RZ/G3L SMARC Evaluation Board Kit Support Files (RZ/G3L) for booting from TF-A on C... Evaluation Kit RZ/G3S Support Files (RZ/G3S) RZN Custom Board Support Files (xSPI0 x1 boot mode)	rzg2l rzg2ul rzg3s rzg3e rzg3l rvz2l rzv2h rzv2n
- Component - BSP - Board - rza3m - rza3ul - rzg2l - rzg2ul - rzg3e - device - device - device - device - device - device - device - device - fsp - rzg3l - rzg3s - rnz - rnz2h - rnz2l - rt - rt2h - rt2l - rt2m - rt2me - rt2n - rv2h - rv2l - rv2n - Common - all - fsp_common - rza - rzg		Board support package for R9A09G047E57GBG Board support package for RZG3E Board support package for R9A09G047E28GBG Board support package for R9A09G047E38GBG Board support package for R9A09G047E48GBG Board support package for R9A09G047E58GBG Board support package for R9A09G047E27GBG Board support package for R9A09G047E37GBG Board support package for R9A09G047E47GBG Board support package for RZ/G3E - FSP Data	R9A09G047E57GBG R9A09G047E28GBG R9A09G047E38GBG R9A09G047E48GBG R9A09G047E58GBG R9A09G047E27GBG R9A09G047E37GBG R9A09G047E47GBG
- Component - HAL Drivers - rza - rzg - r_adc_c - r_adc_e - r_canfd - r_cmtw - r_crc - r_dmac_b - r_elc - r_gpt - r_gtm - r_i3c_b - r_intc_irq - r_intc_nmi - r_intc_tint - r_ioport - r_lcd - r_mhu_b_ns - r_mhu_b_ns_swint_get		A/D Converter A/D Converter Controller Area Network - Flexible Data Compare Match Timer W Cyclic Redundancy Check Direct Memory Access Controller Event Link Controller General PWM Timer General Timer I3C External INT (IRQ) External INT (NMI) External INT (TINT) I/O Port LCD Controller Message Handler Unit (NonSecure) Message Handler Unit Software Interrupt Get	

Figure 113. Components Tab

Clicking the **Generate Project Content** button copies the .c and .h files for each selected component into the following folders:

- rz/fsp/inc/api
- rz/fsp/inc/instances
- rz/fsp/src/bsp
- rz/fsp/src/<Driver_Name>

e² studio also creates configuration files in the rz_cfg/fsp_cfg folder with configuration options set in the **Stacks** tab.

Debugging the Project

Once your project builds without errors, you can use the Debugger to download your application to the board and execute it.

To debug an application, follow these steps:

1. On the drop-down list next to the debug icon, select **Debug Configurations**.

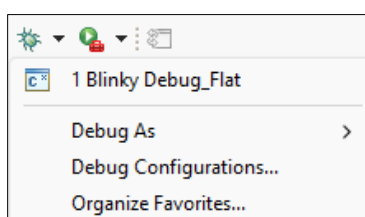


Figure 114. Debug Configuration selection

2. In the **Debug Configurations** view, click on your project listed as **MyProject Debug**.

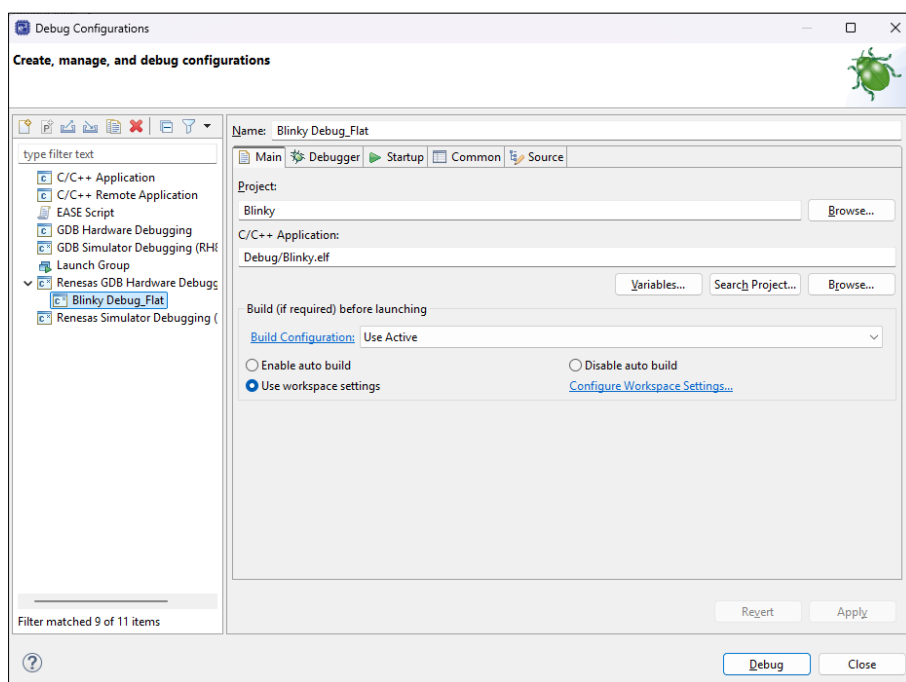


Figure 115. Debug Configuration

3. **Secure Vector Address** and **Non-secure Vector Address** are configured in the **Connection Settings** tab of the **Debugger** tab. The settings in the image below are for setting the addresses of the Secure and Non-secure Vector Offset mapped in the Blinky project. Please note that these addresses vary in accordance with linker settings.

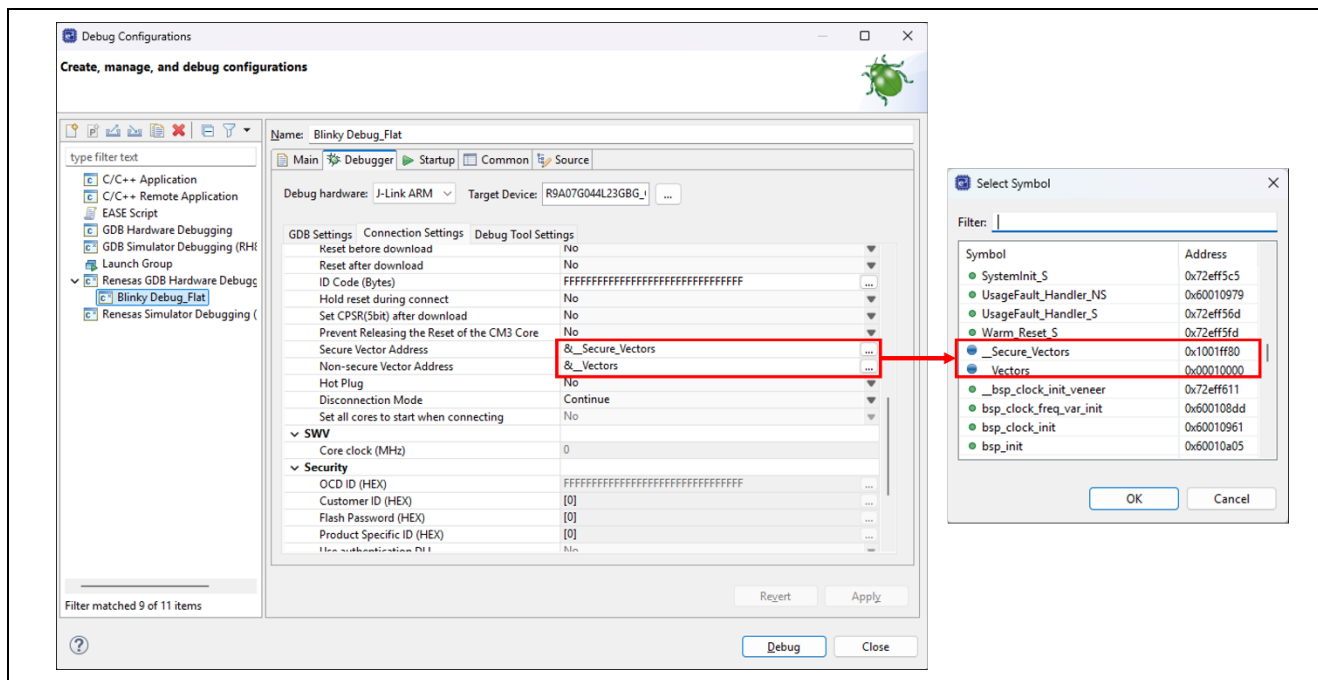


Figure 116. Secure and Non-secure vector addresses configuration

4. Connect the board to your PC via a standalone Segger J-Link debugger and click the **[Debug]** button.

Note: For details on using J-Link and connecting the board to the PC, see 3.1.2.2.JTAG connection.

5.5 Modifying Toolchain Settings

There are instances where it may be necessary to make changes to the toolchain being used (for example, to change the optimization level of the compiler or add a library to the linker). Such modifications can be made within e² studio through the menu **Project > Properties > C/C++ Build > Settings** when the project is selected. The following screenshot shows the settings dialog for the GNU Arm toolchain. This dialog will look slightly different depending on the toolchain being used.

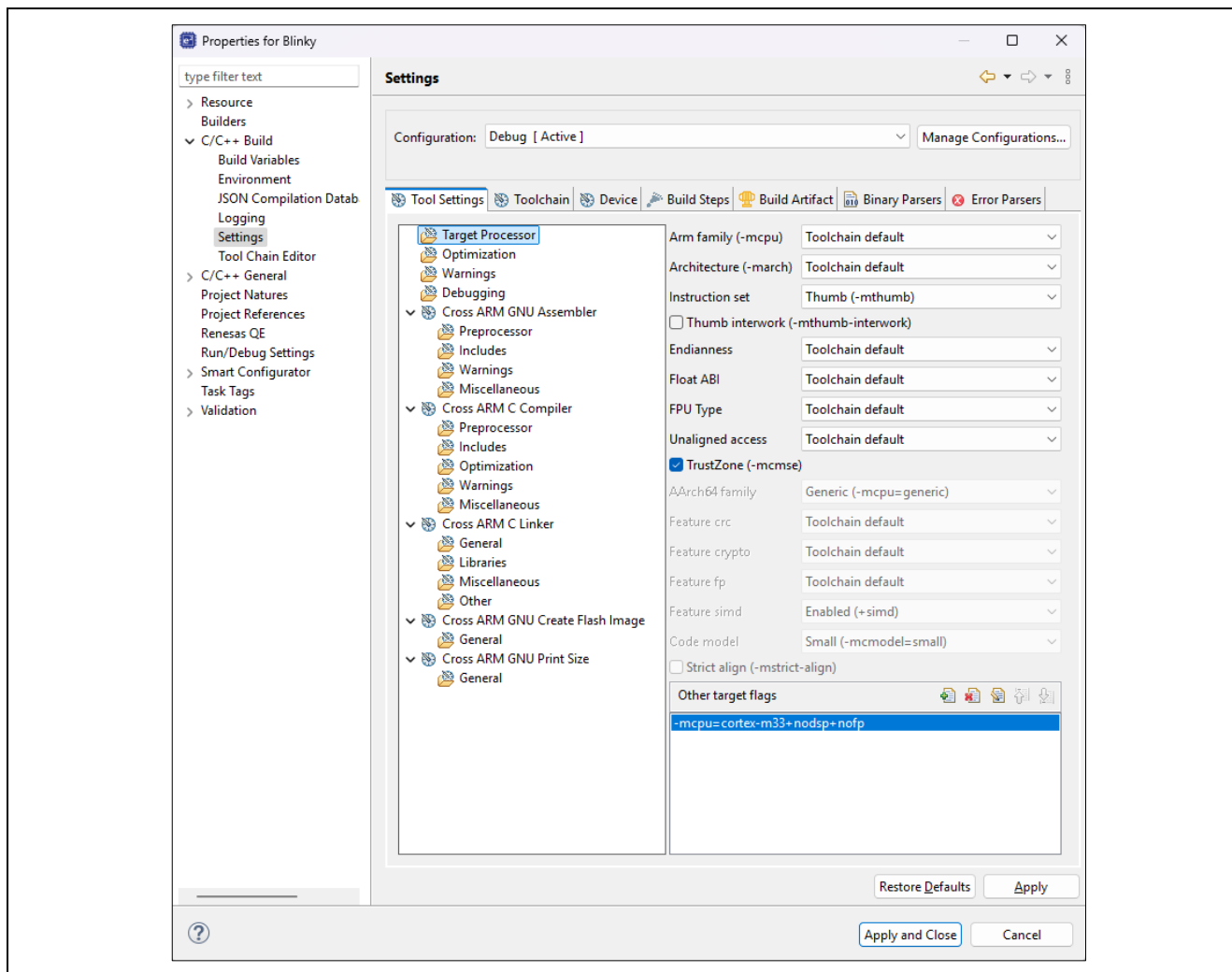


Figure 117. e² studio Project toolchain settings

The scope for the settings is project scope, which means that the settings are valid only for the project being modified.

The settings for the linker, which control the location of the various memory sections, are contained in a script file specific to the device being used. This script file is included in the project when it is created and is found in the created project. (for example, script/fsp.ld).

5.6 Importing an Existing Project into e² studio

1. Start by opening e² studio.
2. Open an existing Workspace to import the project and skip to step 5. If the workspace does not exist, proceed with the following steps:

At the end of the e² studio startup, you will see the Workspace Launcher Dialog box as shown in the following figure.

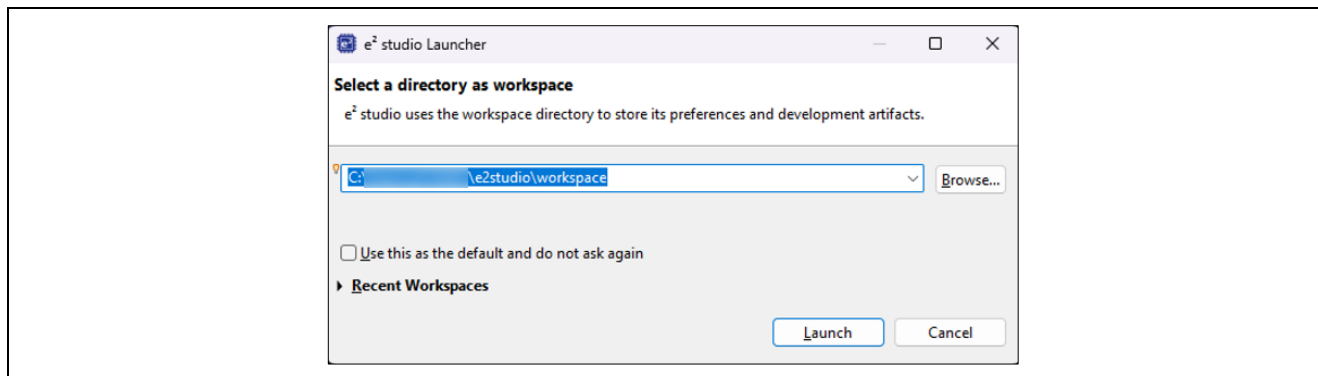


Figure 118. Workspace Launcher dialog

Enter a new workspace name in the Workspace Launcher Dialog as shown in the following figure. e² studio creates a new workspace with this name.

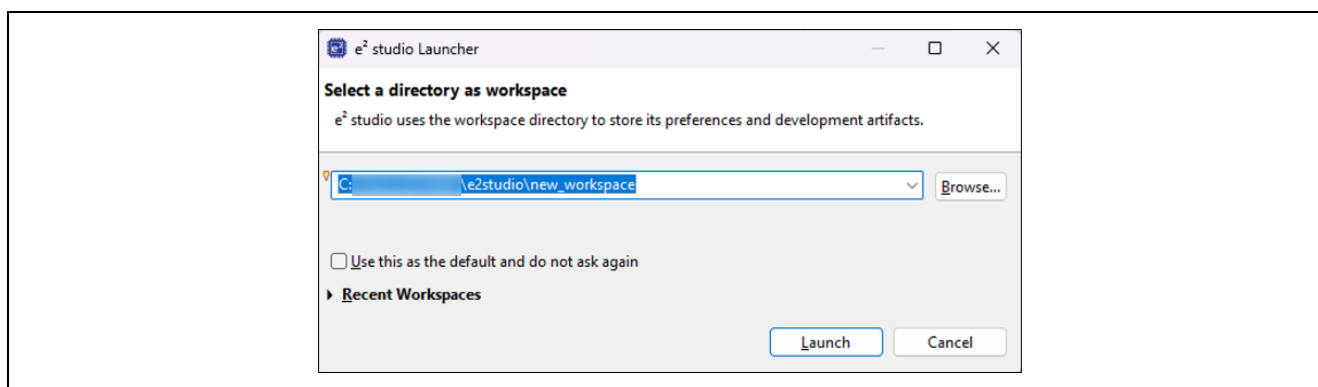


Figure 119. Workspace Launcher dialog - Select Workspace

Click the **[Launch]** button.

When the workspace is opened, you may see the Welcome Window. Click on the **Workbench** arrow button to proceed past the Welcome Screen, as seen in the following figure.

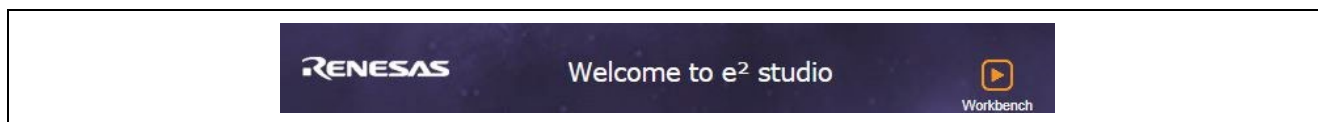


Figure 120. Workbench arrow button

5. You are now in the workspace that you want to import the project into. Click the **File** menu in the menu bar, as shown in the following figure.

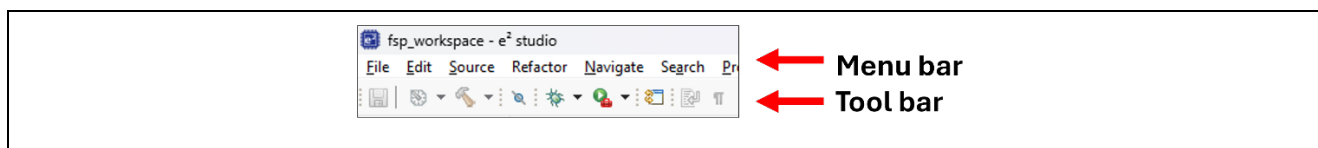


Figure 121. Menu and toolbar

- Click **Import** on the **File** menu or "Import project" on Project Explorer, as shown in the following figure.

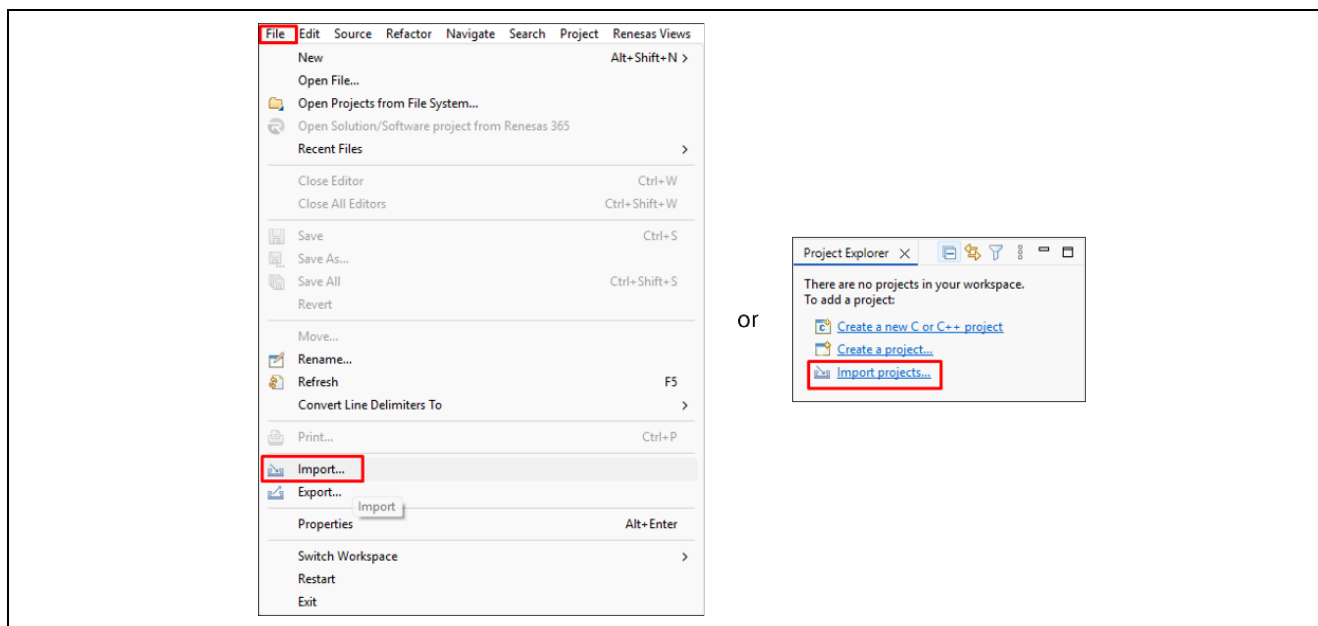


Figure 122. File drop-down menu

- In the **Import** dialog box, as shown in the following figure, choose the **General** option, then **Existing Projects into Workspace**, to import the project into the current workspace.

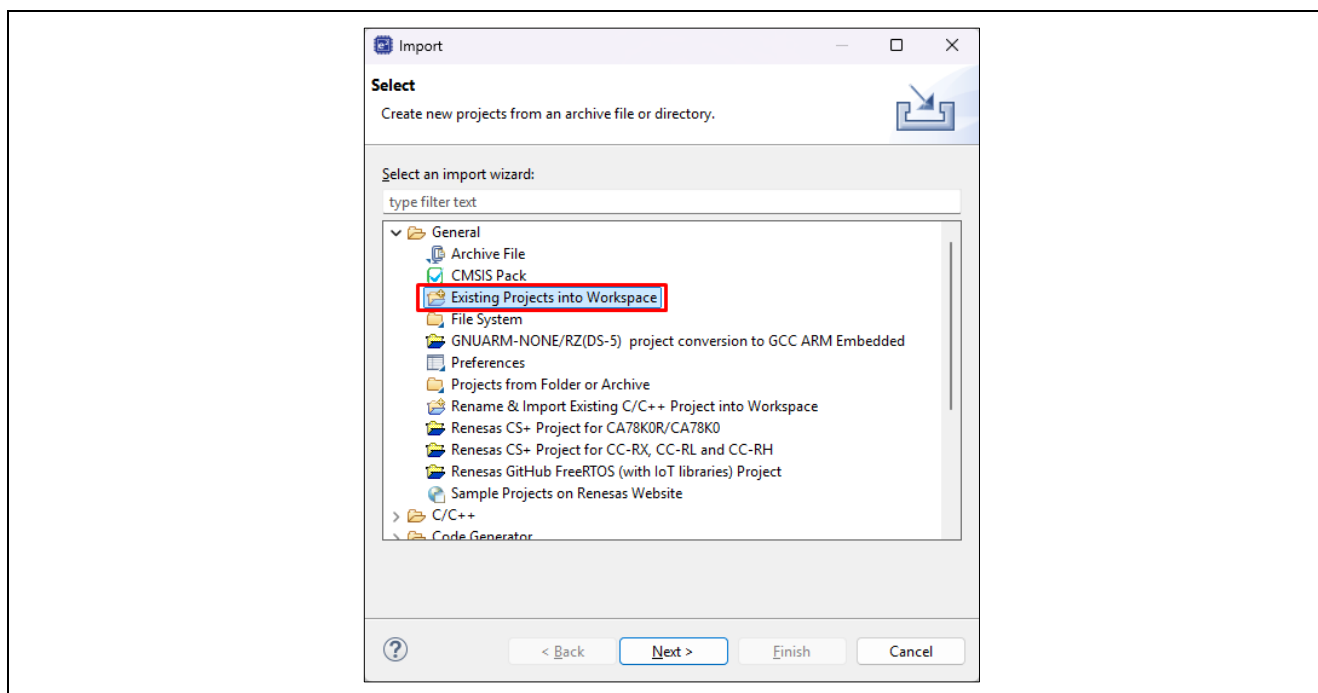


Figure 123. Project Import dialog with "Existing Projects into Workspace" option selected

8. Click the **[Next >]** button.
9. To import the project, use either Select archive file or Select root directory.
 - a. Click **Select root directory** file as shown in the following figure.

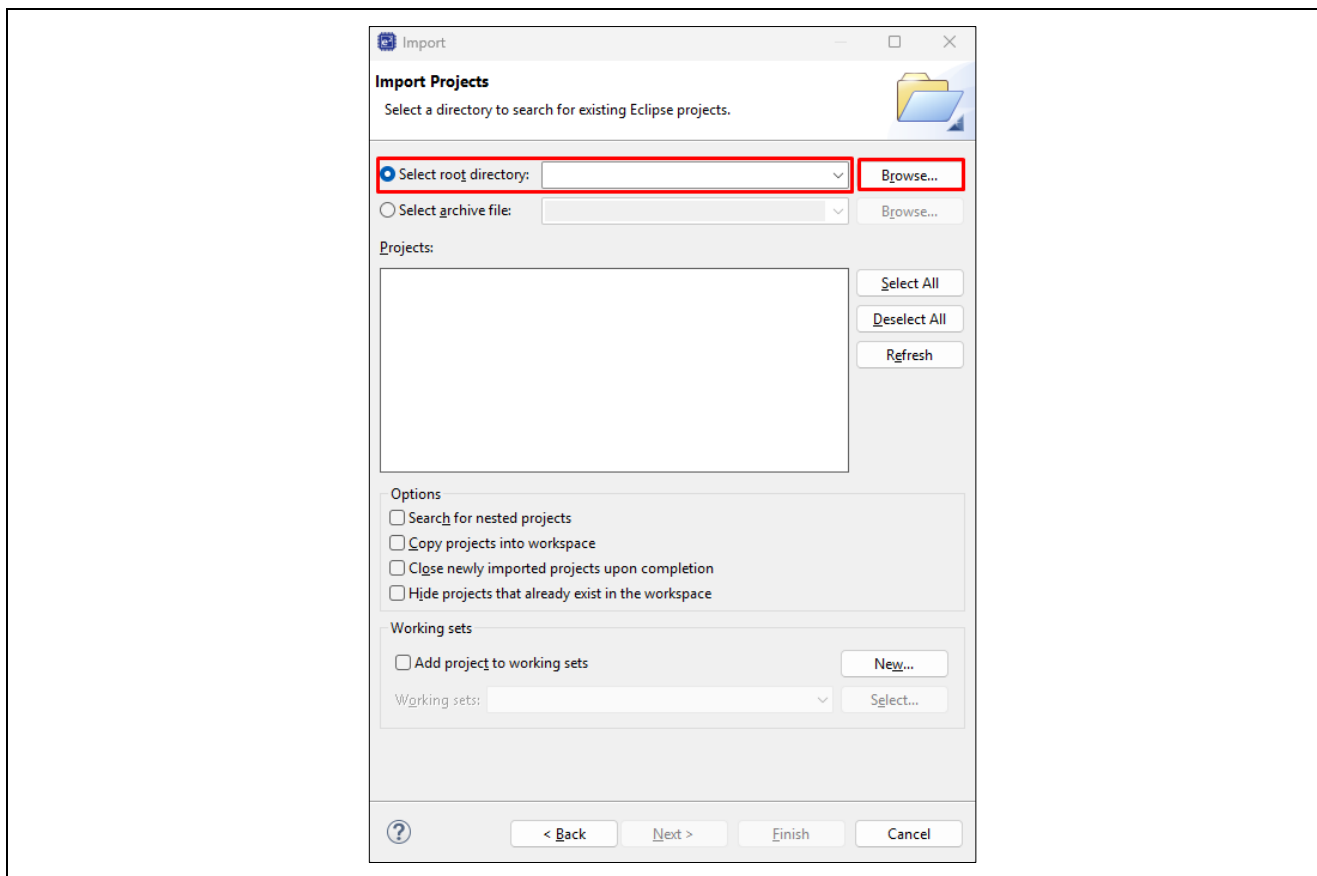


Figure 124. Import Existing Project dialog 1 - Select root directory

- b. Click the [Browse] button.
- c. For Select root directory, browse to the project folder that you want to import.
- d. Select the file for import.
- e. Click the [Open] button.
- f. Select the project to import from the list of Projects, as shown in the following figure.

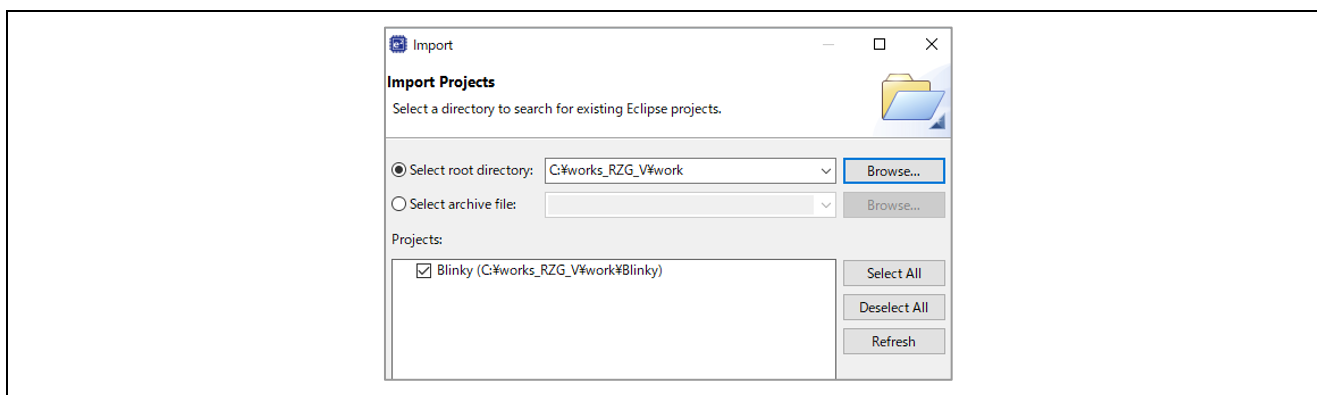


Figure 125. Import Existing Project dialog 2

10. Click the **[Finish]** button to import the project.

Revision History

Rev	Date	Page	Summary
4.2.0	Aug.11.26	5 to 12, 15 8 to 21	Updated e ² studio to version 2026-07, replaced outdated and low-resolution figures Updated FSP to version 4.2.0
		37 to 41 43	Added new chapter 3.4 RZ/G3L SMARK EVK Updated image and information for RZ/G3L in document
		44 to 57	Updated outdated Blinky creation project image
		58 to 78	Updated outdated FSP application launch with e2studio image
4.1.0	May.20.26	18, 20, 21	Updated FSP to version 4.1.0.
		12	Updated e ² studio to version 2026-04.01.
4.0.0	Jan.30.26	-	Updated the description and figure based on the latest development environment.
3.1.0	Jul.22.25	40, 46 to 50,	Added the description for the template of the RZ/G3E CM33 cold boot Added the description of how to debug the RZ/G3S CM33 and CM33_FPU at the same time. Added the description of whether a project is bundled with another project when creating a new project.
3.0.0	Mar.31.25	4 to 20, 31 to 35, 37 to 40, 46, 48, 50 to 52, 56	Updated the description and figure based on the latest development environment.
2.1.0	Sep.30.24	6 to 11, 13 to 22, 35 to 36, 42,44, 46,48, 59 to 67	Updated the description and figure based on the latest development environment.
2.01	Feb.13.24	6 to 11, 13 to 22,	Updated the description and figure based on the latest development environment.
		45	Updated the description of project creation.
		48	Added the section on how to avoid resource duplication in the case of RZ/G3S project creation.
		60 to 69	Added the section on how to migrate the project from the previous FSP version to the latest FSP version.
2.00	Jan.9.24	1	Added RZ/G3S to the target device.
		5	Updated the description of the RAM initialization section.
		6 to 11	Updated the description and figure based on the latest development environment.
		12 to 22	Updated the development setup for Linux Host PC and FSP installation.
		26 to 32	Added description and figure for RZ/G3S SMARC EVK.
		33 to 36	Updated the description and figure based on the latest development environment.
		40	Removed the steps to configure Secure Vector and Non-secure Vector from the Debug step.
		46 to 51 55	Added a description about the Pins and Clocks tabs. Updated the instructions for configuring Secure Vector and Non-secure Vector.
1.20	Nov.30.22	12	Updated version information of the SEGGER J-Link driver and Libgen Update for GNU ARM Embedded Toolchains.
		19, 24	Updated installation procedure for FSP packs.
		74	Updated the method of specifying Secure Vector Address and Non-secure Vector Address.
1.10	Apr.27.22	5 to 53	Updated the description and figure based on the latest development environment.
1.01	Dec.3.21	14 to 22	Added a section on e ² studio installation for Linux PC.

1.00	Jul.30.21	-	First Edition issued.
------	-----------	---	-----------------------

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.