RX24U Group

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Disabling and Restoring PWM Output Using POE3A and MTU3d

Summary

This application note describes procedures for disabling and restoring PWM output using the port output enable 3 (POE3A) and multi-function timer pulse unit 3 (MTU3d) modules on the RX24U Group. This functionality can be used as a fail-safe for controlling PWM output when an error is detected.

Target Device

RX24U Group

Contents

1. Specifications

This application note describes procedures for disabling and restoring PWM output using the port output enable 3 (POE3A) and multi-function timer pulse unit 3 (MTU3d) modules on the RX24U Group.

- The MTU3d outputs a total of six waveforms in complementary PWM mode 1: three positive-phase and three negative-phase waveforms with 50% duty, a period of 100 µs, and dead time of 2 µs.
- When one of the output disable sources (input level detect, output level compare, register setting, comparator output detect, or oscillation stop detect) shown in Figure 1.1, System Overview Diagram, is detected, the PWM output pin enters the Hi-Z state.
- After the output disable source is removed, the PWM output state can be restored by clearing to 0 the POE3A flag corresponding to the disable source. However, when output is disabled due to oscillation stop detection, the system must be reset to restore the PWM output state.

Figure 1.1 is a System Overview Diagram. The pins used are listed in Table 3.1, Pins Used and Their Functions, and the operation of the software is described in 4.1, Operation Overview.

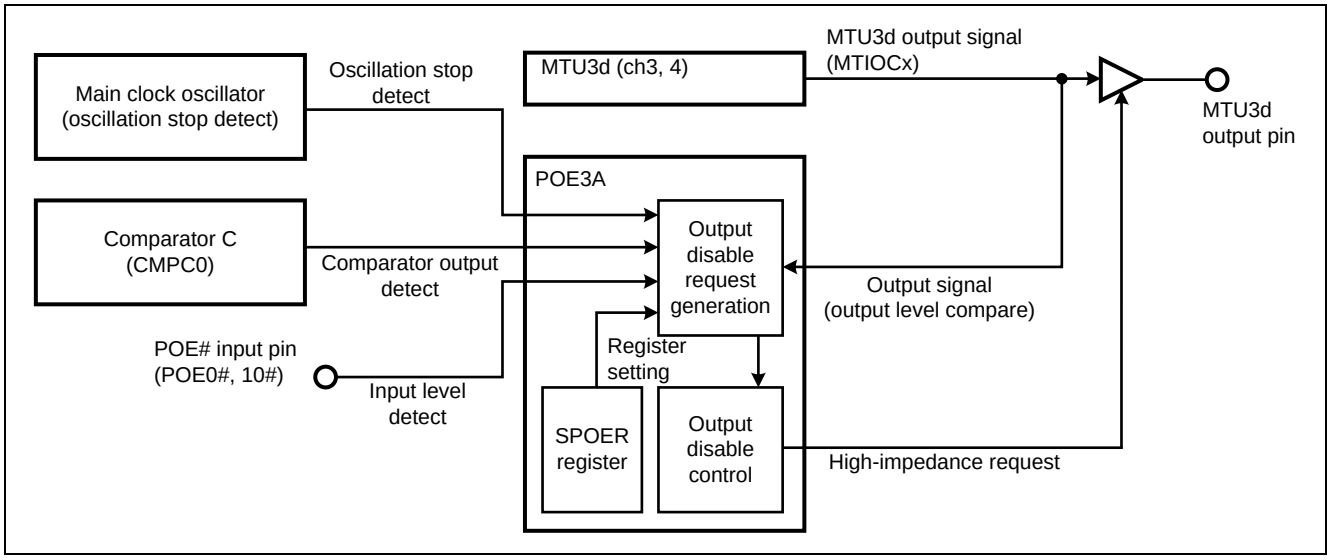


Figure 1.1 System Overview Diagram

2. Operation Confirmation Conditions

The operation of the sample code described in this application note has been confirmed under the conditions listed in Table 2.1.

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	R5F524UEADFB (RX24U Group)
Operating frequency	Main clock: 20 MHz Low-speed on-chip oscillator (LOCO): 4 MHz PLL: 80 MHz (main clock divided by 2 and multiplied by 8) System clock (ICLK): 80 MHz (PLL clock frequency divided by 1) Peripheral module clock (PCLKA): 80 MHz (PLL clock frequency divided by 1) Peripheral module clock (PCLKB): 40 MHz (PLL clock frequency divided by 2)
Operating voltage	5.0 V
Integrated development environment	Renesas electronics e^2 studio V.6.2.0
C compiler	Renesas electronics C/C++ Compiler Package for RX Family V.2.08.00
	Compiler option The integrated development environment default settings are used.
iodefine.h version	1.0H
Code generator plugin version	1.03.00.04
Endian order	Little-endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	1.00
Board used	Renesas Starter Kit for RX24U (Product No.: RTK500524UC00000BE)

3. Hardware

3.1 Hardware Configuration Example

Figure 3.1 shows an example hardware configuration. The sample code described in this application note uses the Renesas Starter Kit for RX24U. Circuit illustrations have been omitted to provide a simplified overview of connections. When designing actual circuits, make sure to provide appropriate pin processing and ensure that the electrical characteristics are satisfied.

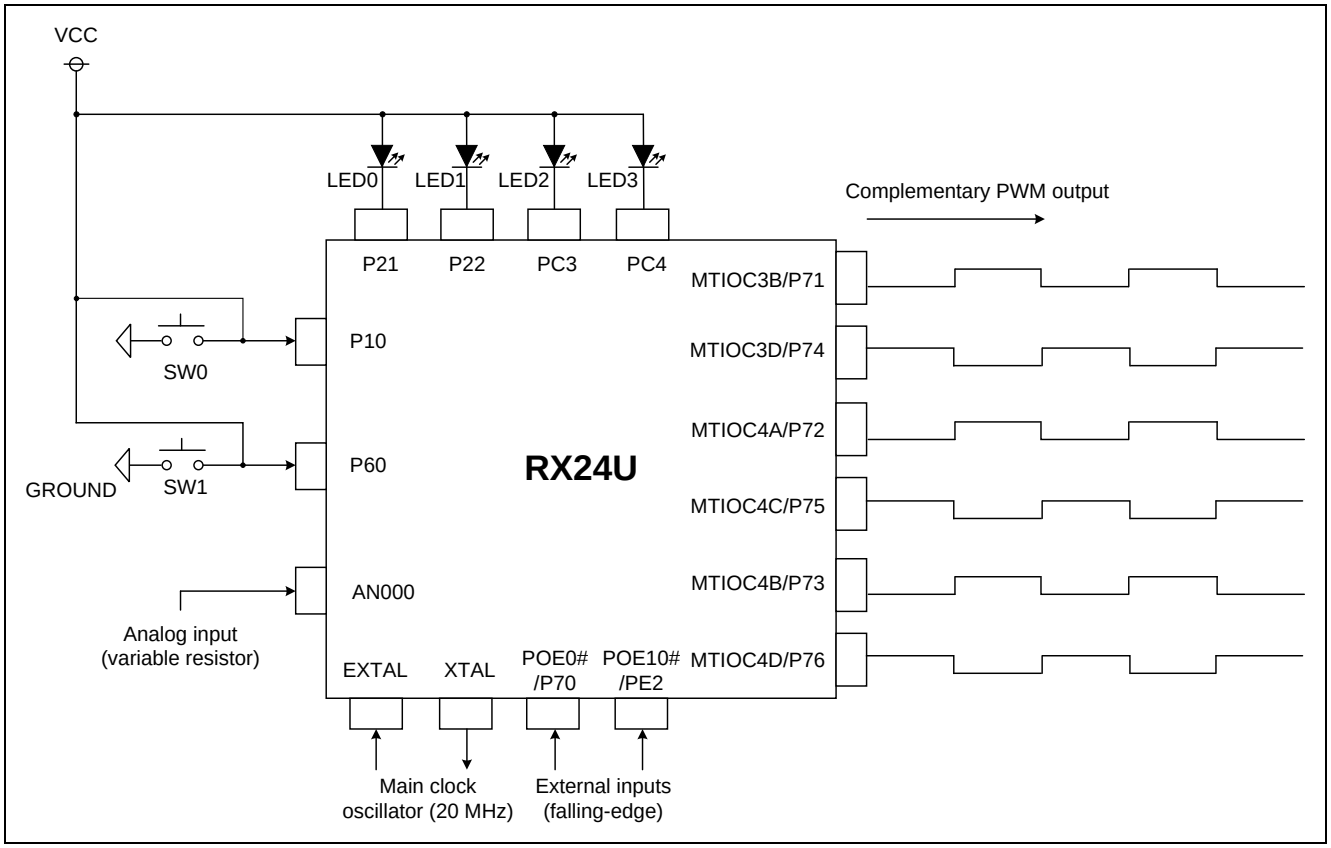


Figure 3.1 Hardware Configuration Example

3.2 List of Pins Used

Table 3.1 lists the pins used and their functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Description
P21, P22, PC3, PC4	Output	LEDs indicating PWM output disabled state (LED0, LED1, LED2, and LED3)
P10	Input	Transition switch to PWM output restored state (SW0)
P60	Input	Switch (SW1) for disabling output using SPOER register
P70/POE0#	Input	POE3A input pin
PE2/POE10#	Input	POE3A input pin (added condition)
P71/MTIOC3B	Output	PWM output pin 1
P72/MTIOC4A	Output	PWM output pin 2
P73/MTIOC4B	Output	PWM output pin 3
P74/MTIOC3D	Output	PWM output pin 1' (PWM output 1 negative-phase waveform output)
P75/MTIOC4C	Output	PWM output pin 2' (PWM output 2 negative-phase waveform output)
P76/MTIOC4D	Output	PWM output pin 3' (PWM output 3 negative-phase waveform output)
P40/AN000	Input	Analog input pin
P36/EXTAL	Output	Oscillator connection pin
P37/XTAL	Input	Oscillator connection pin

4. Software

This application note uses the code generator plugin to make initial settings to the modules used. Refer to 4.3, Code Generator Plugin Setting Items, for the code generator plugin setting values. Refer to 4.1, Operation Overview, and 4.10, Flowcharts, for an explanation of how the software operates.

4.1 Operation Overview

- The MTU3d outputs a total of six waveforms in complementary PWM mode 1: three positive-phase and three negative-phase waveforms with 50% duty, a period of 100 µs, and dead time of 2 µs.
- When an output disable source is detected, the PWM output pin enters the Hi-Z state.
- The MTU module is disabled at the start of the interrupt handler corresponding to the output disable source.
- The LEDs that show the operating state display a different illumination pattern for each output disable source. If multiple output disable sources occur, the LED illumination pattern is that of the last output disable source generated.
- If the output disable source has been removed, pressing SW0 causes the flag corresponding to the output disable source to be cleared to 0, after which the MTU is initialized and operation starts, restoring the PWM output state. In addition, all the LEDs turn off. However, when output is disabled due to oscillation stop detection, the system must be reset to restore the PWM output state.
- If the output disable source remains and restore is not possible, LED3 lights. In this case, the flag corresponding to the output disable source remains set to 1, and the MTU remains in the disabled state.

Sections 4.1.1 to 4.1.5 describe the operation corresponding to each output disable source in the program described in this application note. Table 3.1 lists the pins used and their functions, and Table 4.1 lists the LED illumination patterns corresponding to the various operating states. Figure 4.1 to Figure 4.5 show timing charts for each output disable source. Note that these timing charts do not take dead time into account.

Table 4.1 LED Illumination Patterns

Item			LED Illumination Pattern			
			P21	P22	PC3	PC4
PWM output state			×	×	×	×
PWM output disabled state	Input level detect	POE0#	◯	×	×	—
		POE10#	×	◯	×	—
	Output level compare		◯	◯	×	—
	Output control by register		×	×	◯	—
	Comparator output detect		◯	×	◯	—
	Oscillation stop detect		×	◯	◯	—
Restored state (after SW0 pressed)	Successful restore		×	×	×	×
	Restore not possible		—	—	—	◯

◯: on, ×: off, —: previous state maintained

4.1.1 Output Control by Input Level Detect

When PWM output is restored from the disabled state, note that if a low-level signal is being input on pin POE0# or POE10#, the falling-edge, which is the input level detect (falling-edge) output disable source, does not occur, and switching once again to the PWM output disabled state does not take place, even if the POE0 or POE10 flag (POE0F or POE10F) has been cleared. For details, refer to RX24U Group User's Manual: Hardware, which is listed in the Reference Documents section.

In the program described in this application note, output disable control by register setting is enabled as part of output restore control in order to deal with the issue described above.

An output control operation example using input level detection (falling-edge detection) is described below.

- Output disable control
  - When the input on the POE0# or POE10# pin changes from high- to low-level, the value of the output disable request flag (ICSR1.POE0F or ICSR4.POE10F) changes to 1.
  - The PWM output pin enters the Hi-Z state.
  - Since level detection is used for output enable interrupt 1 (OEI1) and output enable interrupt 4 (OEI4), the interrupts of the corresponding output disable sources are disabled by the interrupt handler.
  - The LEDs illuminate as indicated in Table 4.1, LED Illumination Patterns.
- Output restore control
  - The SPOER.MTUCH34HIZ bit is set to 1 to perform PWM output disable control.
  - The POE0F or POE10F bit is cleared to 0.
  - When the SPOER.MTUCH34HIZ bit is cleared to 0 while a high-level signal is being input on pin POE0# or POE10#, the PWM output state is restored.
  - The interrupts of the corresponding output disable sources are enabled.
  - The LEDs turn off, indicating the output disabled state.

Table 4.2 lists the output disable timing using input level detect (falling-edge), and Figure 4.1 shows an output disable example (falling-edge) using input level detect. Note that since sampling is performed once each PCLK period when the output disable source setting is changed to input level detect (low-level detect), the number of cycles corresponding to the sample count are added to the duration from input level detection to output disable.

Table 4.2 Output Disable Timing Using Input Level Detect (Falling-Edge)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Max.	Unit
Output disable by input level detect	t_0	—	7.5*1	t_{PBcyc}*2

Note 1. This is a reference valve. Make sure to perform careful evaluation on your system.

Note 2. t_{PBcyc}: PCLKB period

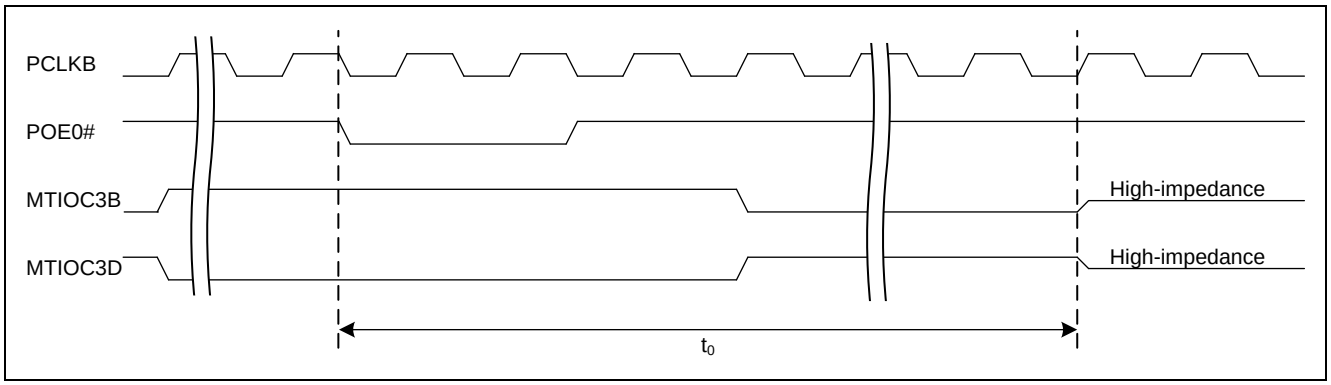


Figure 4.1 Output Disable Example (Falling-Edge) Using Input Level Detect

4.1.2 Output Control by Output Level Compare

The output-shorted pins used by the program described in this application note are MTIOC3B and MTIOC3D, MTIOC4A and MTIOC4C, and MTIOC4B and MTIOC4D. Their active level is set to low.

An output control operation example using output level comparison is described below.

- Output disable control
  - If the output-shorted pins are both at their active level for one PCLKB cycle or more, the value of the simultaneous conduction flag (OCSR1.OSF1) changes to 1.
  - The PWM output pin enters the Hi-Z state.
  - Since level detection is used for output enable interrupt 1 (OEI1), the interrupt of the corresponding output disable source is disabled by the interrupt handler.
  - The LEDs illuminate as indicated in Table 4.1, LED Illumination Patterns.
- Output restore control
  - The OCSR1.OSF1 bit is cleared, restoring the PWM output state.
  - The interrupt of the corresponding output disable source is enabled.
  - The LEDs turn off, indicating the output disabled state.

Table 4.3 lists the output disable timing using output level compare, and Figure 4.2 shows an output disable example (active level: low) using output level compare.

Table 4.3 Output Disable Timing Using Output Level Compare

Conditions: VCC = 2.7 V to 5.5V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Max.	Unit
Output disable by output level compare	t_1	—	4*1	t_{PBcyc}*2

Note 1. This is a reference valve. Make sure to perform careful evaluation on your system.
Note 2. t_{PBcyc}: PCLKB period

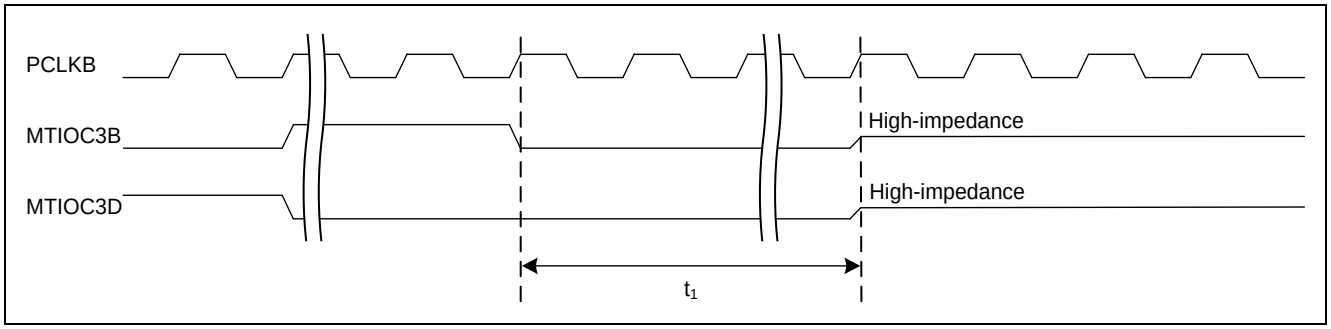


Figure 4.2 Output Disable Example (Active Level: Low) Using Output Level Compare

4.1.3 Output Control by Register Setting

An output control operation example using register setting is described below.

- Output disable control
  - Pressing SW1 causes the MTU3 and MTU4 or GPT0 to GPT2 pin output disable bit (SPOER.MTUCH34HIZ) to change to 1.
  - The PWM output pin enters the Hi-Z state.
  - The LEDs illuminate as indicated in Table 4.1, LED Illumination Patterns.
- Output restore control
  - The SPOER.MTUCH34HIZ bit is cleared, restoring the PWM output state.
  - The LEDs turn off, indicating the output disabled state.

Table 4.4 lists the output disable timing using register setting, and Figure 4.3 shows an output disable operation example using register setting.

Table 4.4 Output Disable Timing Using Register Setting

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Max.	Unit
Output disable by register setting	t_2	—	3*1	t_{PBcyc}*2

Note 1. This is a reference valve. Make sure to perform careful evaluation on your system.

Note 2. t_{PBcyc}: PCLKB period

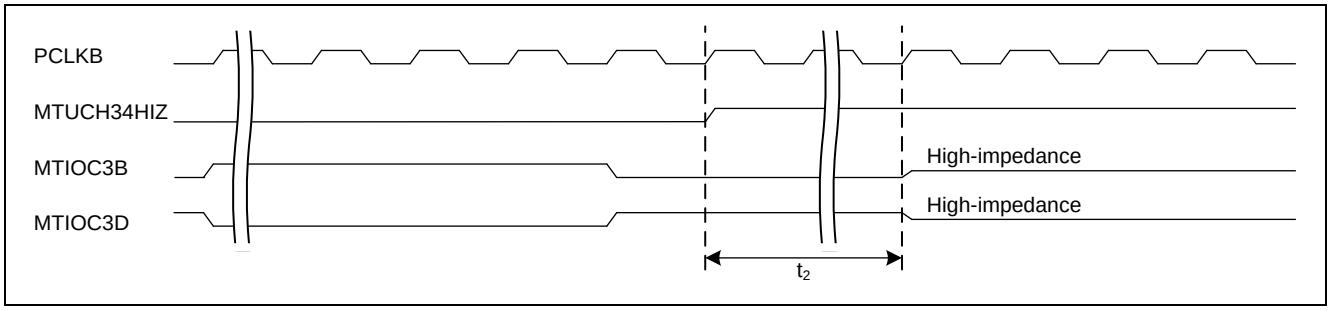


Figure 4.3 Output Disable Operation Example Using Register Setting

4.1.4 Output Control by Comparator Output Detect

When PWM output is restored from the disabled state, note that if the analog input voltage is higher than the reference input voltage while the non-inverted output setting is selected, the edge that is the comparator output detect source does not occur, and switching once again to the PWM output disabled state does not take place, even if the comparator channel 0 output detect flag (POECMPFR.C0FLAG) has been cleared. For details, refer to RX24U Group User's Manual: Hardware, which is listed in the Reference Documents section.

In the program described in this application note, output disable control by register setting is performed as part of output restore control in order to deal with the issue described above.

An output control operation example using comparator output detection is described below.

- Output disable control
  - If the analog input voltage is higher than the reference input voltage when the comparator is set to non-inverted, the value of POECMPFR.C0FLAG changes to 1.
  - The PWM output pin enters the Hi-Z state.
  - The LEDs illuminate as indicated in Table 4.1, LED Illumination Patterns.
- Output restore control
  - The SPOER.MTUCH34HIZ bit is set to 1 to perform PWM output disable control.
  - The POECMPFR.C0FLAG bit is cleared to 0.
  - Clearing the SPOER.MTUCH34HIZ bit to 0 while the value of the comparator output monitor flag (CMPMON.CMPMON0) is 0 restores the PWM output state.
  - The LEDs turn off, indicating the output disabled state.

Table 4.5 lists the output disable timing using comparator output detect, and Figure 4.4 shows an output disable example using comparator output detect. The detection time of comparator C is not included in Table 4.5 and Figure 4.4.

Table 4.5 Output Disable Timing Using Comparator Output Detect

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Max.	Unit
Output disable by comparator output detect	t_3	—	7*1	t_{PBcyc}*2

Note 1. This is a reference valve. Make sure to perform careful evaluation on your system.
Note 2. t_{PBcyc}: PCLKB period

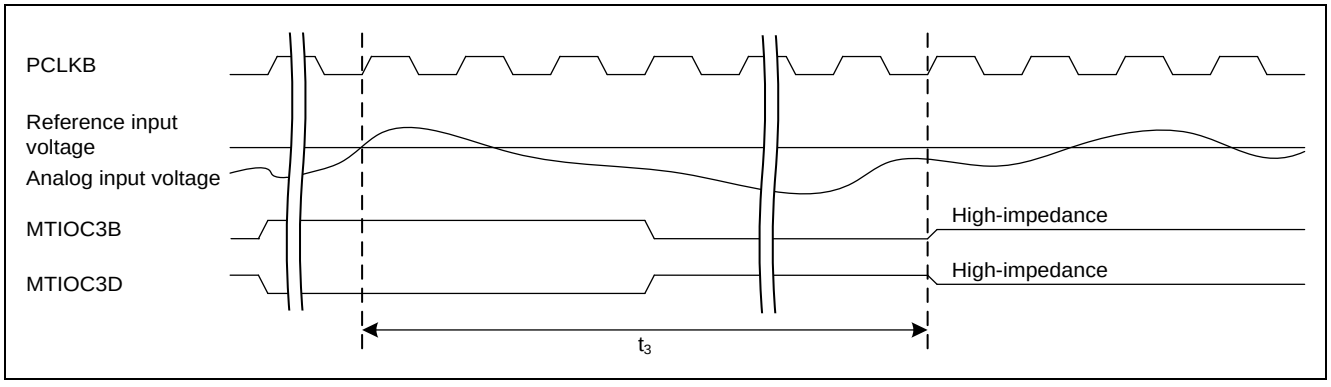


Figure 4.4 Output Disable Example Using Comparator Output Detect

4.1.5 Output Control by Oscillation Stop Detect

An output control operation example using oscillation stop detection is described below.

- Output disable control
  - When oscillation by the main clock oscillator stops, the PWM output pin enters the Hi-Z state and execution branches to an exception handler routine.
  - After the pin output changes, the values of the oscillation stop detect flags (OSTDSR.OSTDF and ICSR6.OSTSTF) change to 1.
  - The LEDs illuminate as indicated in Table 4.1, LED Illumination Patterns.
- Output restore control
  - After oscillation of the main clock restarts, the OSTDSR.OSTDF bit is cleared to 0, the clock is set again, and the ICSR6.OSTSTF bit is cleared to 0, resulting in a state in which the PWM output state can be restored. However, oscillation stop detect is a non-maskable interrupt, so only emergency measures to prevent malfunction should be implemented. Program execution should be halted, or a system reset applied.

Figure 4.6 lists the output disable timing using oscillation stop detect, and Figure 4.5 shows an output disable example using oscillation stop detect.

Table 4.6 Output Disable Timing Using Oscillation Stop Detect

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Max.	Unit
Output disable by oscillation stop detect	t_4	—	10*1	µs
Flag setting by oscillation stop detect	t_5	—	1	ms

Note 1. This is a reference valve. Make sure to perform careful evaluation on your system.

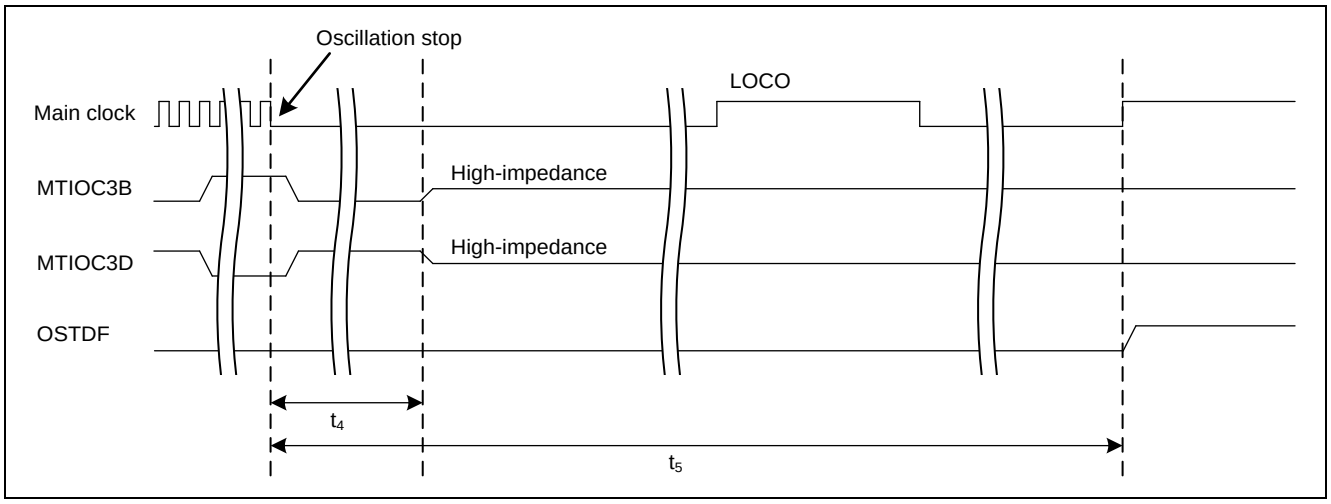
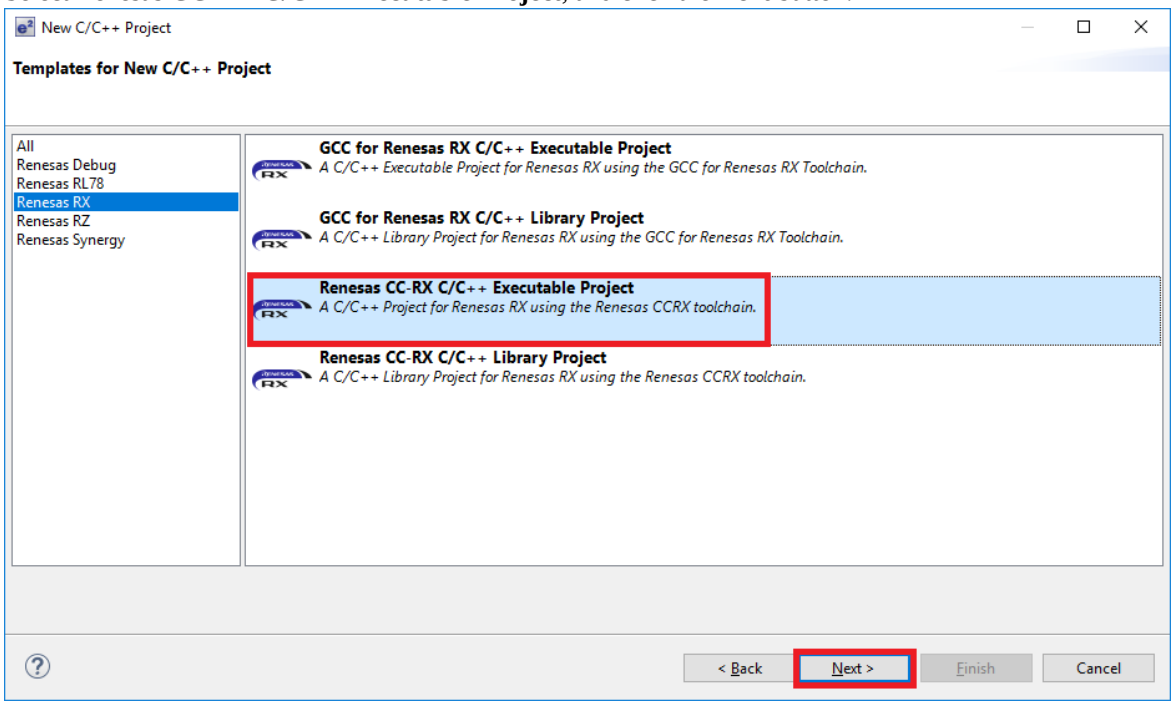


Figure 4.5 Output Disable Example Using Oscillation Stop Detect

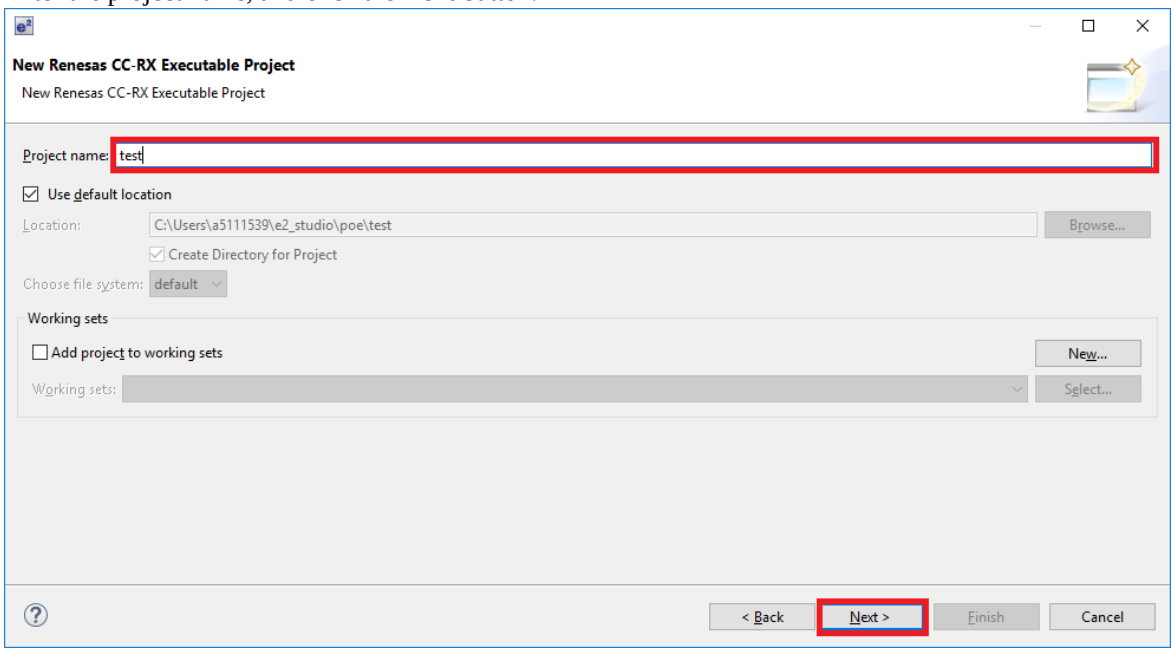
4.2 Adding the Code Generator Plugin to a Project

Steps (1) to (5) below provide an example of adding the code generator plugin to a project. Only the minimum settings required for the program described in this application note are made.

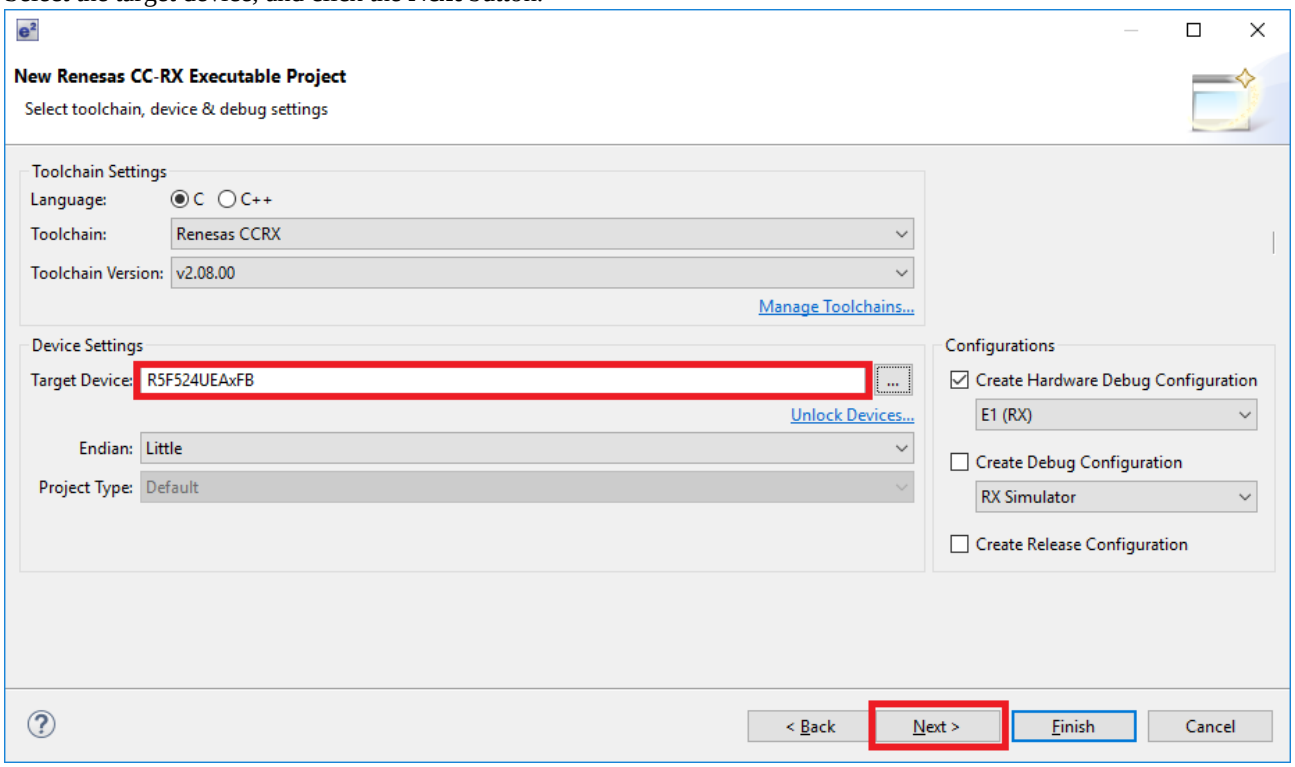
(1) Select Renesas **CC-RX C/C++ Executable Project**, and click the **Next** button.



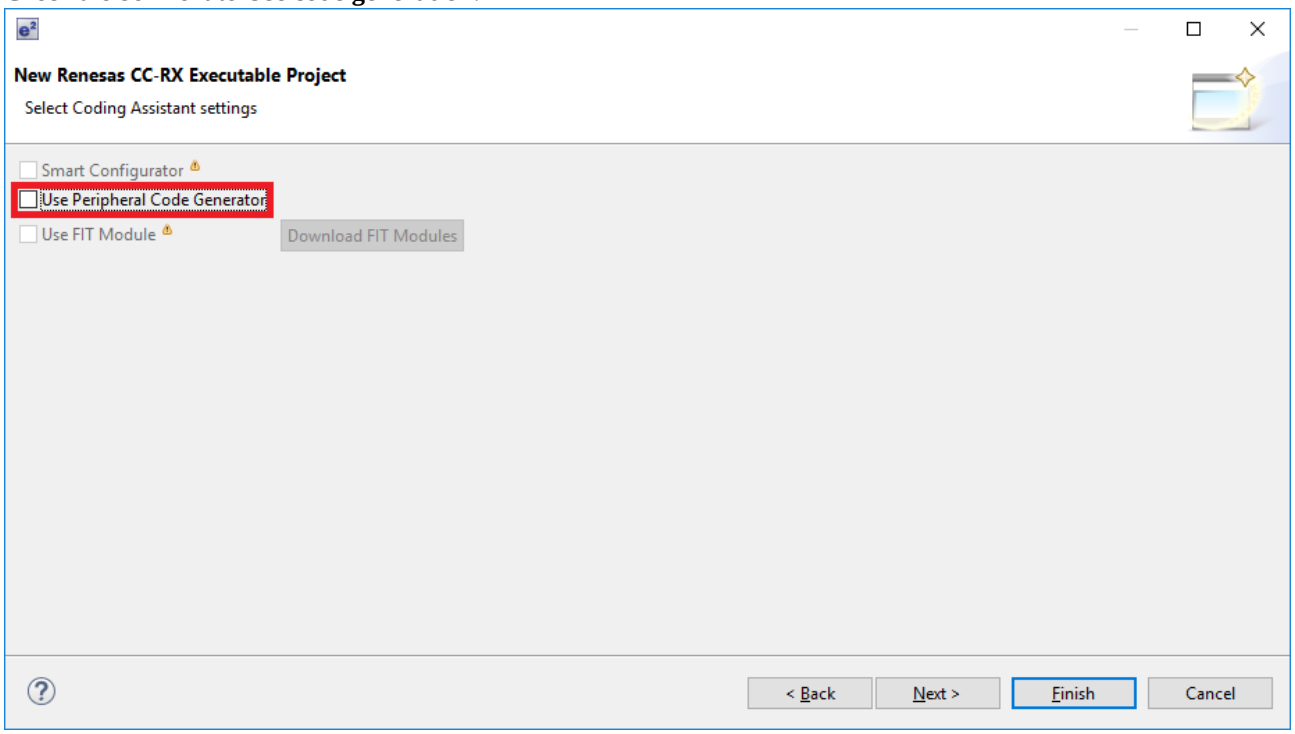
(2) Enter the project name, and click the **Next** button.



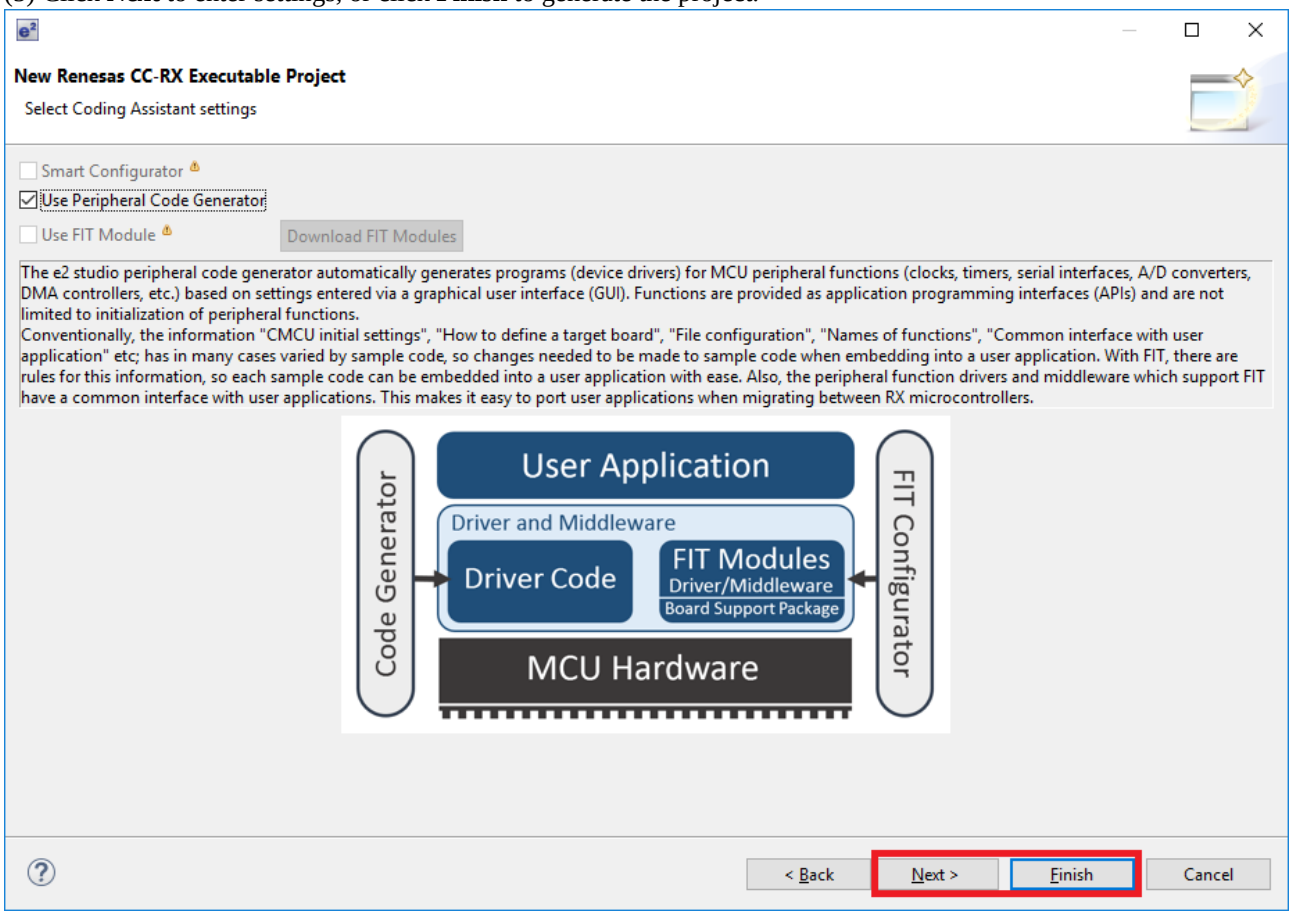
(3) Select the target device, and click the **Next** button.



(4) Check the box next to **Use code generation**.



(5) Click **Next** to enter settings, or click **Finish** to generate the project.



4.3 Code Generator Plugin Setting Items

The code generator plugin setting items for each of the functions used by the program described in this application note are presented in 4.3.1 to 4.3.7. Note that each API function contains comment lines to allow users to add their own code. Do not add code or make changes to the code outside of the designated user code area.

4.3.1 Clock Generation Circuit

Figure 4.6 shows the setting items for the clock generation circuit.

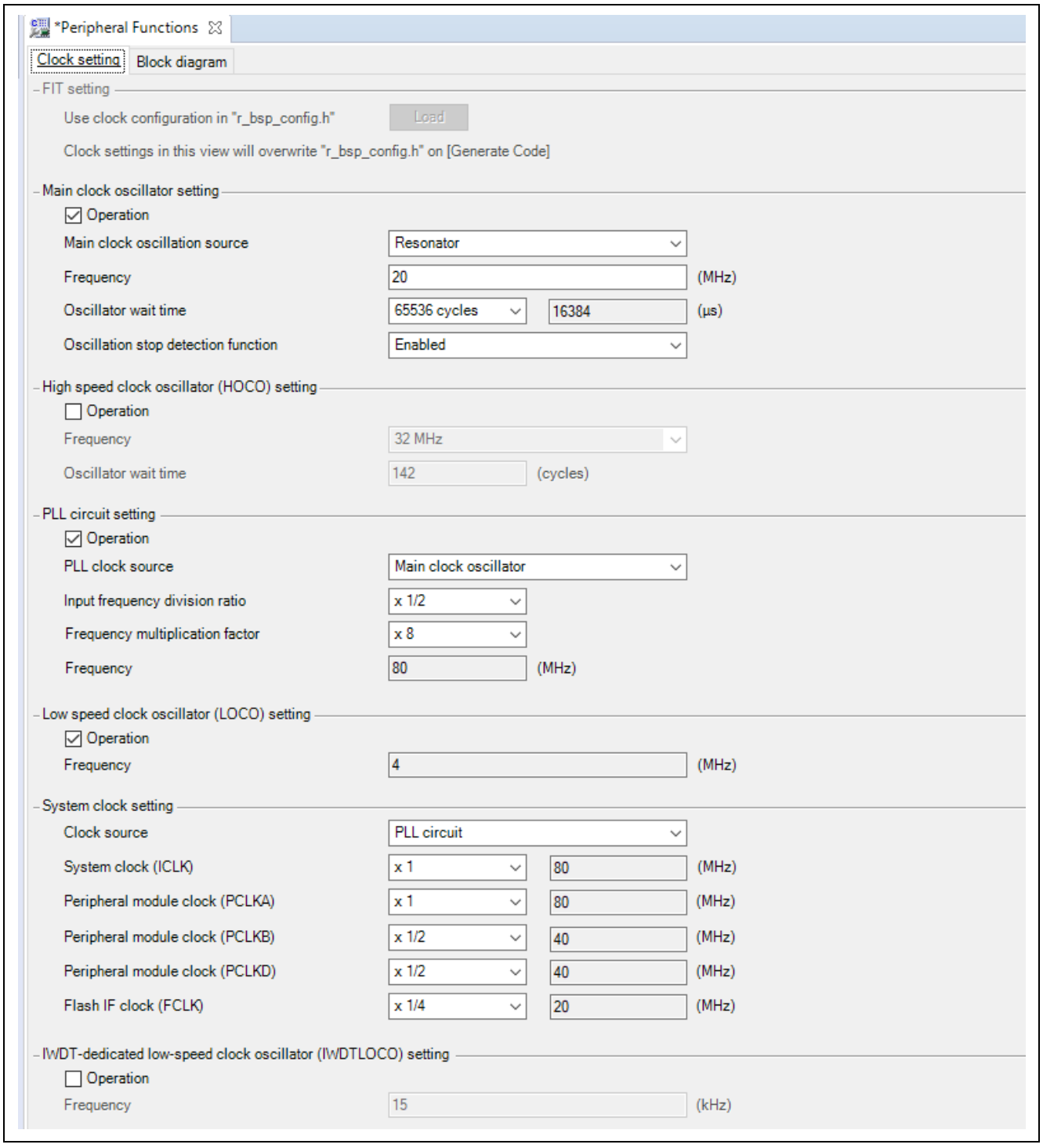


Figure 4.6 Clock Generation Circuit Setting Items

4.3.2 I/O Ports

Figure 4.7 and Figure 4.8 show the setting items for the I/O port pins. Pins other than those corresponding to the I/O ports used by the program described in this application note are omitted. Also, pins used as peripheral functions are indicated by yellow highlighting.

Figure 4.7 I/O Port Pin (PORT2) Setting Items

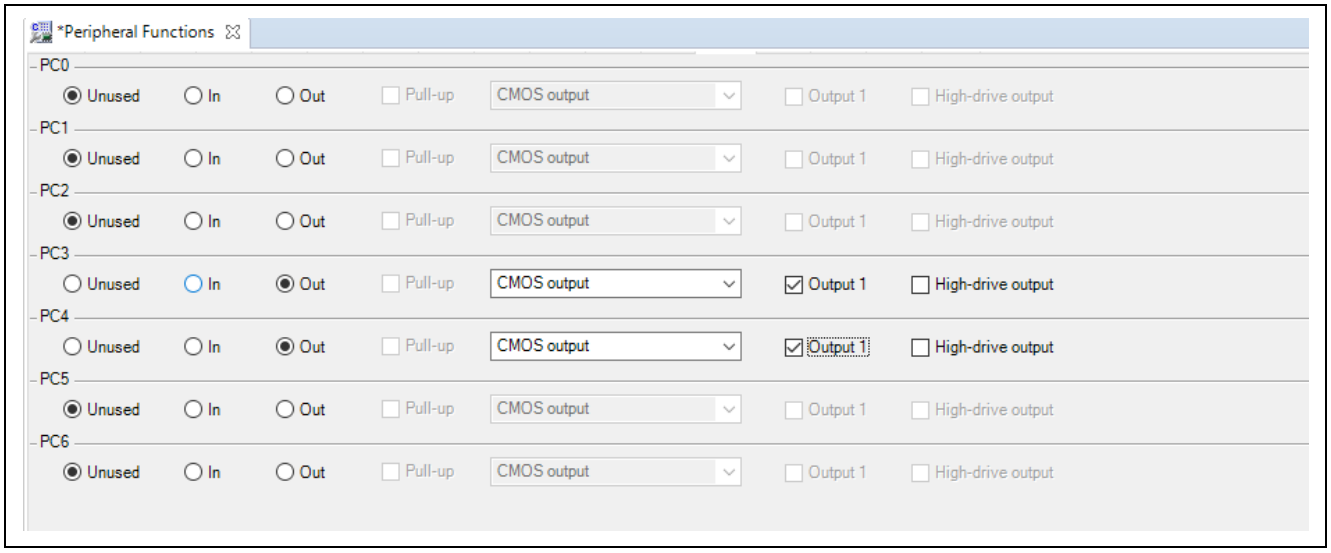


Figure 4.8 I/O Port Pin (PORTC) Setting Items

4.3.3 Interrupt Controller (ICUb)

Figure 4.9 shows the setting items for the interrupt controller.

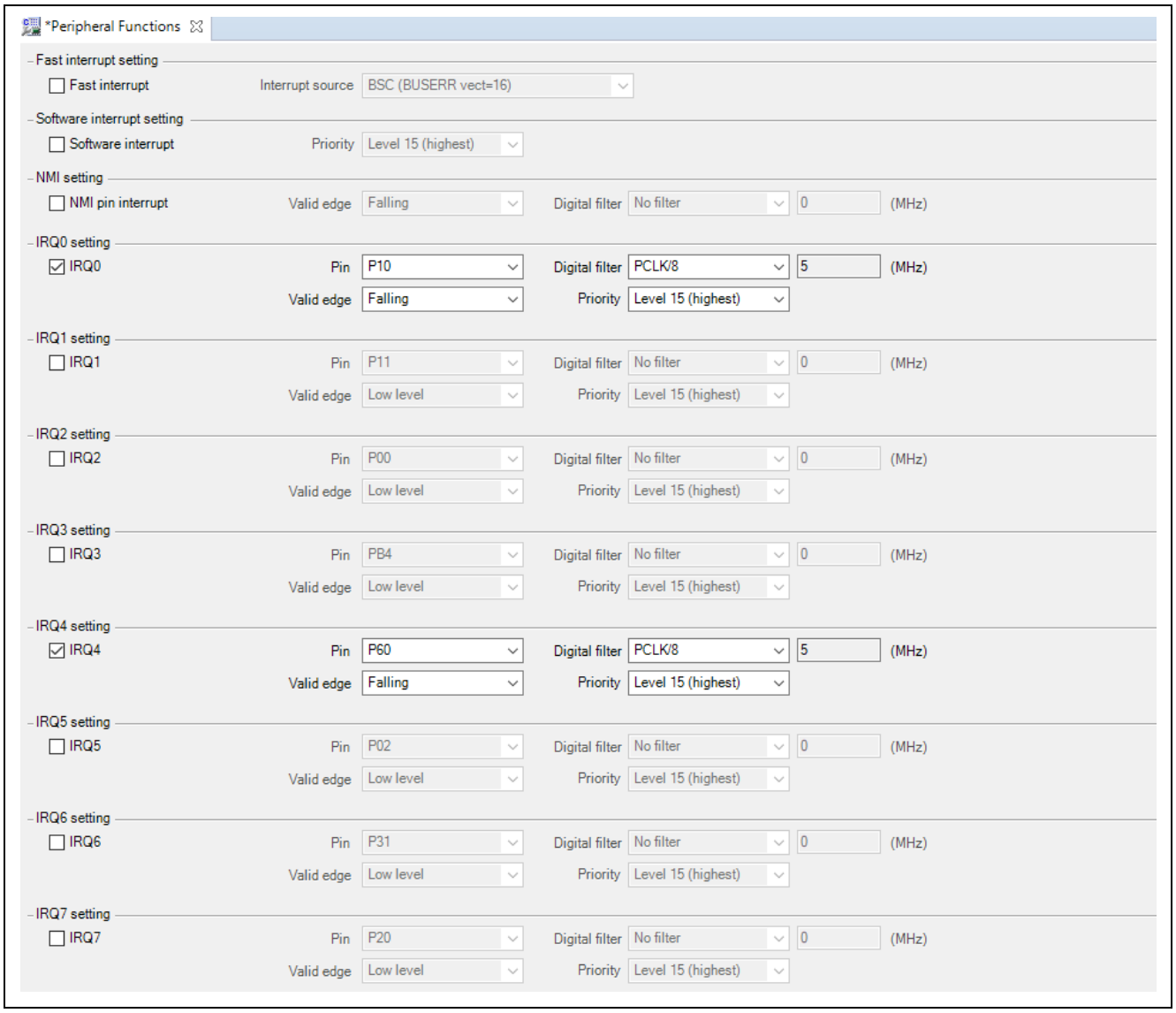


Figure 4.9 Interrupt Controller Setting Items

4.3.4 Multi-Function Timer Pulse Unit 3 (MTU3d)

Figure 4.10 to Figure 4.12 show the setting items for multi-function timer pulse unit 3.

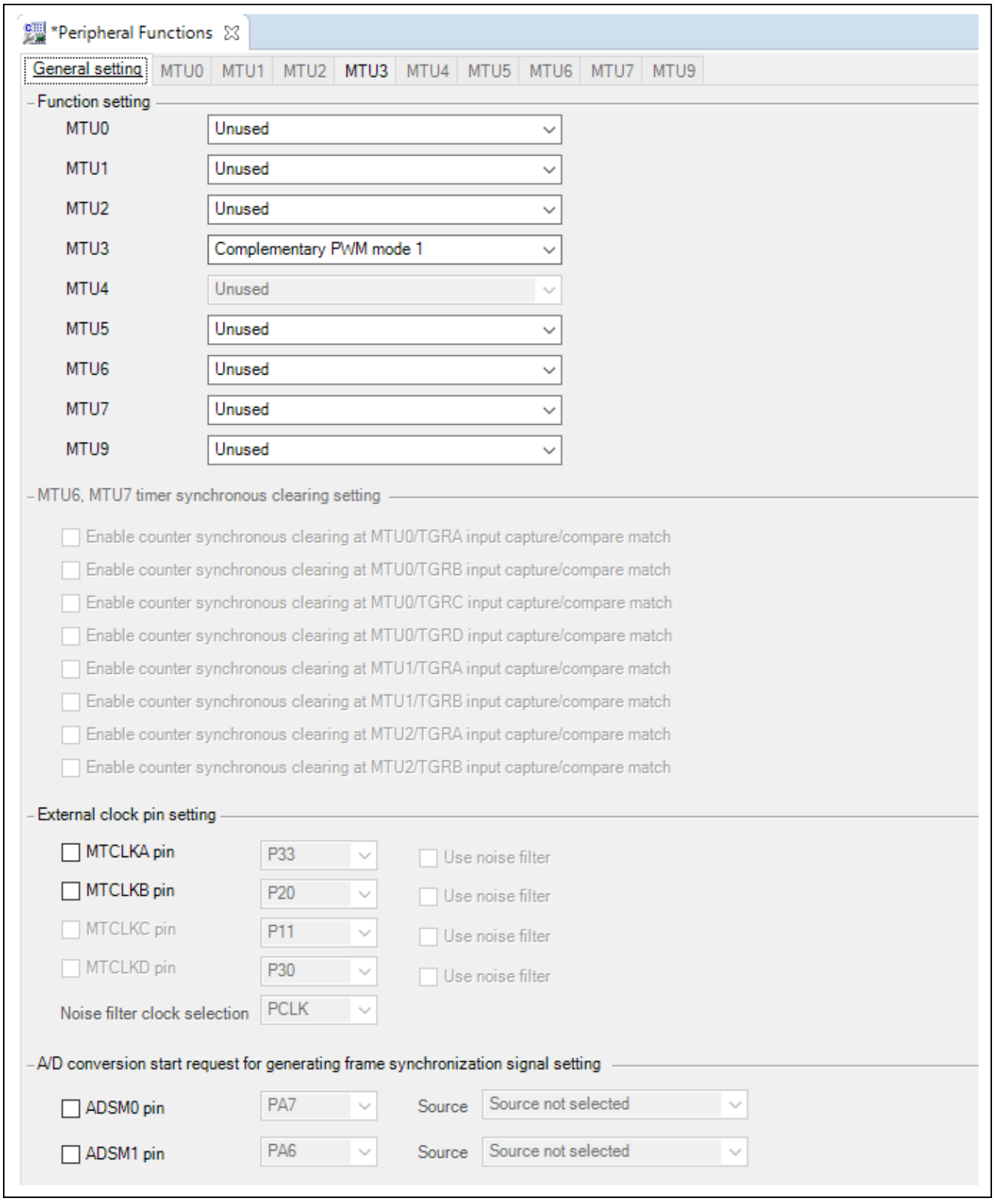


Figure 4.10 Multi-Function Timer Pulse Unit 3 (General Setting) Setting Items

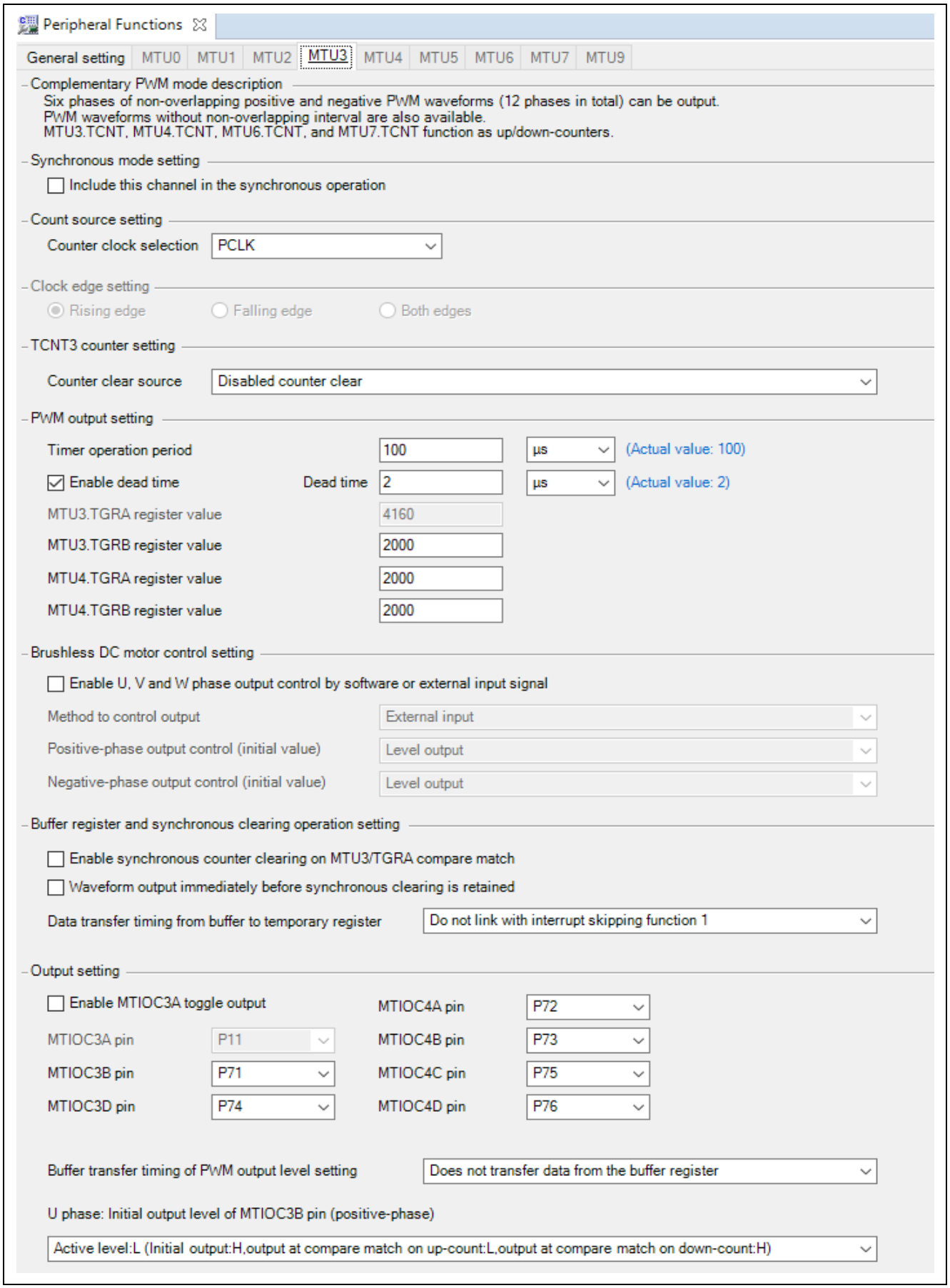


Figure 4.11 Multi-Function Timer Pulse Unit 3 (Channel: MTU3) Setting Items (1/2)

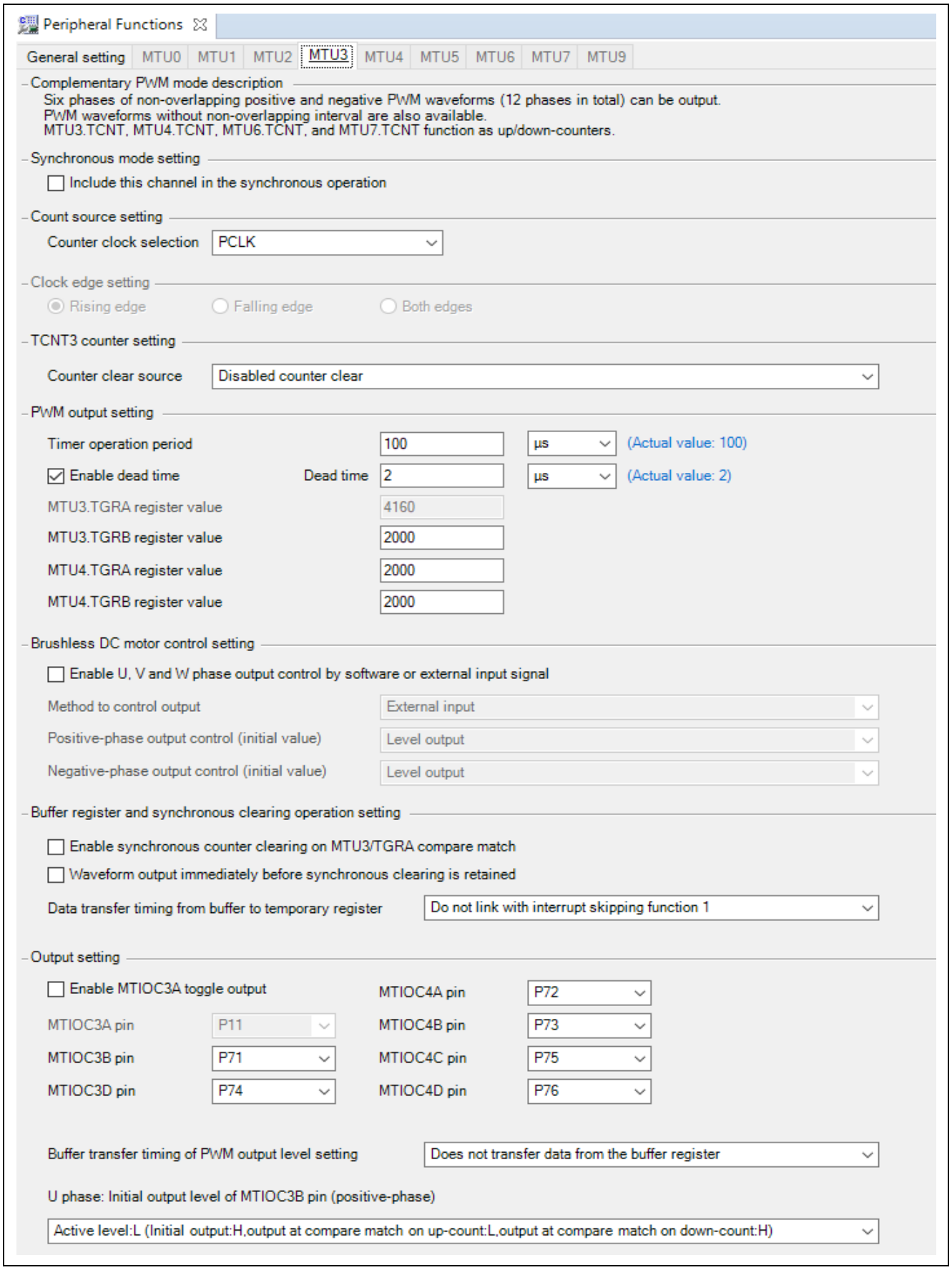


Figure 4.12 Multi-Function Timer Pulse Unit 3 (Channel: MTU3) Setting Items (2/2)

4.3.5 Port Output Enable 3 (POE3A)

Figure 4.13 and Figure 4.14 show the setting items for port output enable 3. Setting locations not used by the program described in this application note are omitted.

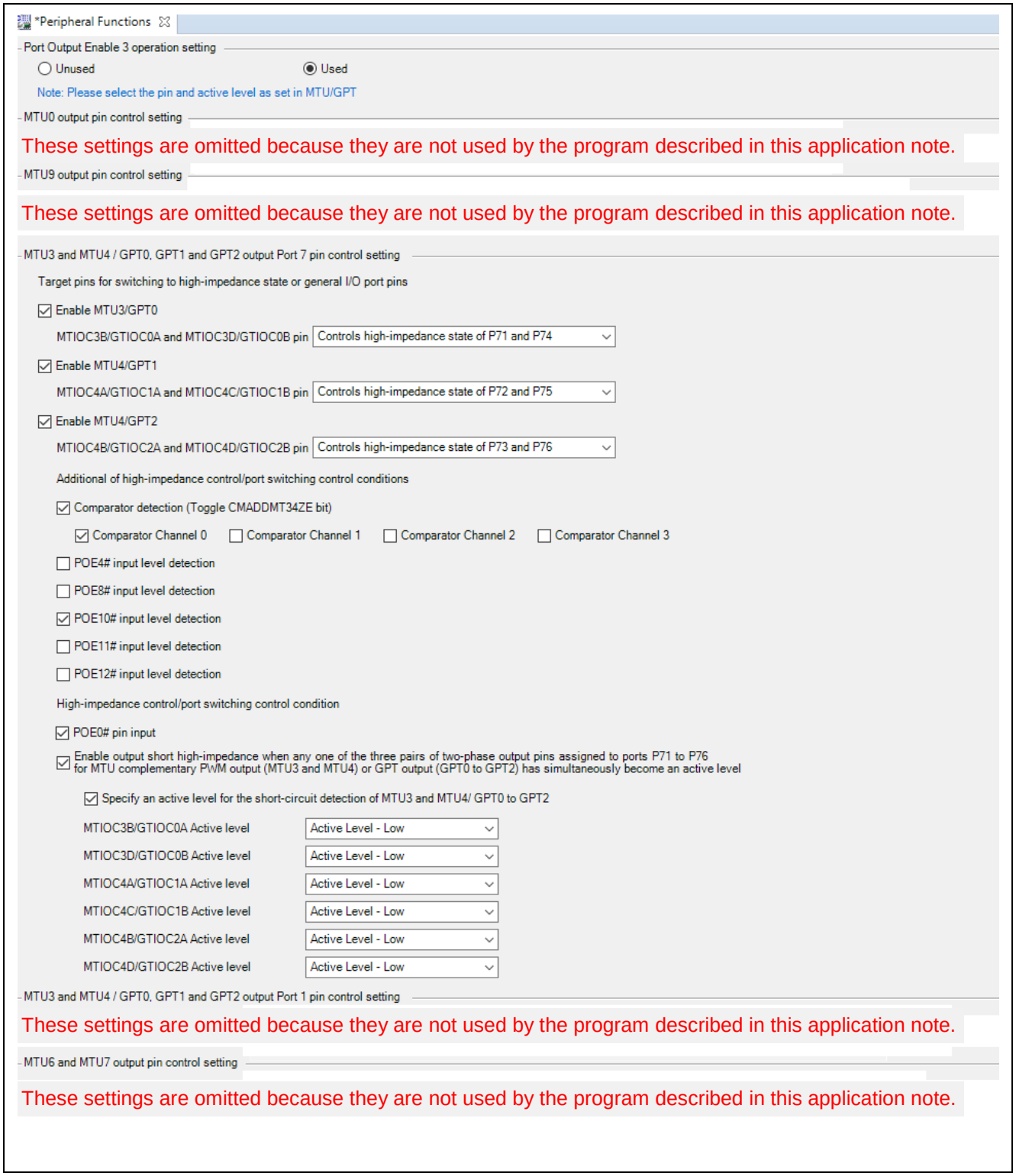


Figure 4.13 Port Output Enable 3 Setting Items (1/2)

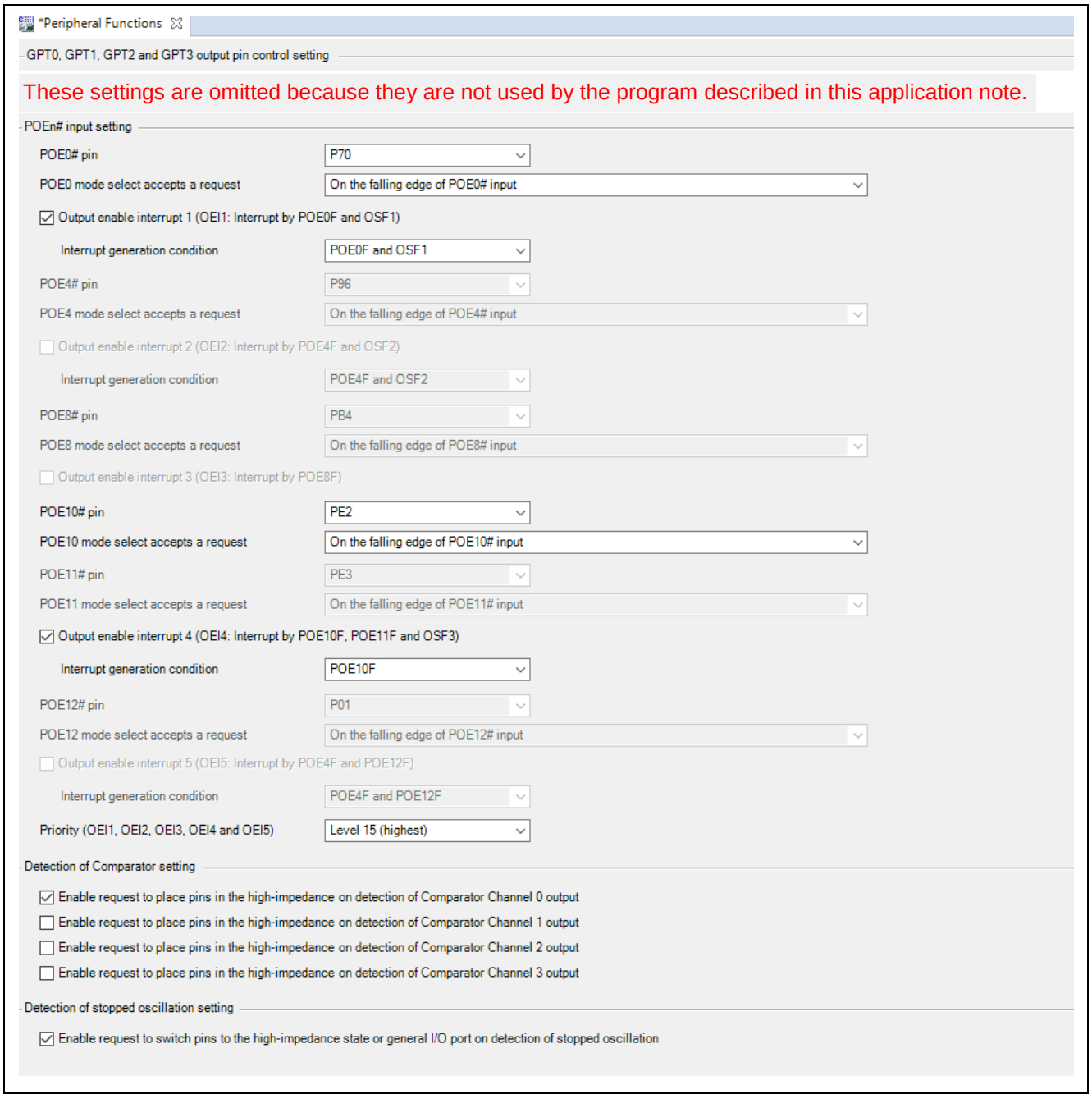


Figure 4.14 Port Output Enable 3 Setting Items (2/2)

4.3.6 Comparator C (CMPC0)

Figure 4.15 and Figure 4.16 show the setting items for comparator C.

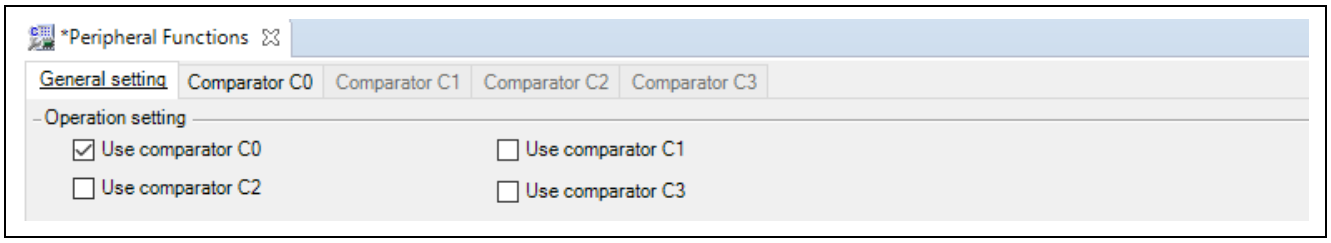


Figure 4.15 Comparator C (General Setting) Setting Items

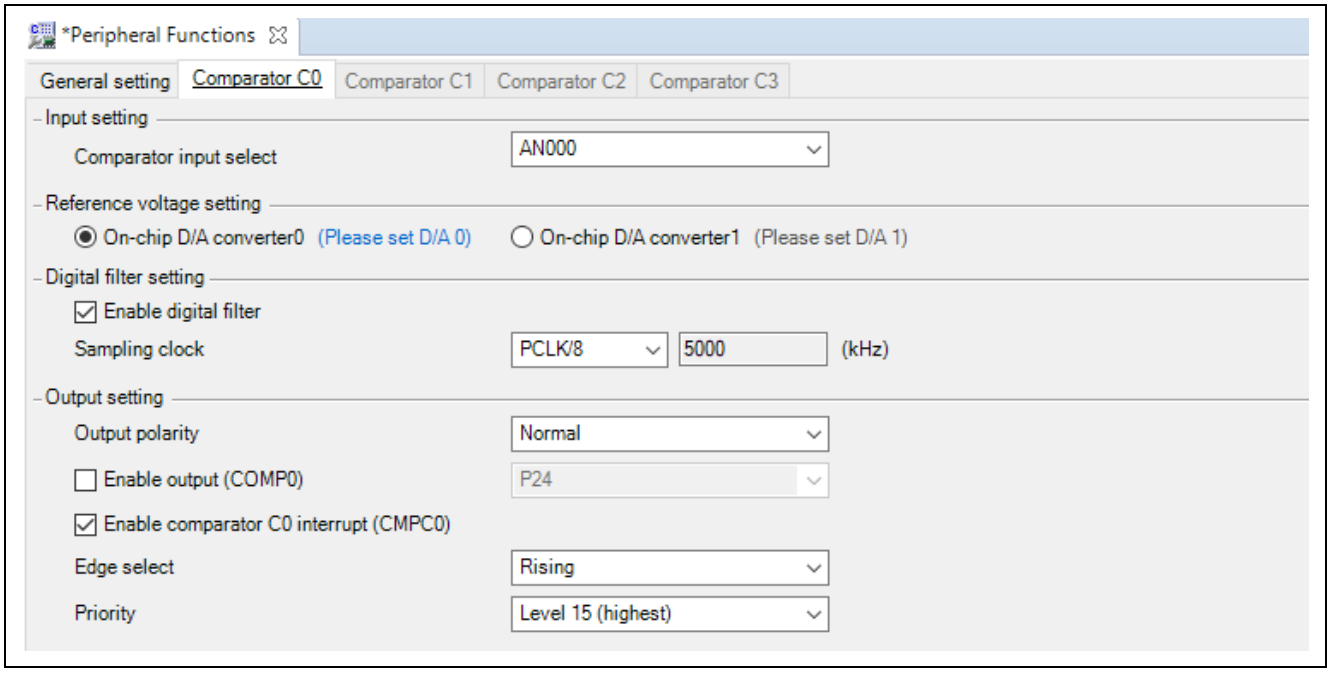


Figure 4.16 Comparator C (Comparator C0) Setting Items

4.3.7 D/A Converter (DAa)

Figure 4.17 shows the setting items for D/A converter.

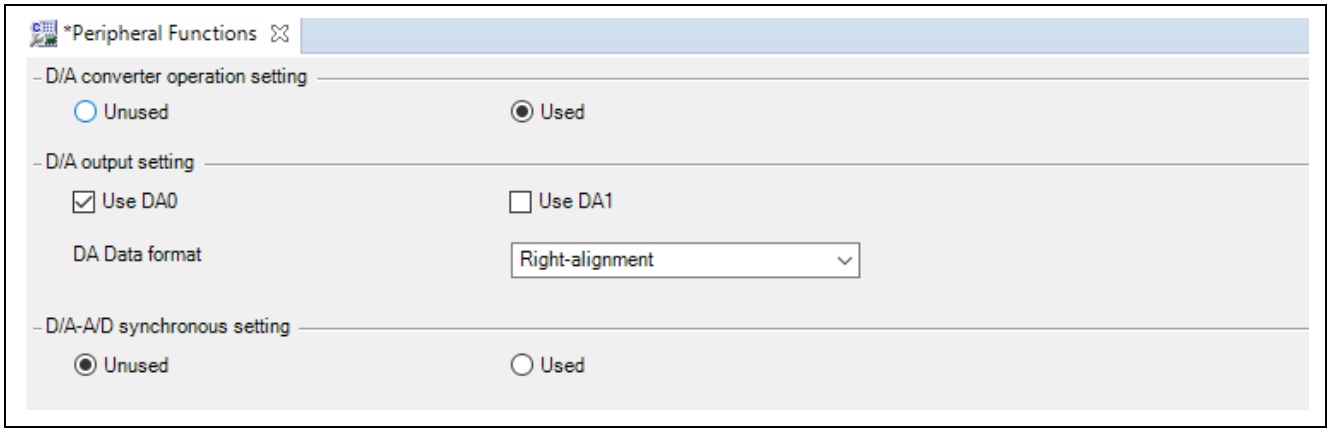


Figure 4.17 D/A Converter Setting Items

4.4 File Configuration

Table 4.7 lists the files used by the sample code. Files that are generated automatically by the integrated development environment and code generator plugin, and whose contents have not been modified, are not listed.

Table 4.7 Files Used by Sample Code

File Name	Outline	Remarks
r_cg_main.c	Main processing routine, D/A converter a startup, comparator C startup, IRQ0 interrupt enable, IRQ4 interrupt enable, MTU3d startup, OEI1 interrupt enable, OEI4 interrupt enable	File generated by code generator plugin
r_cg_icu_user.c	IRQ0 (SW0) and IRQ4 (SW1) interrupt handlers	File generated by code generator plugin
r_cg_poe3_user.c	Input level detect interrupt handler (POE0#, POE10#), output level compare interrupt handler	File generated by code generator plugin
r_cg_cmpc_user.c	Comparator output detect interrupt handler	File generated by code generator plugin
r_cg_cgc_user.c	Oscillation stop detect interrupt handler (NMI)	File generated by code generator plugin
r_cg_userdefine.h	List of constants added after code generation	File generated by code generator plugin

4.5 Option-Setting Memory

Table 4.8 lists the option-setting memory states used by the sample code. If necessary, these should be changed to optimal values.

Table 4.8 Option-Setting Memory States Used by Sample Code

Symbol	Address	Setting Value	Description
OFS0	FFFF FF8Ch to FFFF FF8Fh	FFFF FFFFh	IWDT halted after a reset
OFS1	FFFF FF88h to FFFF FF8Bh	FFFF FFFFh	Voltage monitoring 0 reset disabled after reset
MDE	FFFF FF80h to FFFF FF83h	FFFF FFFFh	Little-endian selected

4.6 Constants

Table 4.9 lists the constants used in the sample code.

Table 4.9 Constants

Constant Name	Setting Value	Contents
LED_ON	0	LED is on.
LED_OFF	1	LED is off.
LOW_LEVEL	0	I/O port output level is low.
HIGH_LEVEL	1	I/O port output level is high.
OUTPUT_STATE_NORMAL	0	PWM output state is normal.
OUTPUT_STATE_STOP	1	PWM output state is disabled (all disable sources included).
DETECTED	1	PWM output disable source detected.
NOT_DETECTED	0	PWM output disable source not detected.
DA0_VALUE	80h	D/A0 setting value

4.7 Variables

Table 4.10 lists the variables.

Table 4.10 Variables

Type	Variable Name	Description	Used by Function
uint8_t	poe_state_of_irq0	PWM output state variable used by irq0	r_icu_irq0_interrupt
uint8_t	poe_flag_state	PWM output disable source flag state variable	get_poe_stop_flag
static uint8_t	poe0_state_of_detect	POE0# pin input level detect state variable	return_to_pwm_output
static uint8_t	poe10_state_of_detect	POE10# pin input level detect state variable	return_to_pwm_output
static uint8_t	comparator_state_of_detect	Comparator output detect state variable	return_to_pwm_output

4.8 Functions

Table 4.11 lists the functions.

Table 4.11 Functions

Function Name	Outline
main	Main processing routine
R_MAIN_UserInit	Initial settings
da0_set_output_value	D/A0 value setting
module_start	Module start
r_icu_irq0_interrupt	IRQ0 interrupt handler
r_icu_irq4_interrupt	IRQ4 interrupt handler
get_poe_stop_flag	Get PWM output disable flag state
return_to_pwm_output	PWM output restore processing
r_cmpc_cmpc0_interrupt	Comparator interrupt handler
r_poe3_oei1_interrupt	OEI1 interrupt handler
r_poe3_oei4_interrupt	OEI4 interrupt handler
r_cgc_oscillation_stop_nmi_interrupt	Oscillation stop detect processing

4.9 Function Specifications

main	
Outline	Main processing routine
Header	None
Declaration	void main(void)
Description	This is the main processing routine.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generator plugin. In the sample program, processing other than initial settings is performed by interrupt handlers.

R_MAIN_UserInit	
Outline	Initial settings
Header	None
Declaration	void R_MAIN_UserInit(void)
Description	Makes initial settings.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generator plugin.

da0_set_output_value	
Outline	D/A0 value setting
Header	None
Declaration	static void da0_set_output_value(void)
Description	Sets the D/A0 value used as the comparator’s reference input voltage.
Arguments	None
Return Value	None

module_start	
Outline	Module start
Header	None
Declaration	static void module_start(void)
Description	Starts a peripheral function and enables interrupts.
Arguments	None
Return Value	None

r_icu_irq0_interrupt	
Outline	IRQ0 interrupt handler
Header	None
Declaration	static void r_icu_irq0_interrupt(void)
Description	Restores PWM output from the disabled state.
Arguments	None
Return Value	None
Remarks	This interrupt handler is generated by the code generator plugin. It is run when the irq0 interrupt occurs (when SW0 is pressed).

r_icu_irq4_interrupt	
Outline	IRQ4 interrupt handler
Header	None
Declaration	static void r_icu_irq4_interrupt(void)
Description	Disables output using the SPOER register.
Arguments	None
Return Value	None
Remarks	This interrupt handler is generated by the code generator plugin. It is run when the irq4 interrupt occurs (when SW1 is pressed).

get_poe_stop_flag	
Outline	Get PWM output disable flag state
Header	None
Declaration	static uint8_t get_poe_stop_flag(void)
Description	This function obtains the state of the PWM output pin.
Arguments	None
Return Value	OUTPUT_STATE_NORMAL The PWM output state is normal. OUTPUT_STATE_STOP The PWM output state is stopped.

return_to_pwm_output	
Outline	PWM output restore processing
Header	None
Declaration	static void return_to_pwm_output(void)
Description	Performs processing to restore the PWM output state when the output disable source has been removed.
Arguments	None
Return Value	None
Remarks	

r_cmpc_cmpc0_interrupt	
Outline	Comparator interrupt handler
Header	None
Declaration	static void r_cmpc_cmpc0_interrupt(void)
Description	Controls LED illumination and disabling of the MTU as part of the processing of PWM output disabling by comparator output detection.
Arguments	None
Return Value	None
Remarks	This interrupt handler is generated by the code generator plugin. It is run when the comparator output interrupt occurs.

r_poe3_oei1_interrupt	
Outline	OEI1 interrupt handler
Header	None
Declaration	static void r_poe3_oei1_interrupt(void)
Description	Controls LED illumination and disabling of the MTU as part of the processing of PWM output disabling by POE0# input level detection or output level comparison on pins P71 to P76.
Arguments	None
Return Value	None
Remarks	This interrupt handler is generated by the code generator plugin. It is run when output enable interrupt 1 occurs.

r_poe3_oei4_interrupt	
Outline	OEI4 interrupt handler
Header	None
Declaration	static void r_poe3_oei4_interrupt(void)
Description	Controls LED illumination and disabling of the MTU as part of the processing of PWM output disabling by POE10# input level detection.
Arguments	None
Return Value	None
Remarks	This interrupt handler is generated by the code generator plugin. It is run when output enable interrupt 4 occurs.

r_cgc_oscillation_stop_nmi_interrupt	
Outline	Oscillation stop detect processing
Header	r_cg_cgc.h
Declaration	void r_cgc_oscillation_stop_nmi_interrupt(void)
Description	Controls LED illumination and disabling of the MTU as part of the processing of PWM output disabling by oscillation stop detection (NMI), then waits until an MCU reset is applied.
Arguments	None
Return Value	None
Remarks	This interrupt handler is generated by the code generator plugin. It is run when generation of the main clock stops.

4.10 Flowcharts

Flowcharts of program operation are presented in 4.10.1 to 4.10.12. Functions generated by the code generator plugin, whose contents have not been modified, are omitted. For details of functions generated by the code generator plugin, refer to e^2 studio Code Generator User's Manual: RX API Reference, which is listed in the Reference Documents section.

4.10.1 Main Processing Routine

Figure 4.18 presents a flowchart of the main processing routine.

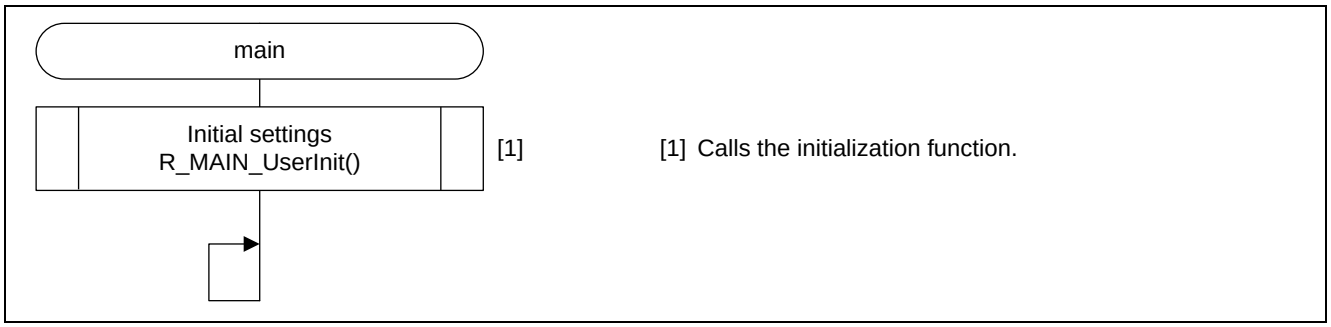


Figure 4.18 Flowchart of Main Processing Routine

4.10.2 Initial Settings

Figure 4.19 presents a flowchart of the initial settings.

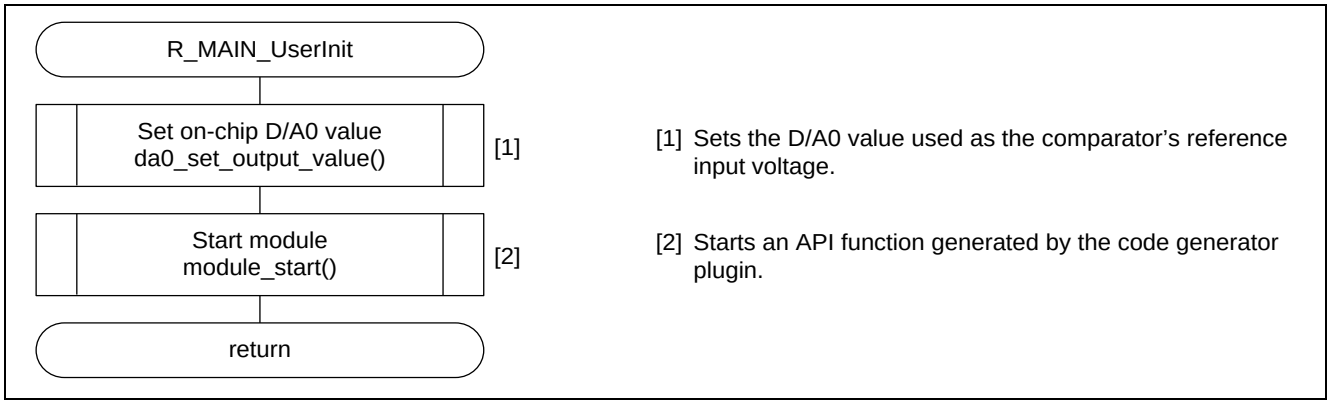


Figure 4.19 Flowchart of Initial Settings

4.10.3 D/A0 Output Voltage Value Setting

Figure 4.20 presents a flowchart of D/A0 output voltage value setting.

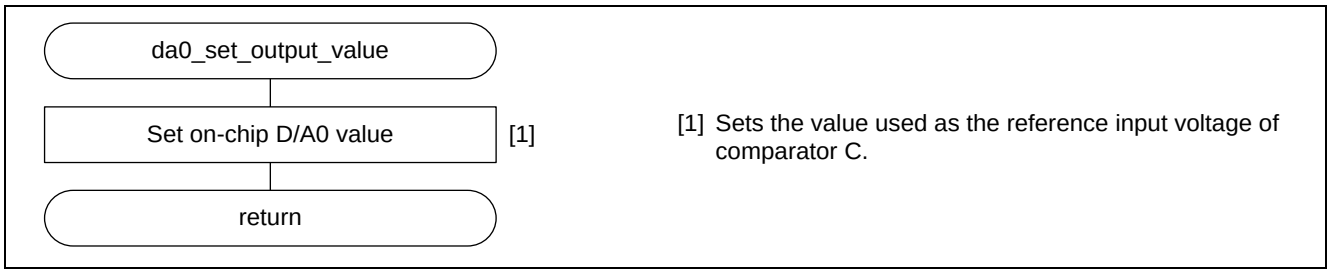


Figure 4.20 Flowchart of D/A0 Output Voltage Value Setting

4.10.4 Module Startup

Figure 4.21 presents a flowchart of module startup.

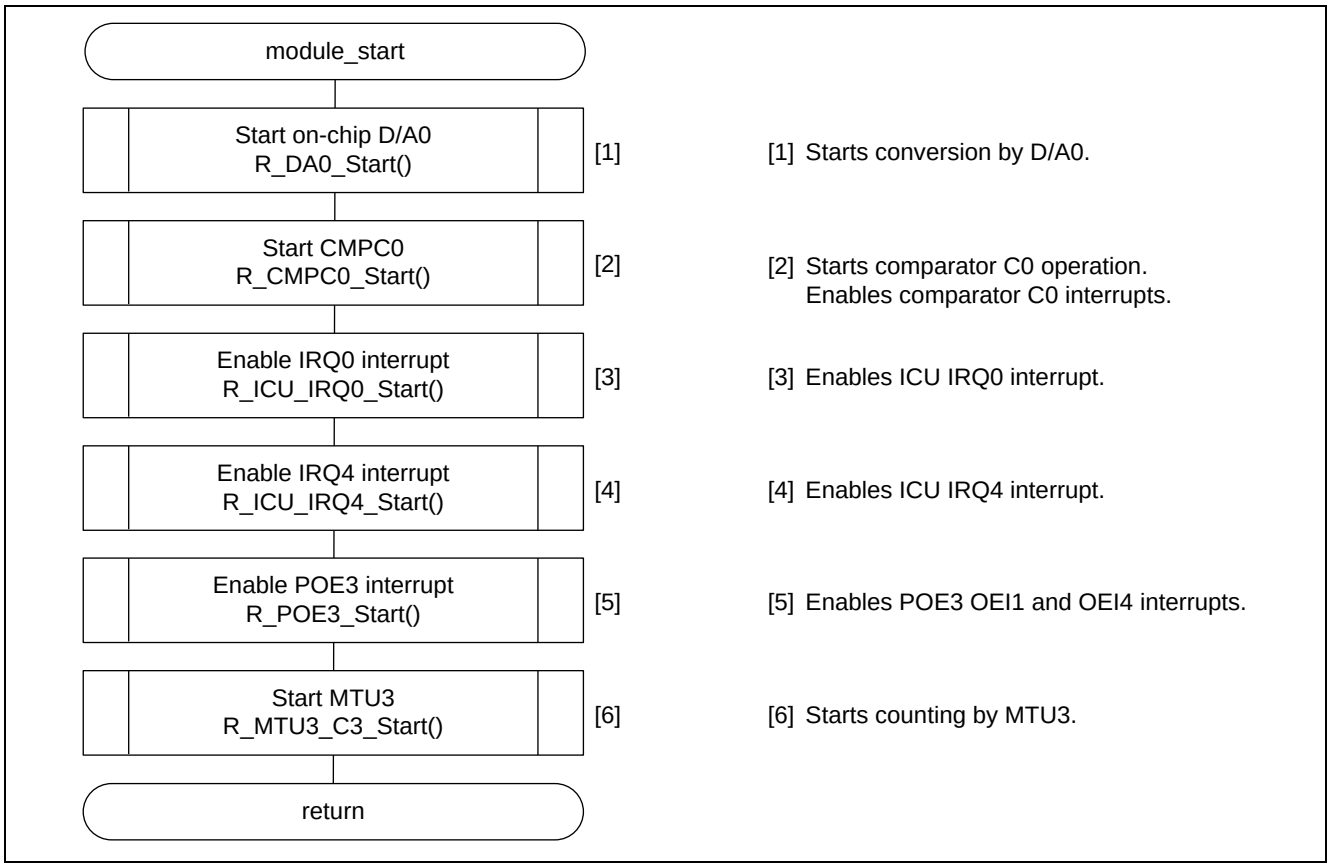


Figure 4.21 Flowchart of Module Startup

4.10.5 IRQ0 Interrupt Handler

Figure 4.22 presents a flowchart of the IRQ0 interrupt handler

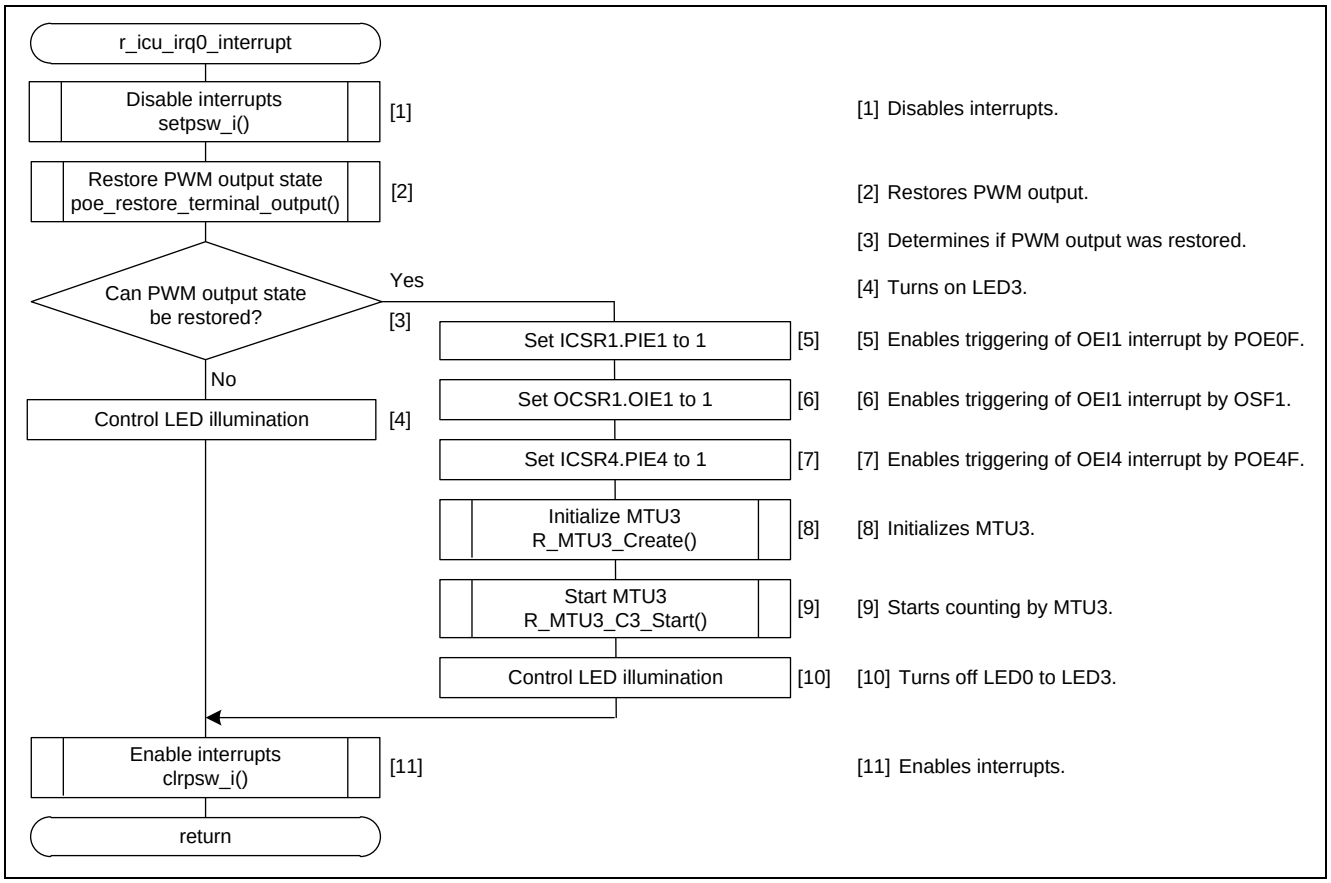


Figure 4.22 Flowchart of IRQ0 Interrupt Handler

4.10.6 IRQ4 Interrupt Handler

Figure 4.23 presents a flowchart of the IRQ4 interrupt handler.

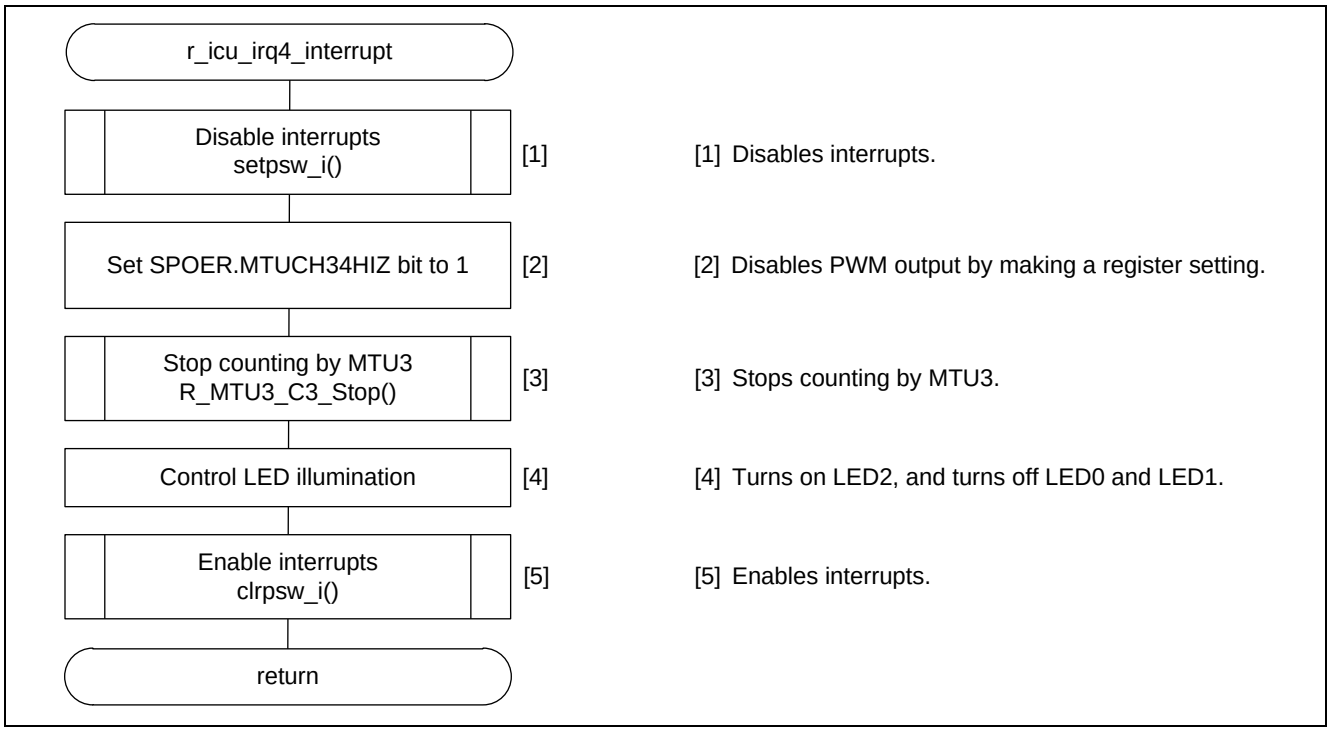


Figure 4.23 Flowchart of IRQ4 Interrupt Handler

4.10.7 Get PWM Output Disabled Flag State

Figure 4.24 presents a flowchart of getting the PWM output disabled flag state.

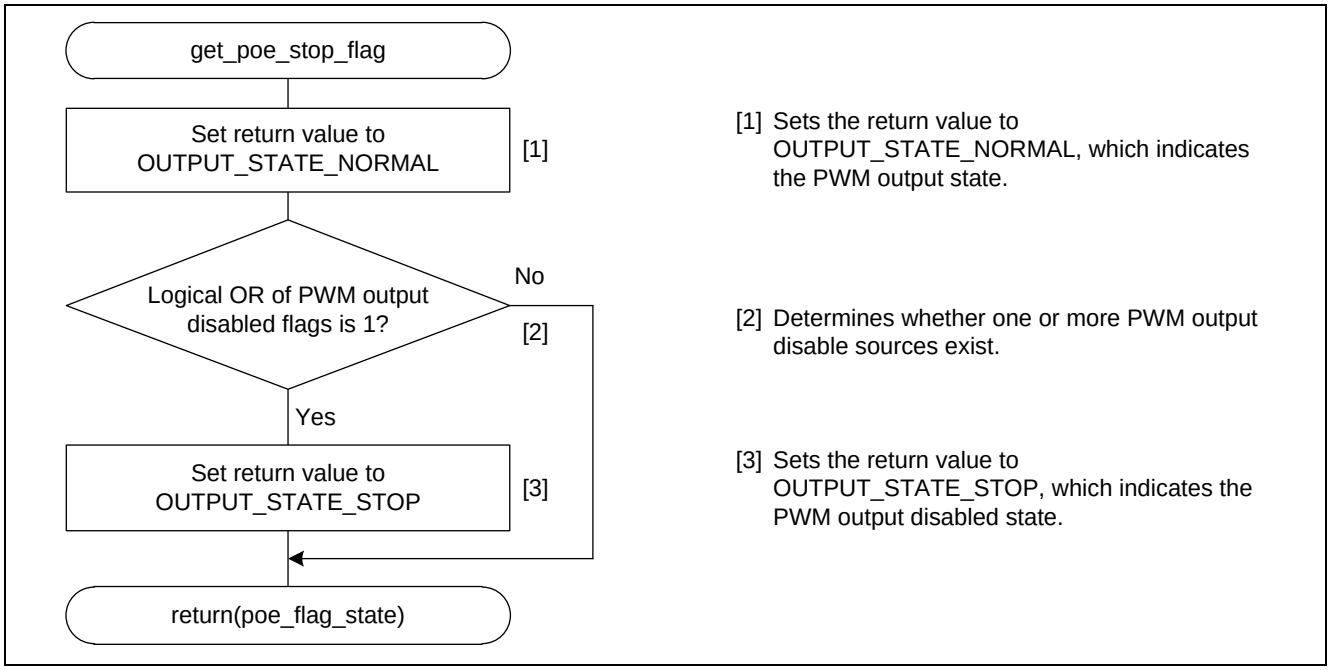
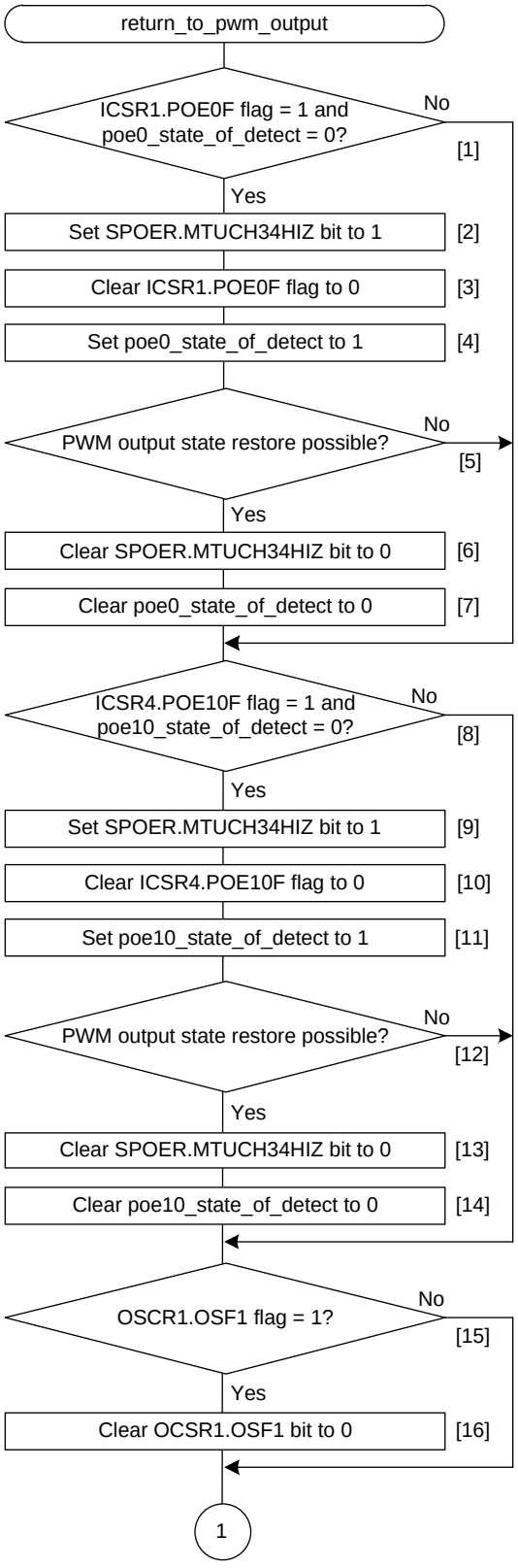


Figure 4.24 Flowchart of Getting PWM Output Disabled Flag State

4.10.8 Restore PWM Output

Figure 4.25 and Figure 4.26 present a flowchart of restoring PWM output.



[1] Determined based on POE0# pin input level and previous value of ICSR1.POE0F flag.

[2] Disables PWM output by making a register setting.

[3] Clears the ICSR1.POE0F flag to 0.

[4] Sets the POE0# pin input level detect state variable to 1.

[5] Determines whether the POE0# pin input is high-level, and halting of PWM output by a register setting due to another output disable source is not valid.

[6] Restores the PWM output state by making a register setting.

[7] Clears the POE0# pin input level detect state variable to 0.

[8] Determined based on POE10# pin input level and previous value of ICSR4.POE10F flag.

[9] Restores the PWM output state by making a register setting.

[10] Clears the POE10F flag to 0.

[11] Sets the POE10# pin input level detect state variable to 1.

[12] Determines whether the POE10# pin input is high-level, and halting of PWM output by a register setting due to another output disable source is not valid.

[13] Disables PWM output by making a register setting.

[14] Clears the POE10# pin input level detect state variable to 0.

[15] Determined based on output level compare detect flag.

[16] Clears output level compare detect flag to 0.

Figure 4.25 Flowchart of Restoring PWM Output (1/2)

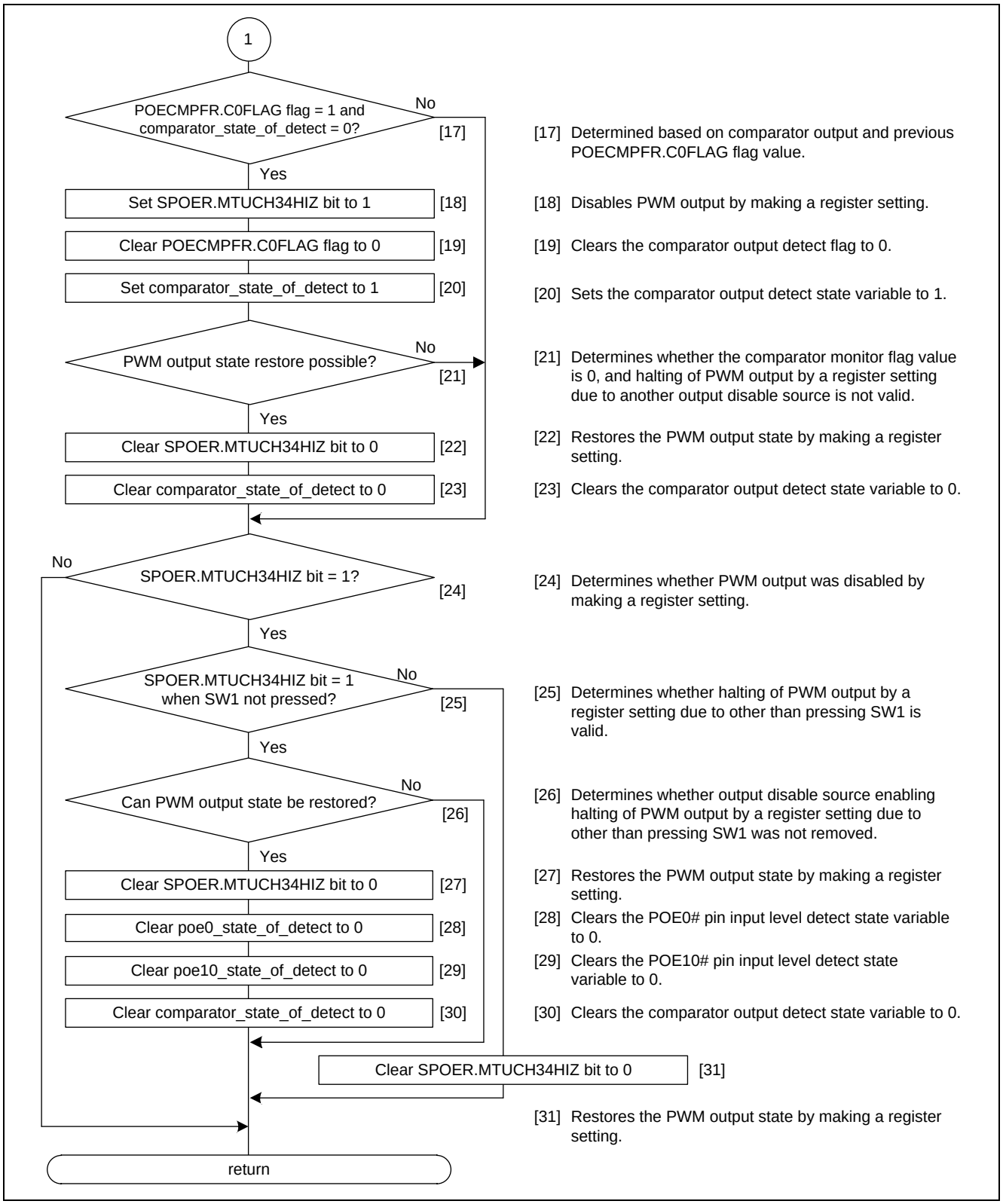


Figure 4.26 Flowchart of Restoring PWM Output (2/2)

4.10.9 Comparator Interrupt Handler

Figure 4.27 presents a flowchart of the comparator interrupt handler.

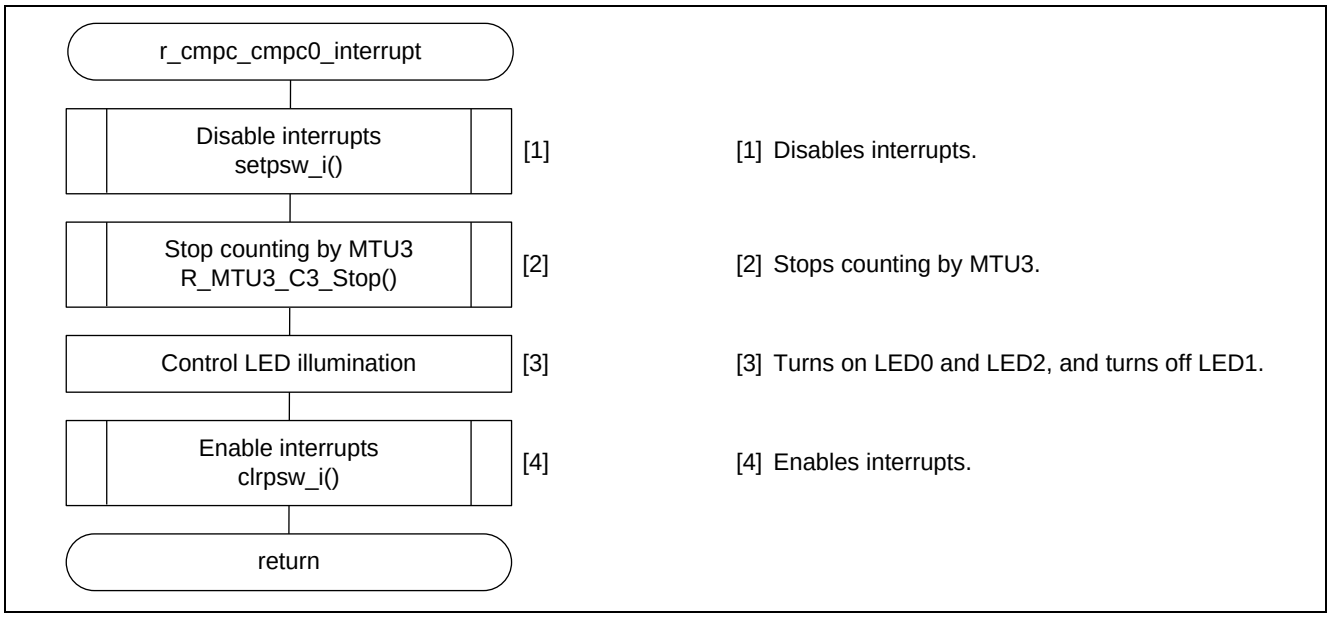


Figure 4.27 Flowchart of Comparator Interrupt Handler

4.10.10 OEI1 Interrupt Handler

Figure 4.28 presents a flowchart of the OEI1 interrupt handler.

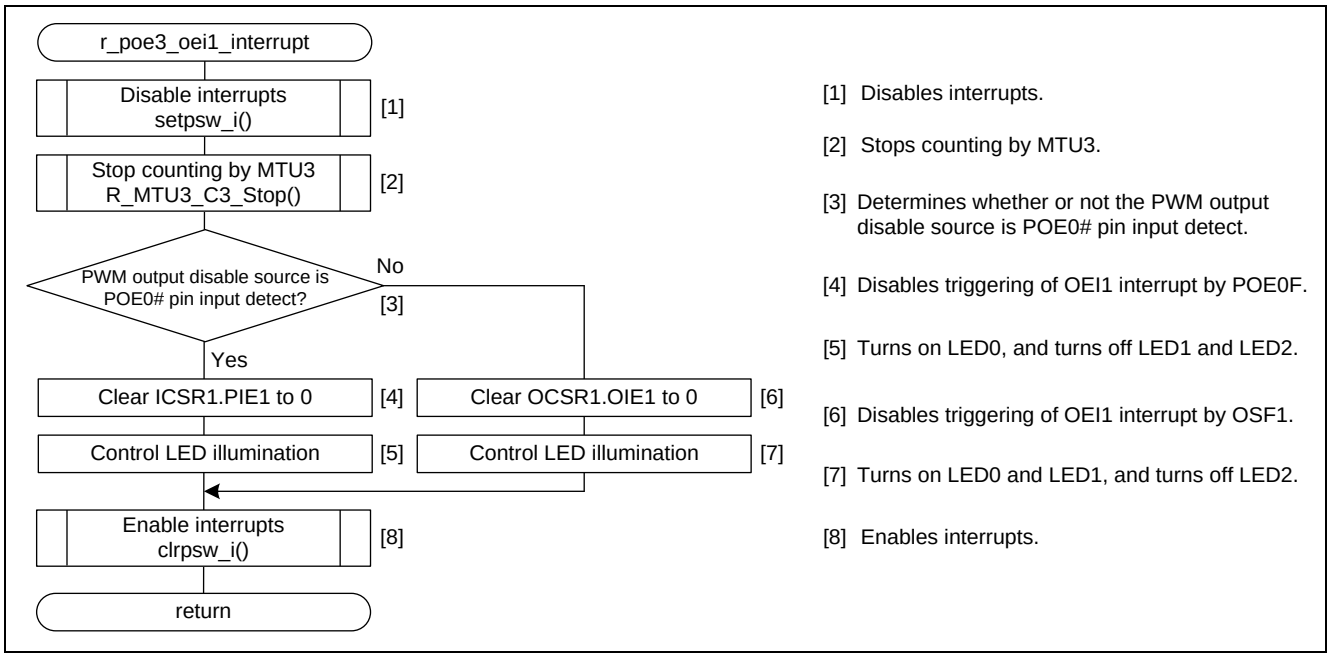


Figure 4.28 Flowchart of OEI1 Interrupt Handler

4.10.11 OEI4 Interrupt Handler

Figure 4.29 presents a flowchart of the OEI4 interrupt handler.

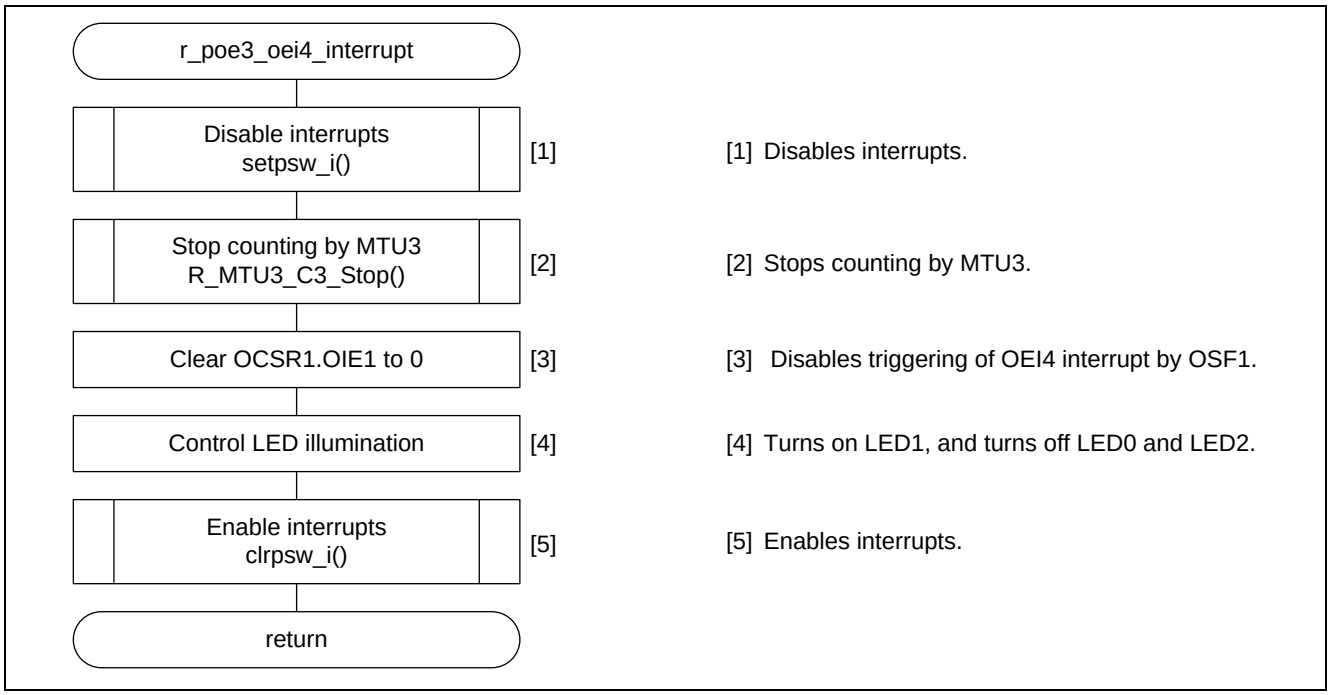


Figure 4.29 Flowchart of OEI4 Interrupt Handler

4.10.12 Oscillation Stop Detection

Figure 4.30 presents a flowchart of oscillation stop detection.

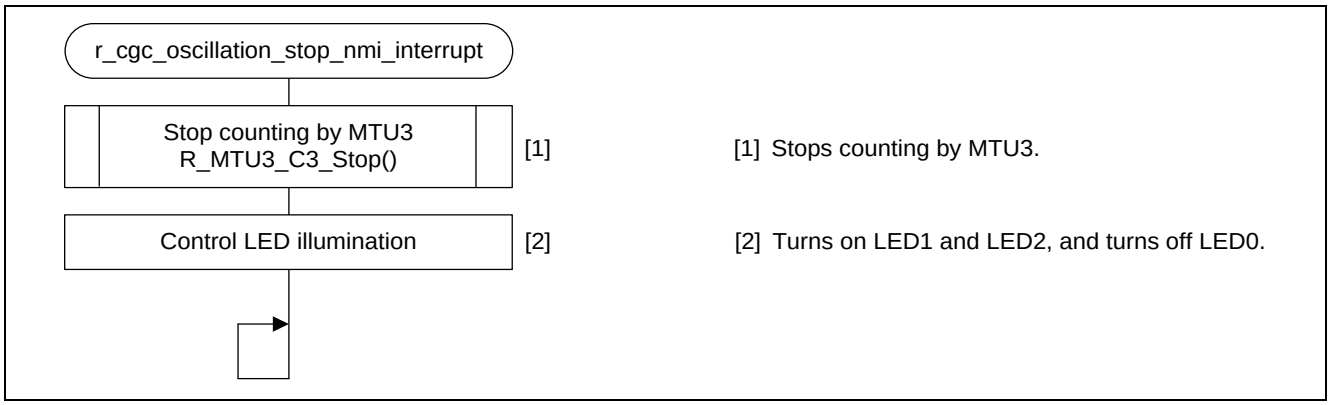


Figure 4.30 Flowchart of Oscillation Stop Detection

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

Reference Documents

User's Manual: Hardware
RX24U Group User's Manual: Hardware Rev.1.00 (R01UH0658)
(The latest versions can be downloaded from the Renesas Electronics website.)

User's Manual: RX API Reference
e^2 studio Code Generator User's Manual: RX API Reference Rev.1.30 (R20UT2864EJ0130)

User's Manual: Renesas Starter Kit
Renesas Starter Kit for RX24U User's Manual Rev.1.00 (R20UT3758EG0100)

CPU Board Schematics: Renesas Starter Kit
Renesas Starter Kit for RX24U CPU Board Schematics Rev.1.00 (R20UT3757EG0100)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

Supported Technical Updates

This application note reflects the contents of the following technical updates:

There are no supported technical updates.

Website and Support

Renesas Electronics Website

http://www.renesas.com/

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Aug. 31, 2018	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

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   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

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   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

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   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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