RX23T Group

Initial Settings Example

R01AN2551EJ0120
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Introduction

This application note describes the settings that must be made after a reset of a RX23T Group microcontroller, including clock settings, disabling of peripheral functions still running after a reset, and nonexistent port settings.

Target Devices

- RX23T Group 64-pin version, ROM capacity: 64 KB, 128 KB
- RX23T Group 52-pin version, ROM capacity: 64 KB, 128 KB
- RX23T Group 48-pin version, ROM capacity: 64 KB, 128 KB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The sample code makes settings to disable peripheral functions still running after a reset, nonexistent port settings, and clock settings. The description in this application note applies to the processing that occurs following power-on (cold start).

1.1 Disabling Peripheral Functions Still Running After a Reset

Some peripheral functions start operating immediately after power-on, and some have the module stop function disabled. The processing covered under this item disables the following functions:

DTC and RAM0

Note that the above processing is not performed by the sample code. As necessary, overwrite the corresponding constants to execute the processing.

1.2 Nonexistent Port Settings

It may be necessary to set the bits in the port direction registers corresponding to nonexistent ports to predetermined values. The sample code contains initial port direction register setting values suitable for 64-pin products. Overwrite the constants as necessary to accommodate the actual target device.

1.3 Clock Settings

1.3.1 Overview

The procedure for making clock settings is as follows:

1. Main clock settings
2. PLL clock settings
3. HOCO clock settings
4. System clock switching

By making changes to the constants defined in r_init_clock.h, the sample code described in this application note can be used to change the various clock settings.

The sample code sets the PLL clock as the system clock. Overwrite the constants as necessary to match the clocks you wish to use.

1.3.2 Clock Specifications Assumed in Sample Code

Table 1.1 lists the clock specifications assumed in sample code. Values such as the oscillation stabilization time have been calculated to match oscillators with the specifications listed in the table.

Table 1.1 Clock Specifications Assumed in Sample Code

Clock	Oscillation Frequency	Oscillation Stabilization Time	Remarks
Main clock oscillator	20 MHz	8.192 ms*2	Crystal
PLL clock	40 MHz	50 μs*3	
HOCO clock	32 MHz*1	30 μs*3	

Note 1. The clock is disabled in the sample code.

Note 2. The oscillation stabilization time of each oscillator will differ depending on conditions such as the wiring pattern of the actual system, the oscillation constant, etc. To determine the appropriate oscillation stabilization time, ask the oscillator manufacturer to evaluate the actual target system.

Note 3. See Electrical Characteristics in RX23T Group User's Manual: Hardware.

1.3.3 Clock Selection

By making changes to the constants defined in r_init_clock.h, the sample code described in this application note can be used to select settings such as the clock source of the system clock and whether each clock is oscillating or stopped. To determine which constants can be changed, see the listing of (user changeable) constants used by the sample code in Table 3.5. Table 1.2 lists clock selection examples.

Table 1.2 Clock Selection Examples

No.		1	2	3
System clock		PLL	Main clock	HOCO clock
PLL clock		Oscillating	Stopped	Stopped
Main clock		Oscillating	Oscillating	Stopped
HOCO clock		Stopped	Stopped	Oscillating
Operating power control mode		High-speed operating mode	High-speed operating mode	High-speed operating mode
Constants	SEL_SYSCLK	CLK_PLL	CLK_MAIN	CLK_HOCO
	SEL_PLL	B_USE	B_NOT_USE	B_NOT_USE
	SEL_MAIN	B_USE	B_USE	B_NOT_USE
	SEL_HOCO	B_NOT_USE	B_NOT_USE	B_USE
	REG_OPCCR	OPCM_HIGH	OPCM_HIGH	OPCM_HIGH
	REG_MEMWAIT*1	MEMWAIT_ON	MEMWAIT_OFF	MEMWAIT_OFF

Note 1. Selecting no wait cycles is prohibited when ×1/1 is selected by bits SCKCR.ICK[3:0] and a clock frequency of 32 MHz or higher is selected by bits SCKCR3.CKSEL[2:0]. In this case, select MEMWAIT_ON as the setting for REG_MEMWAIT.

2. Operation Confirmation Conditions

The operation of the sample code referenced in this application note has been confirmed under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item		Contents
MCU used		R5F523T5ADFM (RX23T Group)
Operating frequency	PLL clock selected as system clock	Main clock: 20 MHz PLL: 40 MHz (main clock ×1/2 ×4) LOCO: 4 MHz HOCO: Stopped System clock (ICLK): 40 MHz (PLL ×1/1) Peripheral module clock A (PCLKA): 40 MHz (PLL ×1/1) Peripheral module clock B (PCLKB): 40 MHz (PLL ×1/1) Peripheral module clock D (PCLKD): 40 MHz (PLL ×1/1) FlashIF clock (FCLK): 20 MHz (PLL ×1/2)
	Main clock selected as system clock	Main clock: 20 MHz PLL: Stopped LOCO: 4 MHz HOCO: Stopped System clock (ICLK): 20 MHz (main clock ×1/1) Peripheral module clock A (PCLKA): 20 MHz (main clock ×1/1) Peripheral module clock B (PCLKB): 20 MHz (main clock ×1/1) Peripheral module clock D (PCLKD): 20 MHz (main clock ×1/1) FlashIF clock (FCLK): 20 MHz (main clock ×1/1)
	HOCO clock selected as system clock	Main clock: Stopped PLL: Stopped LOCO: 4 MHz HOCO: 32 MHz System clock (ICLK): 32 MHz (HOCO ×1/1) Peripheral module clock A (PCLKA): 32 MHz (HOCO ×1/1) Peripheral module clock B (PCLKB): 32 MHz (HOCO ×1/1) Peripheral module clock D (PCLKD): 32 MHz (HOCO ×1/1) Flash interface clock (FCLK): 32 MHz (HOCO ×1/1)
Operating voltage		3.3 V
Integrated development environment		Renesas Electronics e² studio 2020-04
C compiler		Renesas Electronics C/C++ Compiler Package for RX Family V3.02.00
		Compiler option The integrated development environment default settings are used.
iodefine.h version		V1.10
Endian		Little endian
Operating mode		Single-chip mode
Processor mode		Supervisor mode
Sample code version		Version 1.20

Notes:

If the same version of the toolchain (C compiler) specified in the original project is not in the import destination, the toolchain will not be selected and an error will occur.

Check the selected status of the toolchain on the project configuration dialog.

For the setting method, refer to FAQ 3000404.

FAQ 3000404 :Program ""make"" not found in PATH’ error when attempting to build an imported project (e² studio)"

3. Software

After disabling peripheral functions still running after a reset and making nonexistent port settings, the sample code makes clock settings.

3.1 Disabling Peripheral Functions Still Running After a Reset

The sample code disables peripheral functions still running after a reset.

Only the peripheral modules listed below are not in the module stop state after a reset is canceled. To transition a module to the module stop state, set the corresponding module stop bit to 1 (transition to module stop state). Putting modules into the module stop state can reduce the power consumption of the device.

In the sample code the value of the constant MSTP_STATE_<target module name> is 0 (MODULE_STOP_DISABLE), so the target module does not transition to the module stop state. To transition one or more modules to the module stop state on the target system, set the corresponding constant(s) to 1 (MODULE_STOP_ENABLE) in r_init_stop_module.h.

Table 3.1 lists the peripheral modules that are not in the module stop state after a reset.

Table 3.1 Peripheral Modules Not in Module Stop State After a Reset

Peripheral Module	Module Stop Setting Bit	Value After Reset	Setting When Not Using Module
DTC	MSTPCRA.MSTPA28 bit	0 (module stop state canceled)	1 (transition to module stop state)
RAM0	MSTPCRC.MSTPC0 bit		

3.2 Nonexistent Port Settings

3.2.1 Processing Overview

The sample code sets the bits in the PDR registers corresponding to nonexistent ports to 1. When writing in byte units to PDR or PODR registers containing nonexistent ports after the nonexistent port initial setting function has been called, set the direction control bits corresponding to the nonexistent ports to 1 and the port output data storage bits corresponding to the nonexistent ports to 0.

3.2.2 Pin Count Setting

The setting in the sample code (PIN_SIZE=64) is for 64-pin products. The pin counts supported by this application note are 64, 52, and 48. If the pin count of the target device is other than 64, change the value of PIN_SIZE in r_init_port_initialize.h to match the target device.

3.3 Clock Settings

3.3.1 Clock Setting Procedure

Table 3.2 lists the steps in the clock setting procedure, the processing performed in each step, and the settings of the sample code. In the sample code, the main clock and the PLL clock are enabled.

Table 3.2 Clock Setting Procedure

Step	Processing	Details of Processing		Sample Code Settings
1	Main clock setting*1	Not used	This setting is unnecessary.	The main clock is used.
		Used	Sets the main clock drive capacity and sets in MOSCWTCR the waiting time until output of the main clock to the internal clocks starts, then starts oscillation by the main clock. After this, waits for the oscillation stabilization time to elapse.	
2	PLL clock setting*1	Not used	This setting is unnecessary.	The PLL clock is used.
		Used	Sets the PLL input division ratio and frequency multiplication factor, then starts oscillation by the PLL clock. After this, waits for the oscillation stabilization time to elapse.	
3	HOCO clock setting*1	Not used	This setting is unnecessary.	The HOCO clock is not used.
		Used	Starts oscillation by the HOCO clock. After this, waits for the oscillation stabilization time to elapse.	
4	Operating power control mode setting	Sets the operating power control mode according to the operating frequency and operating voltage used.		High-speed operating mode is selected.
5	Memory wait cycles setting	Specifies whether or not wait cycles are inserted for ROM. Selecting no wait cycles is prohibited when ×1/1 is selected by bits SCKCR.ICK[3:0] and a clock frequency of 32 MHz or higher is selected by bits SCKCR3.CKSEL[2:0].		Wait cycles are enabled.
6	Clock division ratio settings	Changes the clock division ratios.		• ICLK, PCLKA, PCLKB, PCLKD: ×1/1 • FCLK: ×1/2
7	System clock switching	Switches according to the system used.		Switches to PLL clock.

Note 1. Change the values of the constants in r_init_clock.h as necessary to match the selection of the clocks you wish to use or not use.

3.4 File Composition

Table 3.3 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 3.3 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing routine	
r_init_stop_module.c	Disable peripheral functions still running after a reset	
r_init_stop_module.h	Header file of r_init_stop_module.c	
r_init_port_initialize.c	Initial nonexistent port settings	
r_init_port_initialize.h	Header file of r_init_port_initialize.c	
r_init_clock.c	Initial clock settings	
r_init_clock.h	Header file of r_init_clock.c	

3.5 Option-Setting Memory

Table 3.4 lists the option-setting memory configured in the sample code. When necessary, set a value suited to the user system.

Table 3.4 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FFFF FF8Fh to FFFF FF8Ch	FFFF FFFFh	IWDT stopped after a reset
OFS1	FFFF FF8Bh to FFFF FF88h	FFFF FFFFh	Voltage monitor 0 reset disabled after a reset HOCO oscillation is disabled after a reset
MDE	FFFF FF83h to FFFF FF80h	FFFF FFFFh	Little endian

3.6 Constants

Table 3.5 lists the (user changeable) constants used by the sample code, Table 3.6 lists the (non user changeable) constants, Table 3.7 lists the constants specific to 64-pin products (PIN_SIZE=64), Table 3.8 lists the constants specific to 52-pin products (PIN_SIZE=52), and Table 3.9 lists the constants specific to 48-pin products (PIN_SIZE=48).

Table 3.5 Constants (User Changeable) Used by Sample Code

Constant Name	Setting Value	Contents
SEL_MAIN*1	B_USE	Main clock enable/disable selection B_USE: Used (main clock enabled) B_NOT_USE: Not used (main clock disabled)
REG_MOFCR*1	20h	Main clock oscillator drive capacity setting (setting value of MOFCR register)
REG_MOSCWTCR*1	06h	Setting value of main clock wait control register
SEL_HOCO*1	B_NOT_USE	HOCO enable/disable selection B_USE: Used (HOCO clock enabled) B_NOT_USE: Not used (HOCO clock disabled)
SEL_PLL	B_USE	PLL clock enable/disable selection B_USE: Used (PLL clock enabled) B_NOT_USE: Not used (PLL clock disabled)
REG_PLLCR	0701h	PLL input division ratio and frequency multiplication factor settings (setting value of PLLCR register)
SEL_SYSCLK*1	CLK_PLL	System clock clock source selection CLK_MAIN: Main clock CLK_PLL: PLL clock CLK_HOCO: HOCO clock
REG_OPCCR*1	OPCM_HIGH	Operating power control mode selection*4 OPCM_HIGH: High-speed operating mode OPCM_MID: Mid-speed operating mode
REG_MEMWAIT	MEMWAIT_ON	Memory wait cycle selection MEMWAIT_ON: Wait cycles enabled MEMWAIT_OFF: Wait cycles disabled
MSTP_STATE_DTC*2	MODULE_STOP_DISABLE	DTC module stop state selection MODULE_STOP_DISABLE: Disable module stop MODULE_STOP_ENABLE: Transition to module stop
MSTP_STATE_RAM0*2	MODULE_STOP_DISABLE	RAM0 module stop state selection MODULE_STOP_DISABLE: Operating MODULE_STOP_ENABLE: Stopped
PIN_SIZE*3	64	Pin count of target device

Note 1. Change the settings values in r_init_clock.h to match the target system.
Note 2. Change the settings values in r_init_stop_module.h to match the target system.
Note 3. Change the settings values in r_init_port_initialize.h to match the target system.
Note 4. The operating frequency range and operating voltage range differ depending on the operating mode. For details, see RX23T Group User's Manual: Hardware.

Table 3.6 Constants (Non User Changeable) Used by Sample Code

Constant Name	Setting Value	Contents
B_NOT_USE	0	Not used
B_USE	1	Used
CLK_HOCO	0100h	Clock source: HOCO
CLK_MAIN	0200h	Clock source: Main clock
CLK_PLL	0400h	Clock source: PLL
REG_SCKCR*1	1000 0000h (PLL selected) 0000 0000h (MAIN or HOCO selected)	Internal clock division ratio (setting value of SCKCR register)
OPCM_MID	02h	Operating power control mode: Mid-speed operating mode
OPCM_HIGH	00h	Operating power control mode: High-speed operating mode
MEMWAIT_OFF	00h	Memory wait cycles disabled
MEMWAIT_ON	01h	Memory wait cycles enabled
MODULE_STOP_ENABLE	1	Transition to module stop state
MODULE_STOP_DISABLE	0	Cancel module stop state

Note 1. The setting value differs depending on the selected system clock clock source.

Table 3.7 Constants for 64-Pin Products (PIN_SIZE=64)

Constant Name	Setting Value	Contents
DEF_P0PDR	F8h	Port P0 direction register setting value
DEF_P1PDR	FCh	Port P1 direction register setting value
DEF_P2PDR	E3h	Port P2 direction register setting value
DEF_P3PDR	30h	Port P3 direction register setting value
DEF_P4PDR	00h	Port P4 direction register setting value
DEF_P7PDR	80h	Port P7 direction register setting value
DEF_P9PDR	E1h	Port P9 direction register setting value
DEF_PAPDR	C3h	Port PA direction register setting value
DEF_PBPDR	00h	Port PB direction register setting value
DEF_PDPDR	07h	Port PD direction register setting value

Table 3.8 Constants for 52-Pin Products (PIN_SIZE=52)

Constant Name	Setting Value	Contents
DEF_P0PDR	FBh	Port P0 direction register setting value
DEF_P1PDR	FCh	Port P1 direction register setting value
DEF_P2PDR	E3h	Port P2 direction register setting value
DEF_P3PDR	37h	Port P3 direction register setting value
DEF_P4PDR	00h	Port P4 direction register setting value
DEF_P7PDR	80h	Port P7 direction register setting value
DEF_P9PDR	E7h	Port P9 direction register setting value
DEF_PAPDR	D3h	Port PA direction register setting value
DEF_PBPDR	00h	Port PB direction register setting value
DEF_PDPDR	87h	Port PD direction register setting value

Table 3.9 Constants for 48-Pin Products (PIN_SIZE=48)

Constant Name	Setting Value	Contents
DEF_P0PDR	FFh	Port P0 direction register setting value
DEF_P1PDR	FCh	Port P1 direction register setting value
DEF_P2PDR	E3h	Port P2 direction register setting value
DEF_P3PDR	3Fh	Port P3 direction register setting value
DEF_P4PDR	00h	Port P4 direction register setting value
DEF_P7PDR	80h	Port P7 direction register setting value
DEF_P9PDR	E7h	Port P9 direction register setting value
DEF_PAPDR	F3h	Port PA direction register setting value
DEF_PBPDR	80h	Port PB direction register setting value
DEF_PDPDR	87h	Port PD direction register setting value

3.7 Functions

Table 3.10 lists the functions.

Table 3.10 Functions

Function Name	Outline
main	Main processing routine
R_INIT_StopModule	Disable peripheral functions still running after a reset
R_INIT_Port_Initialize	Initial nonexistent port settings
R_INIT_Clock	Initial clock settings
CGC_oscillation_main	Main clock oscillation enable
CGC_oscillation_HOCO	HOCO clock oscillation enable
CGC_oscillation_PLL	PLL clock oscillation enable

3.8 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing routine
Header	None
Declaration	void main(void)
Description	Calls the settings function for disabling peripheral functions still running after a reset, the initial nonexistent port settings function, and the initial clock settings function.
Arguments	None
Return Value	None

R_INIT_StopModule	
Outline	Disable peripheral functions still running after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Makes settings to transition to the module stop state.
Arguments	None
Return Value	None
Remarks	In the sample code, no transition to the module stop state occurs.

R_INIT_Port_Initialize	
Outline	Initial nonexistent port settings
Header	r_init_port_initialize.h
Declaration	void R_INIT_Port_Initialize(void)
Description	Makes initial settings to the port direction registers corresponding to the pins of nonexistent port.
Arguments	None
Return Value	None
Remarks	The setting in the sample code (PIN_SIZE=64) is for 64-pin products. When writing in byte units to PDR or PODR registers containing nonexistent ports after this function has been called, set the direction control bits corresponding to the nonexistent ports to 1 and the port output data storage bits corresponding to the nonexistent ports to 0.

R_INIT_Clock	
Outline	Initial clock settings
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Makes initial clock settings.
Arguments	None
Return Value	None
Remarks	In the sample code processing is selected that sets the PLL clock as the system clock.

CGC_oscillation_main	
Outline	Main clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_main (void)
Description	Sets the drive capacity of the main clock and sets the MOSCWTCR register, then starts oscillation of the main clock. After this, waits for the main clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

CGC_oscillation_HOCO	
Outline	HOCO clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_HOCO (void)
Description	Enables the HOCO oscillation. After this, waits for the HOCO clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

CGC_oscillation_PLL	
Outline	PLL clock oscillation enable
Header	r_init_clock.h
Declaration	void CGC_oscillation_PLL (void)
Description	Sets the PLL input division ratio and frequency multiplication factor, then starts oscillation of the PLL clock. After this, waits for the PLL clock oscillation stabilization waiting time.
Arguments	None
Return Value	None

3.9 Flowcharts

3.9.1 Main Processing

Figure 3.1 shows the main processing.

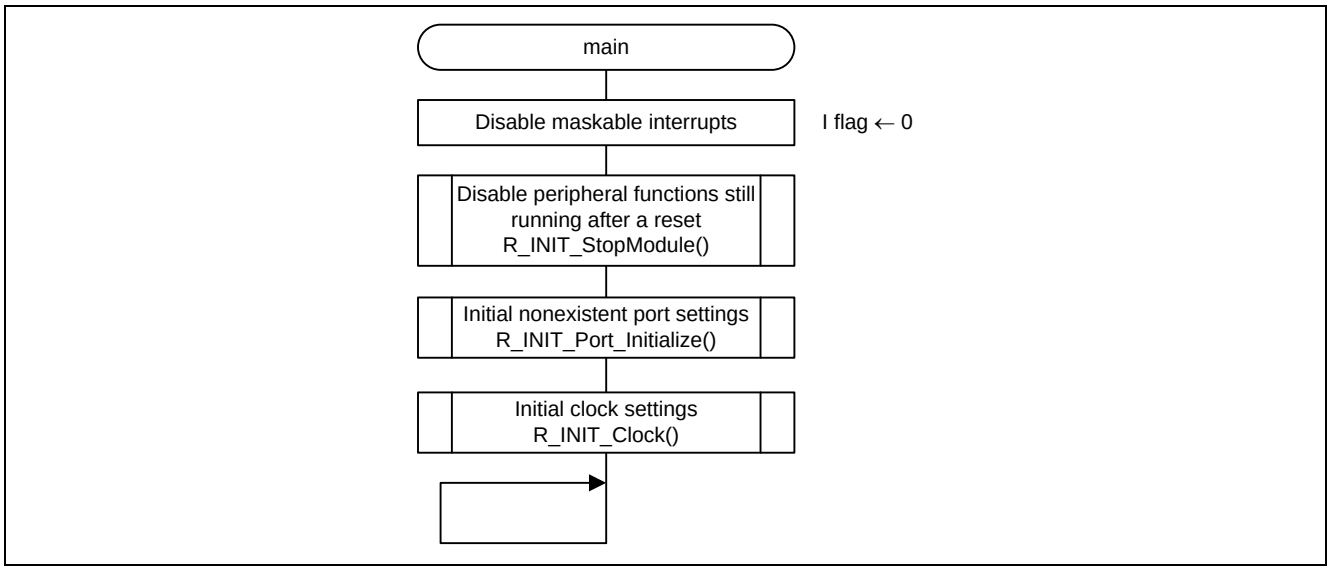
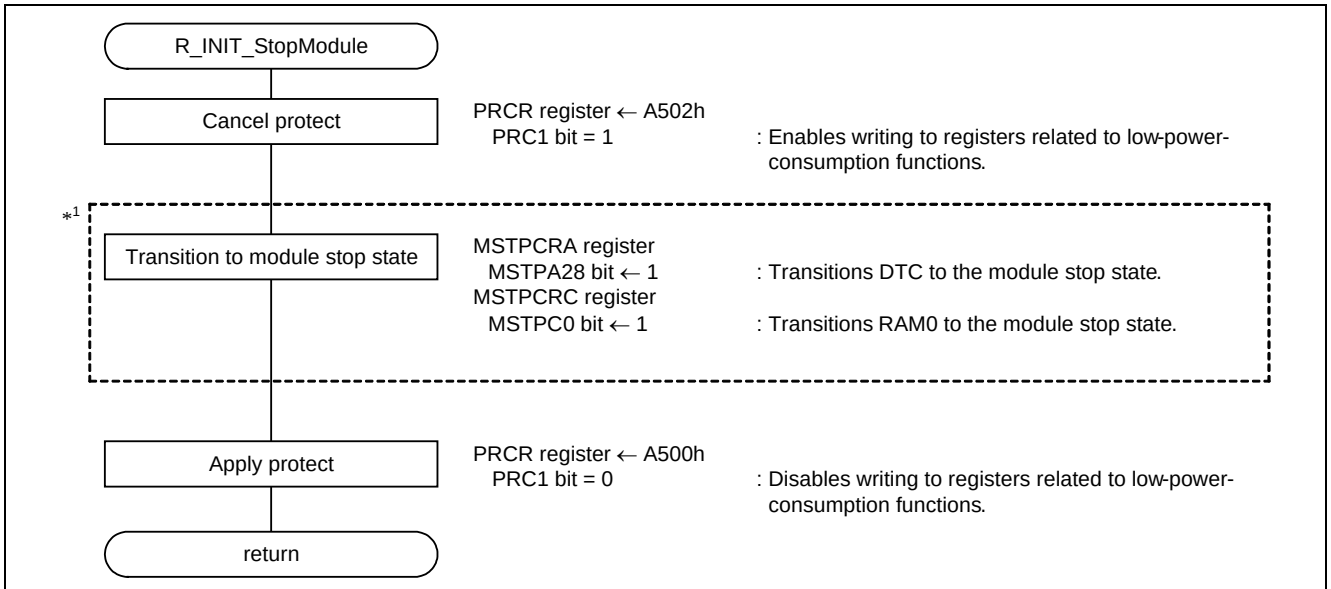


Figure 3.1 Main Processing

3.9.2 Disable Peripheral Functions Still Running After a Reset

Figure 3.2 is a flowchart of the processing for disabling of peripheral functions still running after a reset.



Note 1. In the sample code the module stop state is canceled. To transition to the module stop state, set the corresponding constant #define MSTP_STATE_<target module name> to 1.

Figure 3.2 Disable Peripheral Functions Still Running After a Reset

3.9.3 Initial Nonexistent Port Settings

Figure 3.3 is a flowchart of the processing for making initial nonexistent port settings.

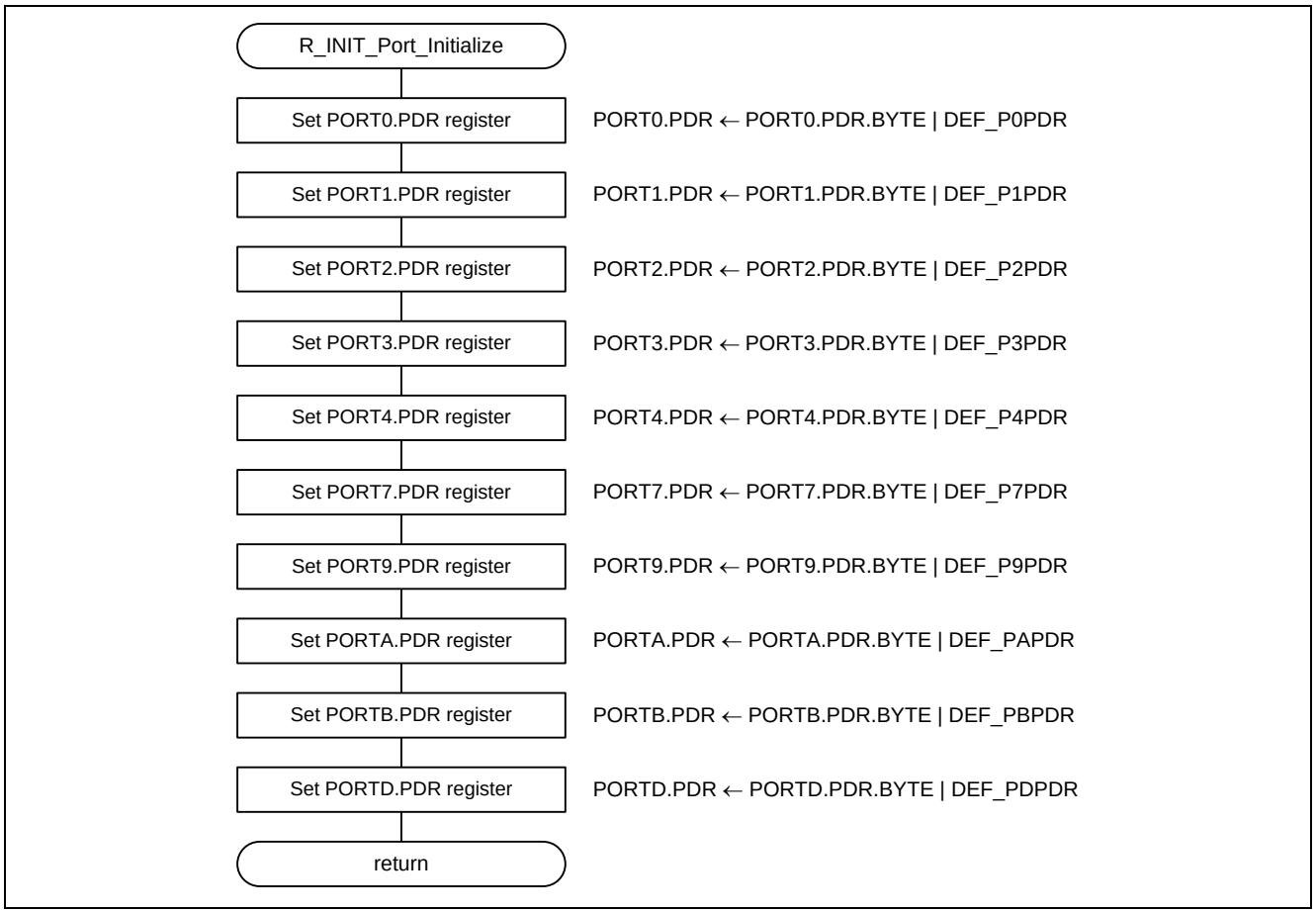
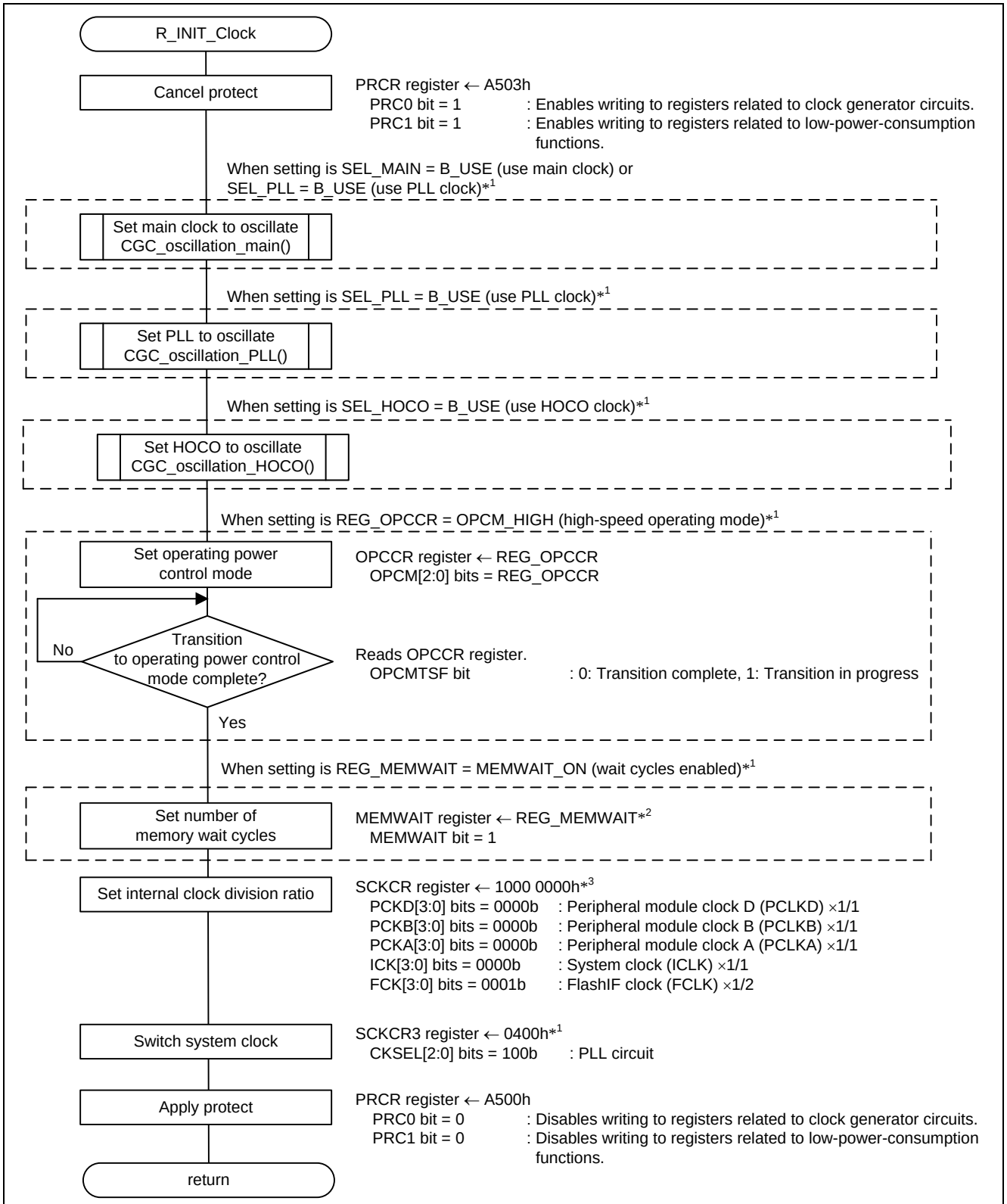


Figure 3.3 Initial Nonexistent Port Settings

3.9.4 Initial Clock Settings

Figure 3.4 is flowchart of the processing for making initial clock settings.

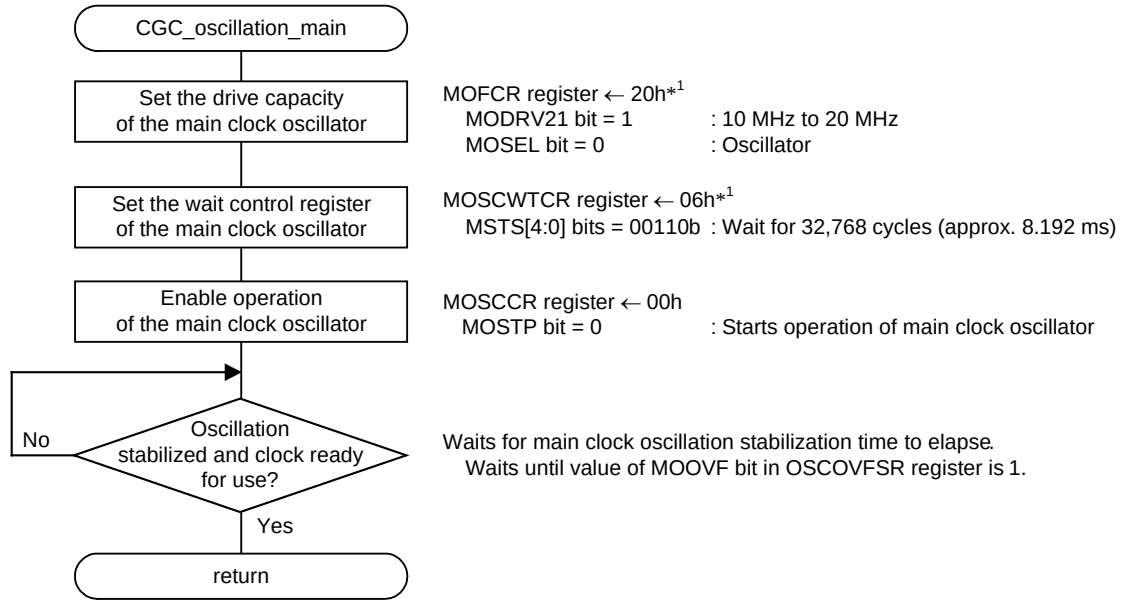


Note 1. Change the values of the relevant constants to match the characteristics of the target system.
Note 2. After writing to the MEMWAIT register, use the read value of the MEMWAIT register to perform calculations.
Note 3. The setting values differ depending on the system clock selected by the constant.

Figure 3.4 Initial Clock Settings

3.9.5 Main Clock Oscillation Enable

Figure 3.5 is a flowchart of the processing for starting oscillation of the main clock.



Note 1. Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.5 Main Clock Oscillation Enable

3.9.6 HOCO Clock Oscillation Enable

Figure 3.6 is a flowchart of the processing for starting oscillation of the HOCO clock.

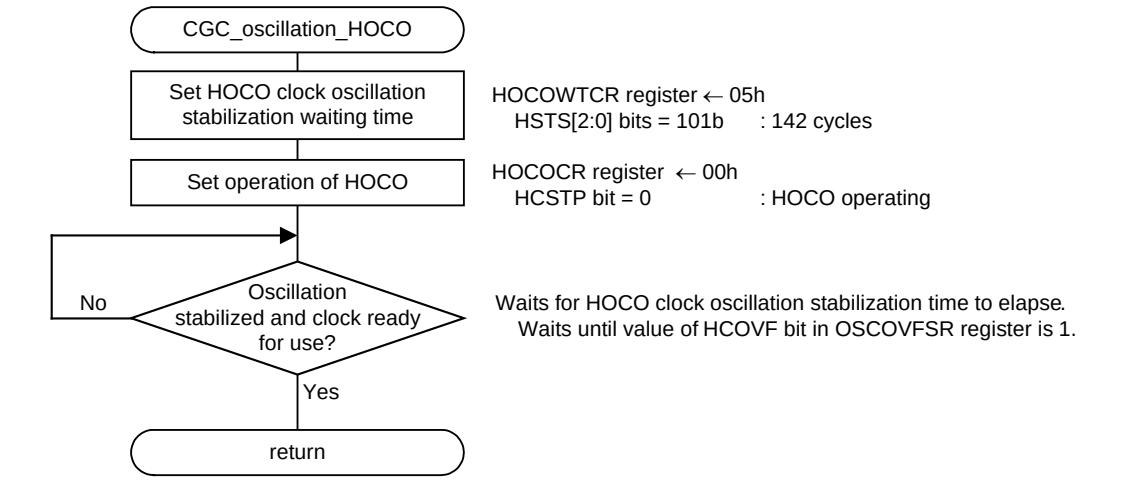
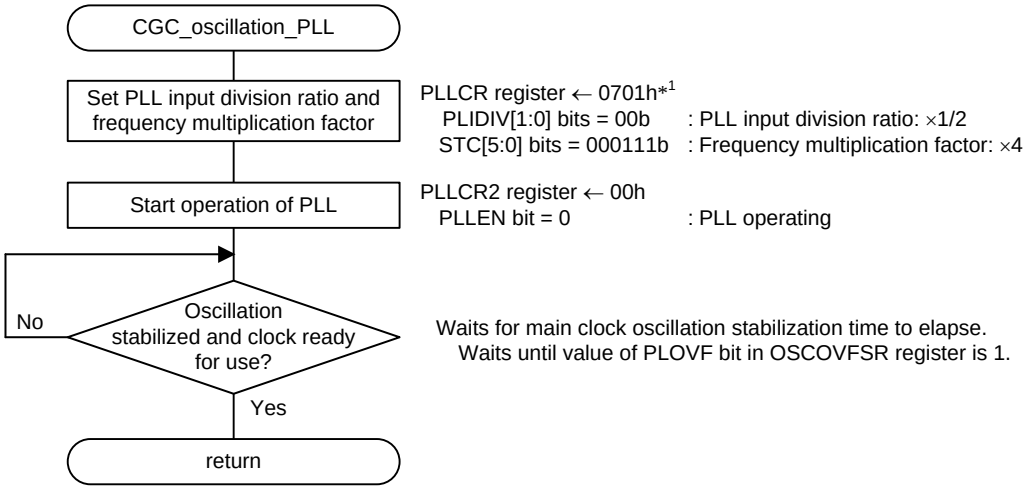


Figure 3.6 HOCO Clock Oscillation Enable

3.9.7 PLL Clock Oscillation Enable

Figure 3.7 is a flowchart of the processing for starting oscillation of the PLL clock.



Note 1. Change the values of the relevant constants to match the characteristics of the target system.

Figure 3.7 PLL Clock Oscillation Enable

4. Importing a Project

4.1 Importing a Project into e² studio

Follow the steps below to import your project into e² studio.

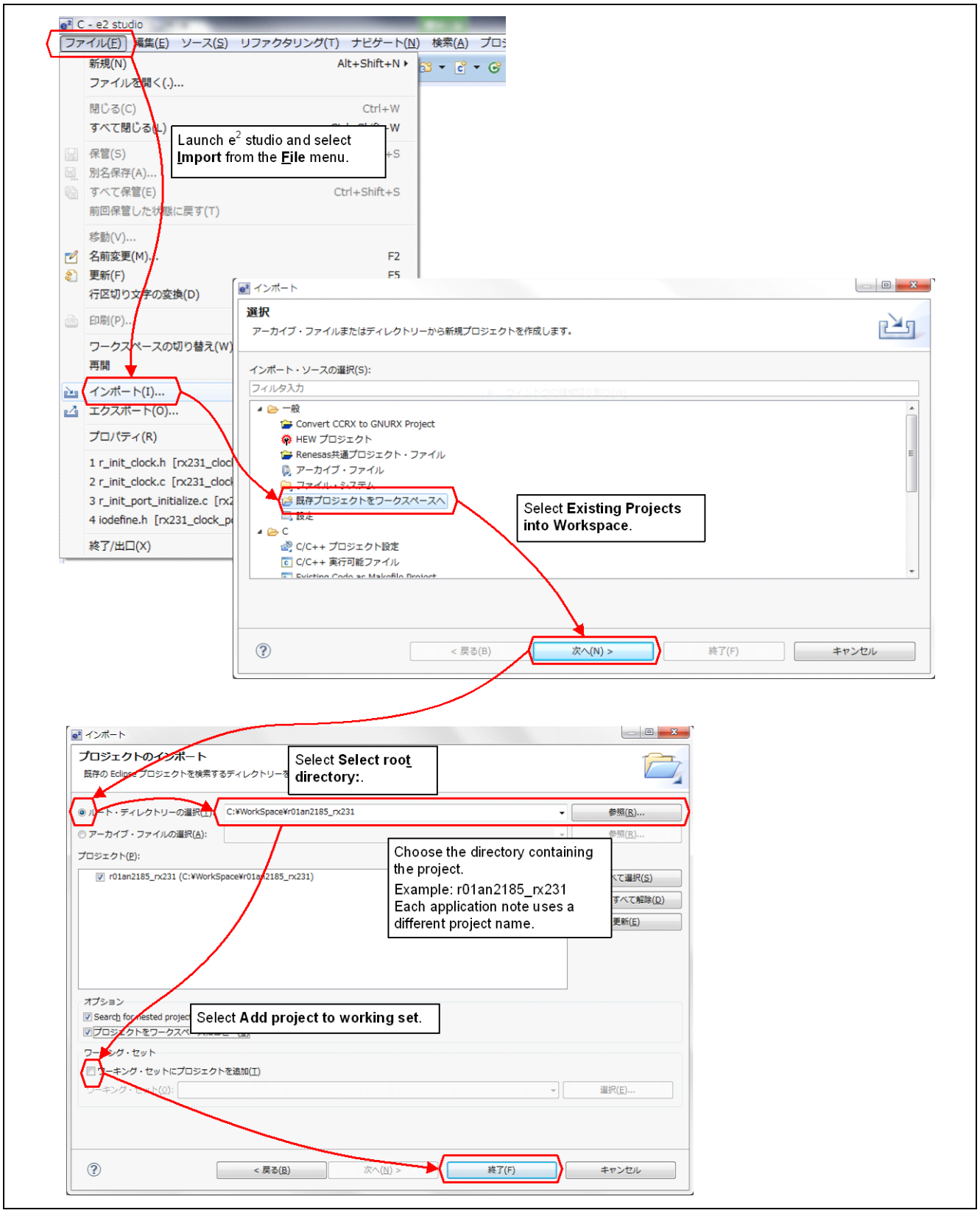


Figure 4.1 Importing a Project into e² studio

4.2 Importing a Project into CS+

Follow the steps below to import your project into CS+.

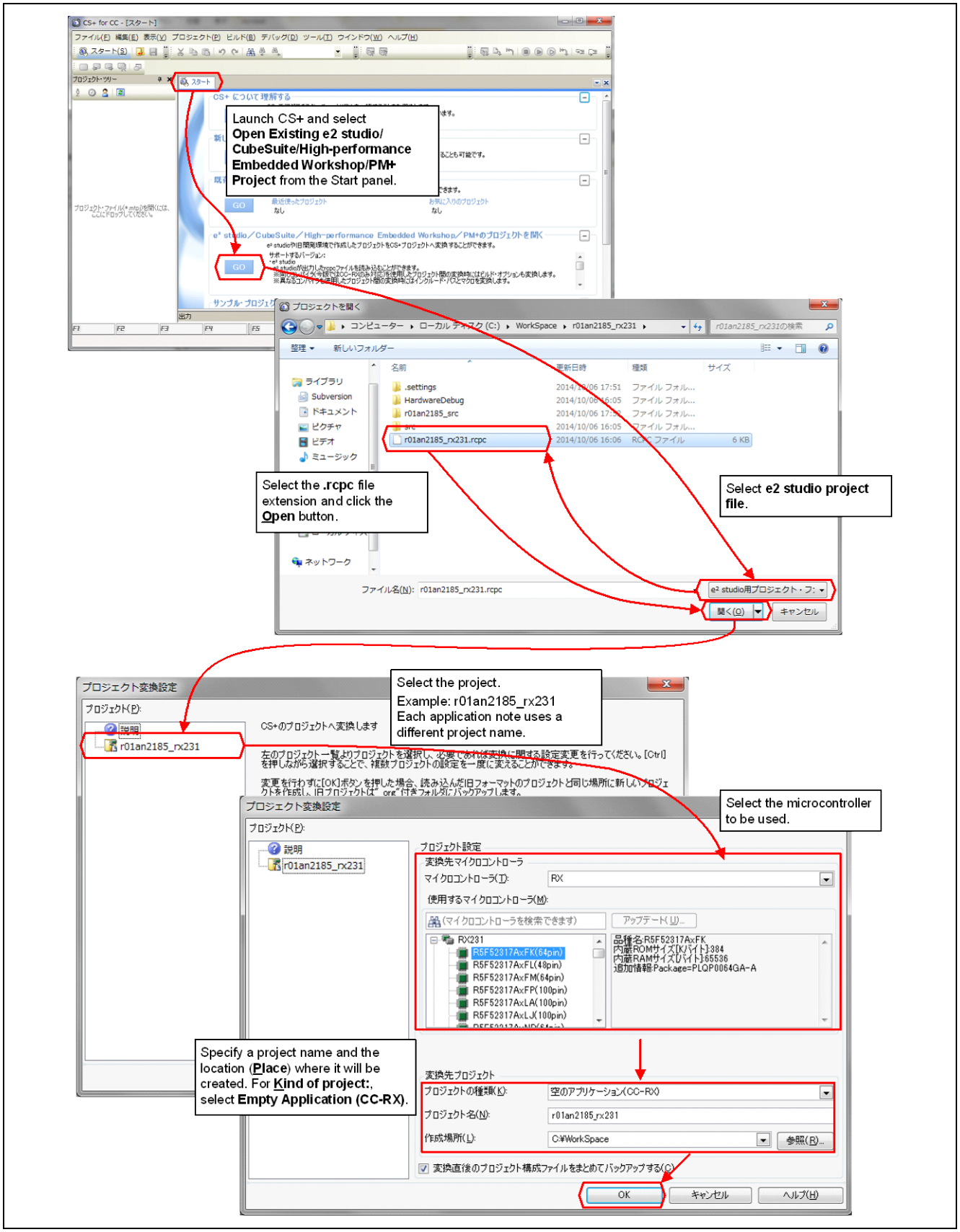


Figure 4.2 Importing a Project into CS+

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

User's Manual: Development Tools

[CS+][e^2 studio] RX C/C++ Compiler CC-RX User's Manual (R20UT3248EJ0101)
(The latest version can be downloaded from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun. 17, 2015	—	First edition issued
1.10	May 25, 2016	3	Added HOCO clock settings to 1.3.1 Changed oscillation frequency of main clock oscillator in Table 1.1 Added HOCO clock to Table 1.1
		4	Added HOCO clock to Table 1.2 as No. 3
		5	Changed oscillation frequency of main clock oscillator in Table 2.1 Added HOCO clock to Table 2.1
		7	Added HOCO clock settings to Table 3.2
		8	Added information about HOCO oscillation after a reset to description of OFS1 in Table 3.4
		9	Added constant SEL_HOCO to Table 3.5 Changed setting value of constant REG_PLLCR in Table 3.5
		10	Added constant CLK_HOCO to Table 3.6
		11	Added function CGC_oscillation_HOCO to Table 3.10
		13	Added function CGC_oscillation_HOCO
		16	Added HOCO clock oscillation setting to Figure 3.4
		17	Added HOCO clock oscillation enable flowchart as Figure 3.6
		18	Changed PLLCR register setting value in Figure 3.7
1.20	Jul.1.2020	—	Update the toolchain version

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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