RX23E-A Group RX23E-B Group

Effective use of AFE and DSAD

Overview

This document describes methods to implement various processing carried out for sensor use on RX23E-A and RX23E-B (hereafter, collectively referred to as 'RX23E') as well as important points of peripheral circuits and board design to bring out analog performance of RX23E-A.

Target device

RX23E-A

RX23E-B

Contents

1. Analog Front End (AFE) and 24-bit Δ-Σ A/D Converter (DSAD)

1.1 Δ-Σ A/D Converter

RX23E incorporates 24-bit Δ-Σ A/D converter (DSAD).

Principle diagram of Δ-Σ A/D converter is shown in

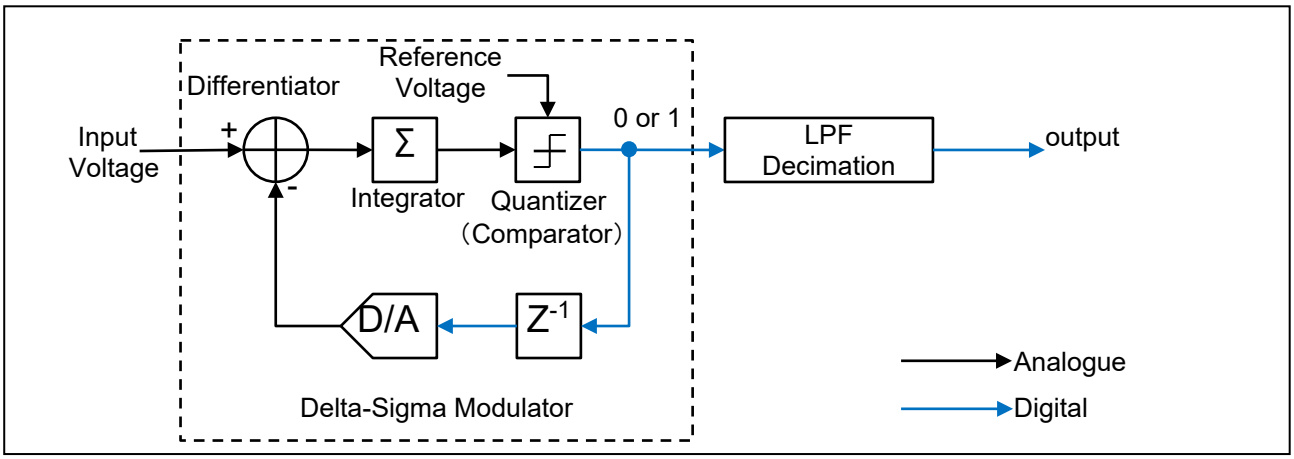


Figure 1-1 Principle diagram of Δ-Σ A/D converter

Δ-Σ A/D converter consists of Δ-Σ modulator and low-pass filter/decimation processing.

The Δ-Σ modulator compares the results of accumulating differences between the input voltage and the voltage corresponding to the previous A/D conversion value with the reference voltage to output with 2 values of 0 and 1.

Sampling rate of the Δ-Σ modulator is normally high enough for the frequency component of input signal, therefore anti-aliasing filter can be simplified or is not necessary. Besides it does not become fixed value to DC voltage input and appears as swing of 0 and 1. This is the frequency component high enough for that of the input signal.

The results of the A/D conversion by the Δ-Σ modulator are decimated by oversampling ratio through digital filter with low-pass characteristics.. Since the Δ-Σ modulator has noise shaping characteristics, quantization noises shift to high frequency range. Furthermore, by suppressing the noise components which were attracted to the high frequency range, bit resolution can be increased while decimating with the digital filter.

DSAD mounted on RX23E converts analog signal into digital at the sampling frequency, and eliminates and decimates high frequency by using SINC4 filter as digital filter, of which frequency characteristic is determined by oversampling ratio.

The comparison between DSAD on RX23E-A and RX23E-B is shown in .

Table 1-1 Comparison of DSAD

Function		RX23E-A	RX23E-B
Recommended sampling frequency (F_{MOD})		Normal Mode: 0.5MHz Low Power Mode: 0.125MHz	4MHz
Digital filter	Type	SINC4	SINC4+SINC4 SINC5+SINC1
	Oversampling ratio (data rate)	32 – 65536 (15.625kSPS – 7.629SPS: Normal Mode)	32 – 1048576 (125kSPS – 3.815SPS)

1.2 A/D conversion of Multiple Signals with Channel Function

RX23E uses channel function to set up A/D conversion condition for each of multiple signals and are capable of A/D conversion one by one. With One DSAD, RX23E-A can convert six channels of A/D conversion at maximum, RX23E-B can convert eight channels at maximum.

The channel function enables to mainly set up the following conditions as the condition of A/D conversion for each input signal.

- Input pin
- Reference voltage of A/D conversion
- Gain setting of PGA
- Oversampling ratio (OSR) of Digital filter
- Correction coefficient of Digital filter gain (RX23E-B)
- Correction factor of Offset/gain
- Averaging value function (RX23E-A)

This section describes the example of converting signals from analog into digital by one sample each time under each condition by allocating three input signals to each channel in order of channel 0, 1, 2 using DSAD0. Block diagram is shown in .

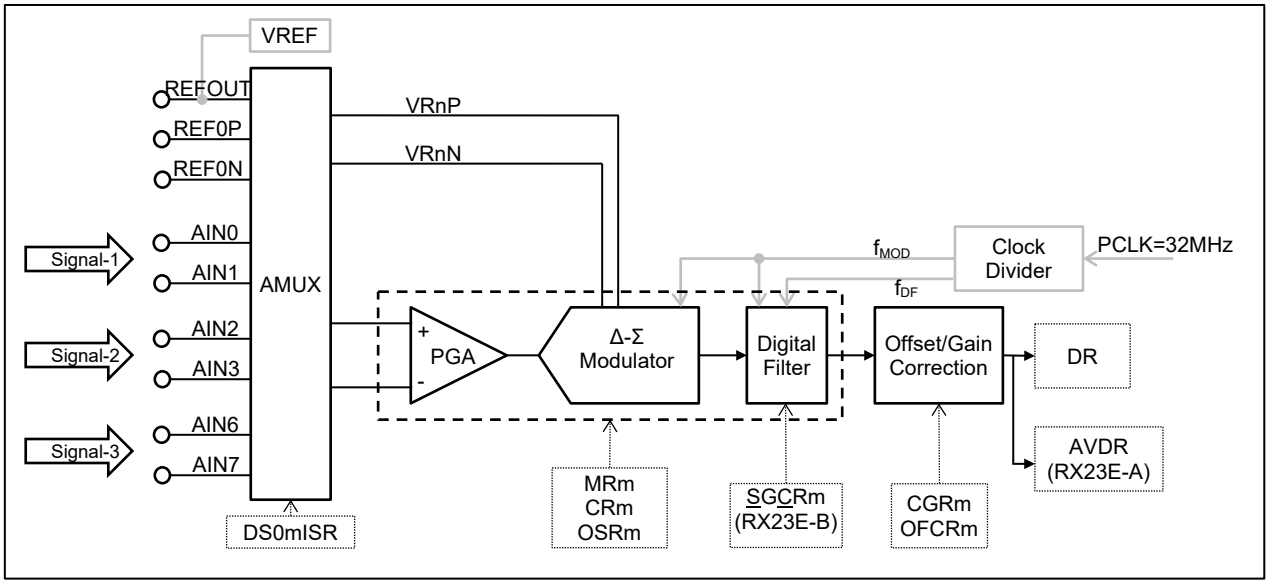


Figure 1-2 DSAD0 block diagram

The sequence of A/D conversion is shown in , and the example of DSAD0 conversion condition for each input signal is shown in and .

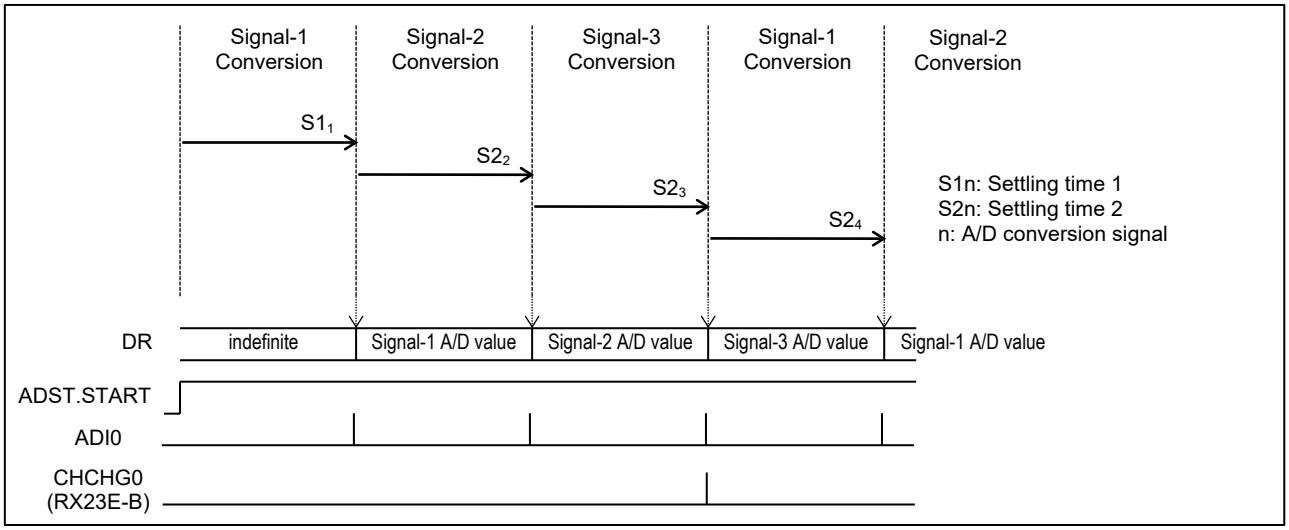


Figure 1-3 A/D conversion sequence

Table 1-2 Example of DSAD0 conversion condition for input signal (RX23E-A)

Normal Mode: f_{MOD} = 0.5MHz

Channel			0	1	2	Remarks
Input signal			1	2	3	
Setting	Input pin		+: AIN0 –: AIN1	+: AIN2 –: AIN3	+: AIN6 –: AIN7	
	PGA gain		x32	x16	x128	
	Reference voltage	+	REF0P	AVCC0	REFOUT	
		-	REF0N	AVSS0	AVSS0	
	OSR		50000	10000	8336	Oversampling ratio setting
A/D conversion time (settling time)		$S1_n$	400.259ms			-
		$S2_n$	400.256ms	80.256ms	66.944ms	time for digital filter processing, Stability waiting time
Data rate			1.8266 SPS/ch			$1/\sum_{i=0}^{2} S2_i$

Table 1-3 Example of DSAD0 conversion condition for input signal (RX23E-B)

f_{MOD} = 4MHz

Channel			0	1	2	Remarks
Input signal			1	2	3	
Setting	Input pin		+: AIN0 –: AIN1	+: AIN2 –: AIN3	+: AIN6 –: AIN7	
	PGA gain		x32	x16	x128	
	Reference voltage	+	REF0P	AVCC0	REFOUT	
		-	REF0N	AVSS0	AVSS0	
	Digital Filter		SINC4+SINC4	SINC4+SINC4	SINC4+SINC4	
	OSR		50176	10240	8192	Oversampling ratio setting OSR =OSR1 x OSR2
		OSR1	256	256	256	
		OSR2	196	40	32	
A/D conversion time (settling time)		$S1_n$	50.45766ms	-	-	
		$S2_n$	50.45725ms	10.52125ms	8.47325ms	
Data rate			14.39848528 SPS/ch			$= 1/\sum_{i=0}^{2} S2_i$

1.3 Built-in Digital Filter

1.3.1 Select RX23E-B Built-in Digital Filter

The digital filter built in RX23E-B is implemented as a two stage filter structure. SINC4+SINC4 or SINC5+SINC1 can be selected as the first stage + second stage.

The over sampling ratio for the first stage filter is OSR1, and that for the second stage filter is OSR2, and the whole oversampling ratio OSR is obtained by multiplication OSR1 x OSR2. Only when OSR1 is 256, OSR2 can be set over 1.

shows the settling time 2 of the digital filter. As shown in , the settling time 2 is the time required for the first A/D conversion result output at channel switching. When OSR is 256 or less, only the first stage filter is processed, then SINC4+SINC4 achieves shorter settling time 2 since its filter order is lower. On the other hand, when OSR exceeds 256, SINC5+ SINC1 achieves shorter settling time 2 since its filter order is lower.

shows the RMS noise when PGA gain is 16. The higher the filter order, the lower the RMS noise. Therefor, when OSR is 256 or less, SINC5+SINC1 achieves lower RMS noise, and when OSR exceeds 256, SINC4+SINC4 achieves lower RMS noise.

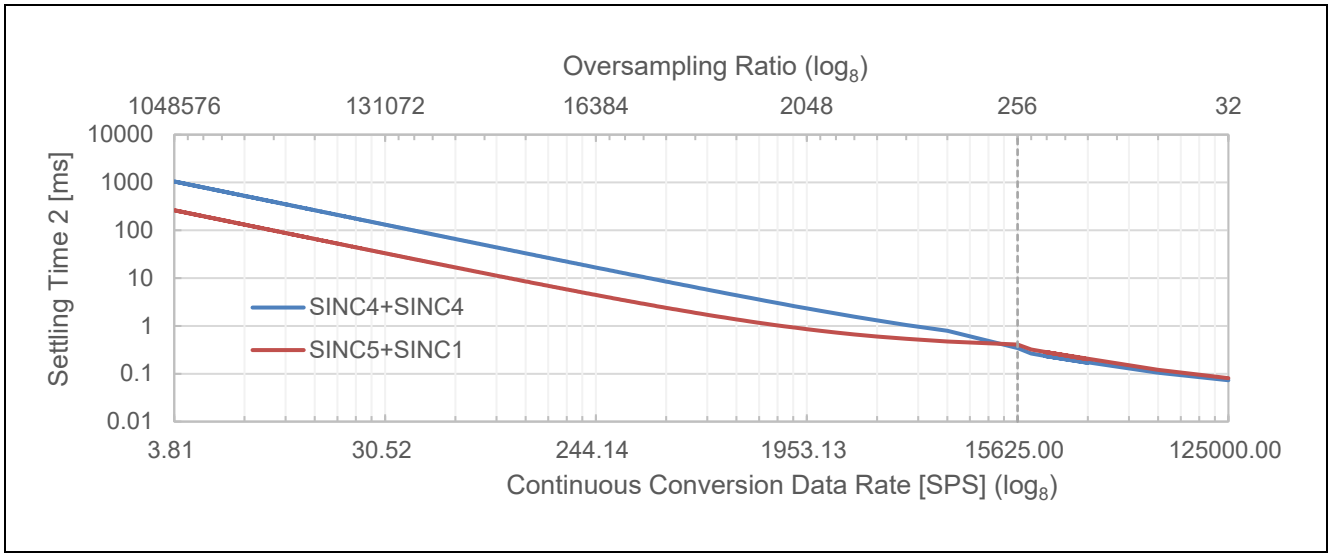


Figure 1-4 Comparison of setting time 2

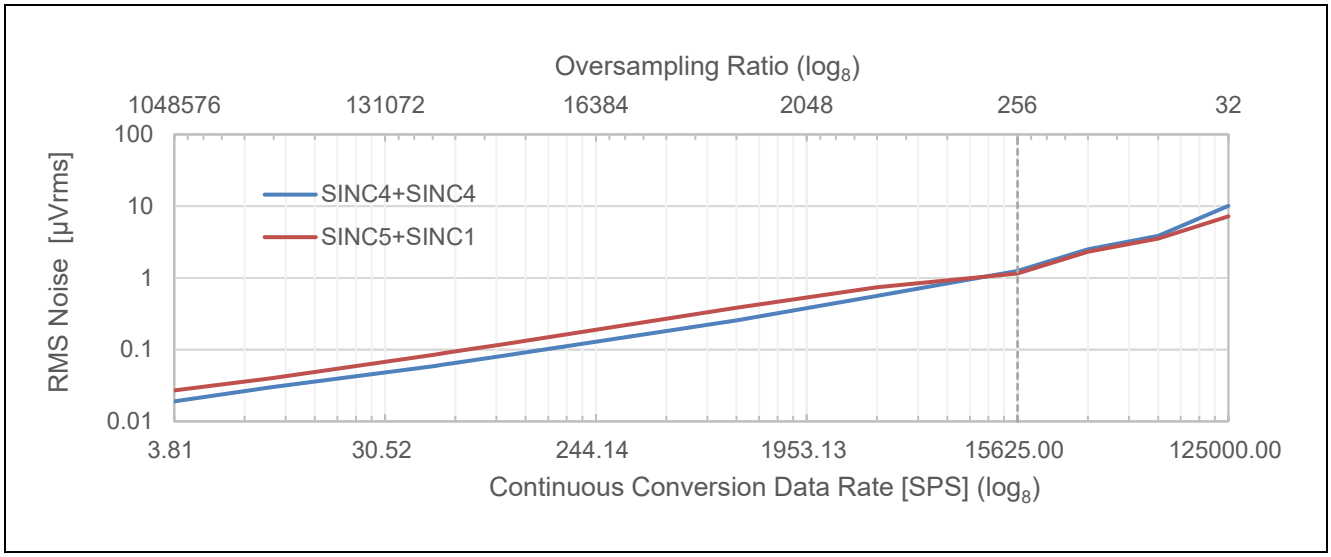


Figure 1-5 Comparison of RMS Noise (PGA Gain=16)

1.3.2 Gain Corrections

If the oversampling ratio is not a power of two, the built-in digital filter of the DSAD generates a gain. This section describes the digital filter gain and the correction methods for each device.

For details, refer to the User's Manual: Hardware for each device.

1.3.2.1 RX23E-A

The digital filter gain is described with the equation below.

$$G_{DF} = \frac{1}{2^{(Ceil(4\log_2 OSR)-4\log_2 OSR)}}$$

The gain can be corrected by either of two ways below.

(1) Multiply the A/D conversion result by $1/G_{DF}$

(2) Multiply the setting value of the gain correction register GCRm by $1/G_{DF}$ and set the result to GCRm again.
GCRm = GCRm * $1/G_{DF}$

1.3.2.2 RX23E-B

The digital filter gain is described with the equation below. The orders of the first and second stage filters are determined depending on the type of the selected digital filter.

$$G_{DF} = \frac{1}{2^{(Ceil(N1\cdot\log_2 OSR1)-N1\log_2 OSR1)}} \cdot \frac{1}{2^{(Ceil(N2\cdot\log_2 OSR2)-N2\log_2 OSR2)}}, \begin{cases} N1\text{: First stage digital filter order} \\ N2\text{: Second stage digital filter order} \end{cases}$$

$SINC4 + SINC4: N1 = 4, N2 = 4$
$SINC5 + SINC1: N1 = 5, N2 = 1$

The gain can be corrected by either of two ways below.

(1) Multiply the A/D conversion result by $1/G_{DF}$

(2) Set the value the digital filter gain correction register SGCRm by the following equation.
SGCRm = H'00400000 / G_{DF}

1.4 Remove Commercial Power Frequency Noise

Example of removing commercial power frequency noise of 50Hz/60Hz is described separately depending on the relation between noise frequency and necessary bandwidth.

1.4.1 In case of Higher than Necessary Bandwidth

If noise frequency is higher than the necessary bandwidth, remove it with the built-in digital filter.

Set oversampling ratio utilizing the low-pass characteristics of the built-in digital filter so that the notch comes to the frequency to remove. Refer to the “User’s Manual: Hardware” of RX23E-A group or RX23E-B group for details.

1.4.2 In case of Within the Necessary Bandwidth or Lower

If commercial power frequency noise is within the necessary bandwidth or lower than necessary bandwidth, it can be removed by processing with digital filter using the software. The band elimination filter is effective in case that noise is within the necessary bandwidth, and the band-pass filter or high-pass filter is effective in case that noise is out of the necessary bandwidth.

1.4.2.1 Band Eliminate Filter

This section describes the example of band elimination filter removing components which exists from 50Hz to 60Hz by IIR Biquad filtering operation. In this example, floating-point arithmetic is carried out using Biquad IIR of “RX DSP library V5.0 R01AN4359”.

Transfer function for IIR Biquad filter shown in is described with the below equation.

$$H(z) = \prod_{m=1}^{M} \frac{b_0^m + b_1^m * Z^{-1} + b_2^m * Z^{-2}}{1 + a_1^m * Z^{-1} + a_2^m * Z^{-2}}$$

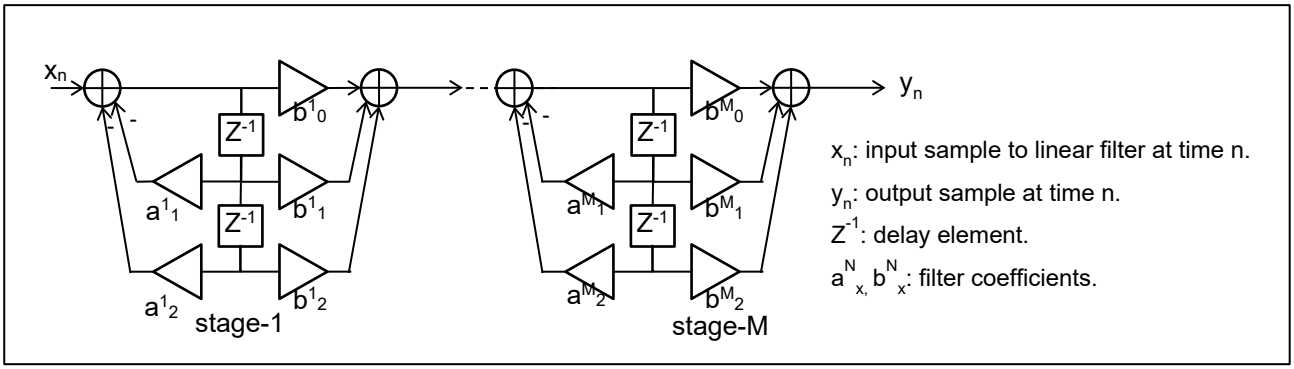


Figure 1-6 IIR Biquad filter (Two-stage cascade)

As the frequency error of the commercial power supply is ±0.3Hz, coefficients of the band elimination filter designed under the following filter condition is shown in . Frequency characteristic is shown in .The number of IIR Biquad filter stage has been realized with 10 stages.

Sampling frequency:	1000[Hz]: determine by output data rate of DSAD
Lower passband edge frequency:	42[Hz]
Lower stopband edge frequency:	48[Hz]
Higher stopband edge frequency:	62[Hz]
Higher passband edge frequency:	70[Hz]
Passband attenuation	0.5[dB]
Stopband attenuation:	48[dB]

Table 1-4 Band elimination filter coefficient

Band	Coefficient	Value	Band	Coefficient	Value
1	b0	-1.759983012	6	b0	-1.728177942
	b1	0.859464848		b1	0.878290095
	b2	0.859754821		b2	1.0
	a1	-1.620427124		a1	-1.884754914
	a2	0.859754821		a2	1.0
2	b0	-1.734986523	7	b0	-1.869770676
	b1	0.849769017		b1	0.943952367
	b2	1.0		b2	0.927312973
	a1	-1.884754914		a1	-1.747757683
	a2	1.0		a2	0.927312973
3	b0	-1.79337287	8	b0	-1.751726936
	b1	0.880852509		b1	0.917752298
	b2	0.871253429		b2	1.0
	a1	-1.642099183		a1	-1.884754914
	a2	0.871253429		a2	1.0
4	b0	-1.723132138	9	b0	-1.908330129
	b1	0.855408533		b1	0.980811771
	b2	1.0		b2	0.969800235
	a1	-1.884754914		a1	-1.827835759
	a2	1.0		a2	0.969800235
5	b0	-1.830921396	10	b0	-1.792740878
	b1	0.910019237		b1	0.97044565
	b2	0.893996162		b2	1.0
	a1	-1.684963659		a1	-1.884754914
	a2	0.893996162		a2	1.0

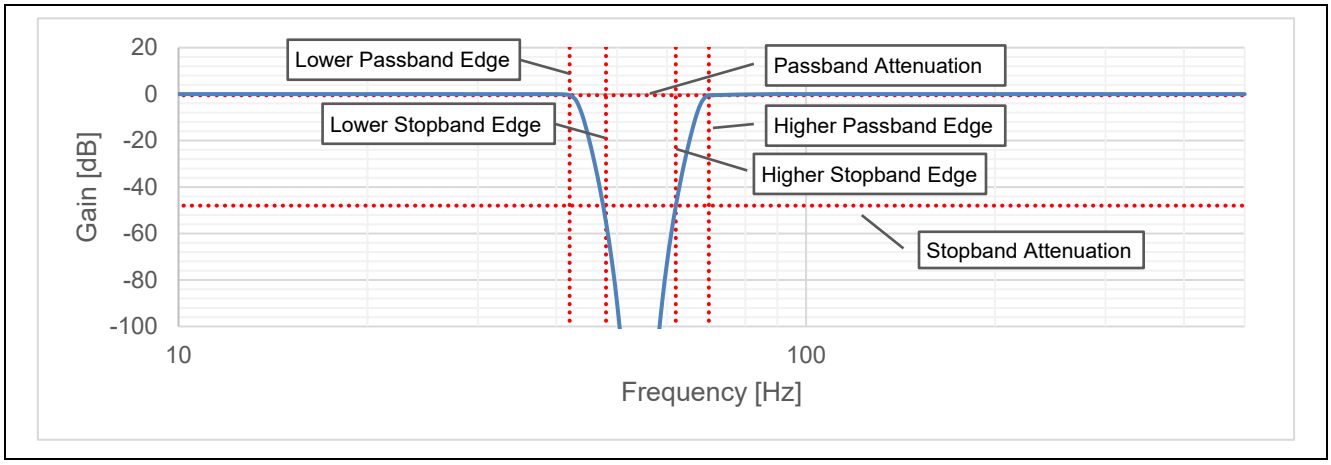


Figure 1-7 Band elimination filter frequency characteristic

Execution cycle of IIR Biquad of DSP library is shown in . Also, the example program of band elimination filter calculation is shown on the next page.

Table 1-5 The number of execution cycle

ICLK=32MHz

Arithmetic functions	Execution cycle number (Execution time)	Processing load [%]	Condition
R_DSP_IIRBiquad_f32f32	306cycle (9.5625µsec)	0.014	stages: 10, 1sample I/O

```
#include <r_dsp_filters.h>
#include <iodefine.h>
#define NUM_COEFS_PER_BIQUAD  (5)
#define NUM_DELAYS_PER_BIQUAD (2)
#define NUM_BIQUAD_STAGES     (10)

/* Coefficients should be stored in reserved order as follows,
 b10, b11, b12, a11, a12, b20, b21, b22, a21, a22, b30, ... */
float myCoeffs[NUM_COEFS_PER_BIQUAD * NUM_BIQUAD_STAGES] =         //
b0,b1,b2,a1,a2
{-1.759983012, 0.859464848,0.859754821,-1.620427124,  0.859754821,// stage-1
-1.734986523,  0.849769017,1.0,         -1.884754914,  1.0,         // stage-2
 -1.79337287,     0.880852509,0.871253429,-1.642099183,  0.871253429,// stage-
3
-1.723132138,  0.855408533,1.0,         -1.884754914,  1.0,         // stage-4
-1.830921396,  0.910019237,0.893996162,-1.684963659,  0.893996162,// stage-5
-1.728177942,  0.878290095,1.0          -1.884754914,  1.0,         // stage-6
-1.869770676,  0.943952367,0.927312973,-1.747757683,  0.927312973,// stage-7
-1.751726936,  0.917752298,1.0,         -1.884754914,  1.0,         // stage-8
-1.908330129,  0.980811771,0.969800235,-1.827835759,  0.969800235,// stage-9
-1.792740878,  0.97044565, 1.0,         -1.884754914,  1.0          // stage-10
};
float myDLine[NUM_DELAYS_PER_BIQUAD * NUM_BIQUAD_STAGES];

r_dsp_iirbiquad_t myHandle = {// instantiate a handle for IIR Biquad filter
api
  NUM_BIQUAD_STAGES,     // stages
  (void*)myCoeffs,    // Pointer to coefficients array
  (void*)myDLine,     // Pointer to delay line
  1.0,                // scalling factor
  0,                  // qint, not referred on floating points api
  0,                  // option, not referred on floating point api
  R_DSP_BIQUAD_FORM_II   // Biquad form
};

float    InData, OutData;
vector_t myInput = {1, (void*)&InData};    // input vector
vector_t myOutput = {1, (void*)&OutData}; // output vector
r_dsp_status_t myRetVal = R_DSP_STATUS_OK; // place to store return status

/* Initialize the coefficients and internal state */
myRetVal = R_DSP_IIRBiquad_Init_f32f32(&myHandle);

while(1)
{
  while (1U == IR(DSAD0, ADI0))   // waiting for A/D conversion to end
  {
    /*----- Get DSAD0 data -----*/
    IR(DSAD0, ADI0) = 0;                          // Clear IR flag
    InData = (float)(((int32_t)((DSAD0.DR.LONG) << 8)) >> 8); // sign extension

    /*--------------- DSP Library function call --------------*/
    myRetVal = R_DSP_IIRBiquad_f32f32(&myHandle, &myInput, &myOutput);

    /*--- filtered output is stored in OutData as float type ---*/
  }
}
```

1.4.2.2 Moving Average Filter

Considering the processing load, the moving average filter is effective. Supposing that the output data rate of DSAD0 is the output sampling frequency f_s and that the lowest frequency to suppress is f_{c0}, the number of samples for a moving average AS is calculated with the equation below.

$$AS = {f_s}/{f_{c0}}$$

Setting the suppression frequency in 10Hz increments to reduce the commercial power frequency of 50Hz and 60Hz, the number of averaging samples is 98 from the following equation supposing that the output data rate of DSAD0 is 976.5625SPS, and the lowest frequency to suppress is 10Hz.

$$AS = {f_s}/{f_{c0}} = {976.5625}/{10} = 97.65625 \cong 98$$

The frequency characteristic of the moving average filter on the above conditions is shown in , and a program example is shown in the next page.

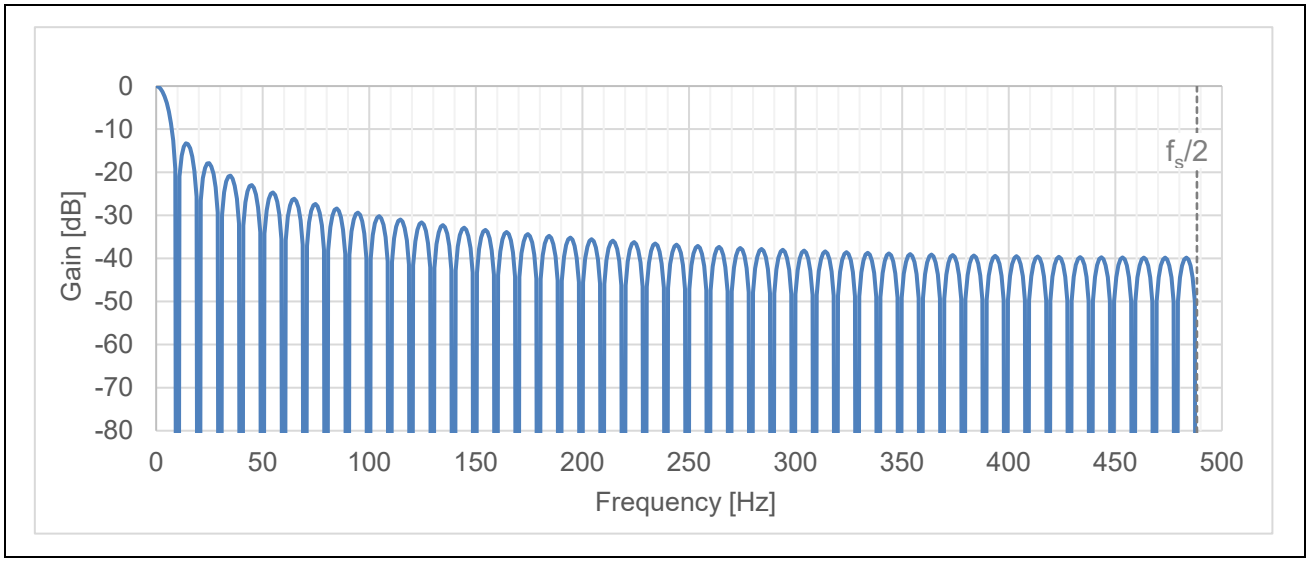


Figure 1-8 Frequency characteristic of Moving Average Filter

```
#include <iodefine.h>
#include <stdint.h>
#include <string.h>

#define D_MOVING_AVERAGE_NUM    (98)     // Number of Moving Average: 1 to 127

int32_t  myDLine[D_MOVING_AVERAGE_NUM];  // Delay line
int32_t  sum    = 0;                      // Sum value
uint32_t index = 0;                       // Sample count

/*---- Initialize Delay line ----*/
memset(myDLine, 0, sizeof(int32_t) * D_MOVING_AVERAGE_NUM);

while(1)
{
while (1U == IR(DSAD0, ADI0))   // waiting for A/D conversion to end
{
       int32_t adval;     // A/D value
       int32_t average;    // Moving averaged A/D value

       /*---- Get DSAD0 data -----*/
       IR(DSAD0, ADI0) = 0;                                  // Clear IR flag
       adval = ((int32_t)((DSAD0.DR.LONG) << 8)) >> 8;    // sign extension

       /*---- Moving average operation ----*/
       sum = (sum - myDLine[index]) + adval;
       myDLine[index] = adval;
       index++;

       if (D_MOVING_AVERAGE_NUM <= index)
       {
          index = 0;
       }

       average = sum / D_MOVING_AVERAGE_NUM;
   }
}
```

1.5 Chopping

Offset voltage of A/D converter can be corrected with offset correction function of DSAD. However, it is unsuited to correcting offset change caused by temperature drift which is the change due to change in ambient temperature as time passes.

If A/D input is carried out with differential input, the offset caused by temperature drift can be compensated by averaging the results of converting signals from analog to digital alternately with input normal connection and reverse connection. shows the image of offset drift removal.

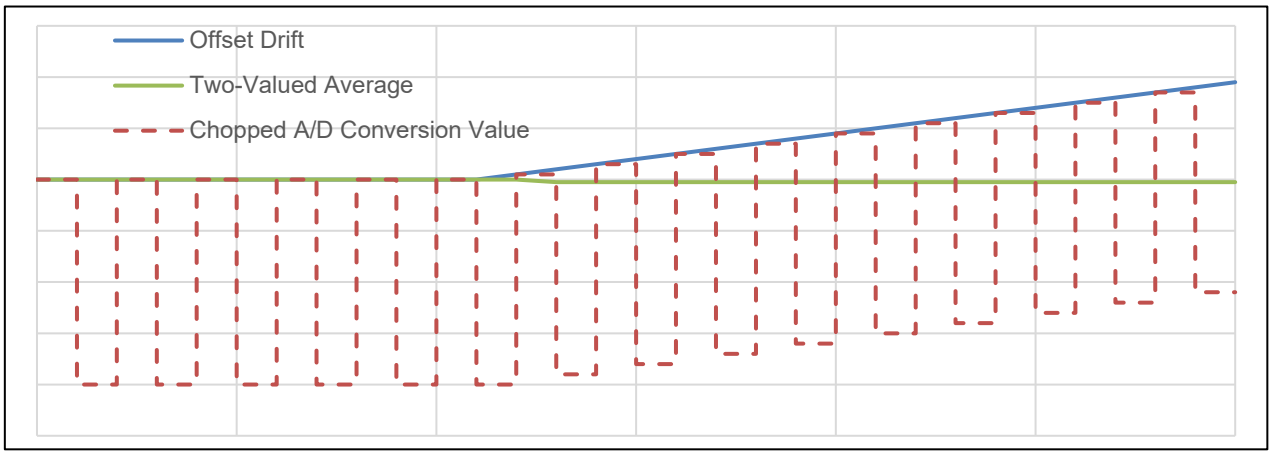


Figure 1-9 Offset drift removal by chopping

For example, take a sampling using the channel function with channel 0 normal connection input and channel1 reverse connection, and then continue by alternating by one sample. Block diagram is shown in , and A/D conversion conditions for each device are shown in and .

Setting of channel 0 and 1 is the same except for that of input pin. Channel 0 has normal connection and channel 1 has reverse connection.

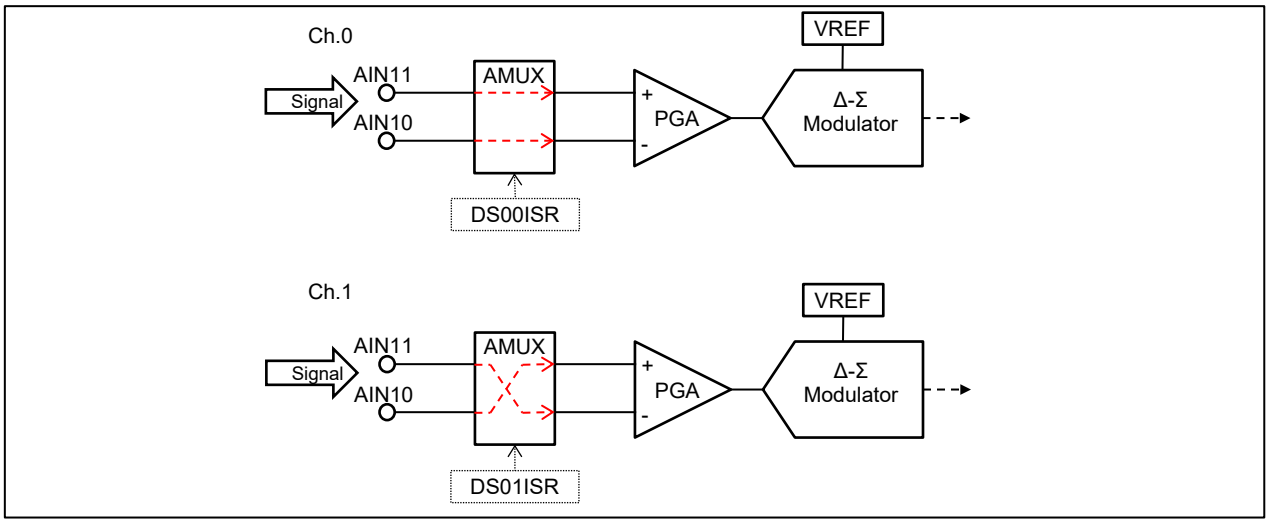


Figure 1-10 Block diagram of chopping on DSAD0

Table 1-6 Example of RX23E-A DSAD0 conversion condition for chopping

Normal Mode: f_{MOD} = 0.5MHz

Item	Setting		Remarks
Channel	0	1	
Input pin	+: AIN10 –: AIN11	+: AIN11 –: AIN10	
OSR	6208		Set oversampling ratio
A/D conversion time	49.92 [msec]	49.92 [msec]	Settling time
Data rate after chopping	10.01603 SPS		0.5 / A/D conversion total time

Table 1-7 Example of RX23E-B DSAD0 conversion condition for chopping

f_{MOD} = 4MHz

Item		Setting		Remarks
Channel		0	1	
Input pin		+: AIN10 –: AIN11	+: AIN11 –: AIN10	
Digital Filter		SINC4+SINC4	SINC4+SINC4	
OSR		49664		Oversampling ratio OSR = OSR1 x OSR2
	OSR1	256		
	OSR2	194		
A/D conversion time		49.94525ms	49.94525ms	Settling time 2
Data rate after chopping		10.010962 SPS		0.5 / A/D conversion total time

The following is the example of coding for the process of averaging A/D conversion value acquired in normal and reverse connection.

```
#include <iodefine.h>
#include <stdint.h>

uint32_t ad_data;
int32_t  ad_value = 0;

while(1)
{
  while (1U == IR(DSAD0, ADI0))   // waiting for A/D conversion to end
  {
    IR(DSAD0, ADI0) = 0;                          // Clear IR flag
    ad_data = DSAD0.DR.LONG;                 // Get DSAD0 data
    if ( 1 == (ad_data >> 29) )
    {  // channel-0: positive connection data
       ad_value = ((int32_t)(ad_data << 8)) >> 8; // sign extension
    }
    else
    {  // channel-1: negative connection data
       ad_value -= ((int32_t)(ad_data << 8)) >> 8;   // sign extension and
substitute
       ad_value >>= 1;                          // averaging
    }
  }
}
```

1.6 Temperature Sensor

RX23E has a temperature sensor built in to measure temperature within the device. Output of the temperature sensor is converted from analog to digital with DSAD0 and then change into temperature using floating point format coefficients which are incorporated in the device.

The temperature sensor output can be converted with other external sensors signal as sequentially, using the channel function which is explained in “1.2 A/D conversion of Multiple Signals with Channel Function”.

This example shows how to take a sampling of output from the temperature sensor and convert it into temperature. and show DSAD0 conversion condition. An example of coding which calculates temperature from acquired A/D conversion value is shown in the next page.

Gain of digital filter changes with the setting of oversampling ratio (OSR), therefore, A/D conversion value needs to be corrected. For the digital filter gain correction, refer to “1.3.2 ”.

The temperature is calculated with the below equation using single-precision floating-point calculation from *ADValue* which is the value determined by performing gain correction on A/D conversion value with digital filter.

$$Temperature = (AFE.TC2R) \cdot ADValue^2 + (AFE.TC1R) \cdot ADValue + (AFE.TC0R)\ [℃]$$

Table 1-8 Example of RX23E-A DSAD0 conversion condition for temperature sensor

Normal Mode: f_{MOD} = 0.5MHz

Item	Setting	Remarks
Channel	0	
Input pin	Temperature sensor	DS00ISR.TSEN = 1
PGA gain	Bypass	DSAD0.CR0.GAIN setting disabled
Reference voltage	Exclusively for temperature sensor	RSEL setting disabled
OSR	50000	Oversampling ratio setting
Data rate[SPS]	10.000	

Table 1-9 Example of RX23E-B DSAD0 conversion condition for temperature sensor

f_{MOD} = 4MHz

Item		Setting	Remarks
Channel		0	
Input pin		Temperature sensor	DS00ISR.TSEN = 1
PGA gain		Bypass	DSAD0.CR0.GAIN Setting disabled
Reference voltage		Exclusively for temperature sensor	RSEL setting disabled
OSR		399872	Oversampling ratio OSR = OSR1 x OSR2
	OSR1	256	
	OSR2	1562	
Data rate [SPS]		10.003	

```
#include <iodefine.h>
#include <stdint.h>
#include <mathf.h>

/* Temperature coefficients */
float tc0r = *(float*)&AFE.TC0R;
float tc1r = *(float*)&AFE.TC1R;
float tc2r = *(float*)&AFE.TC2R;

uint32_t osr = DSAD0.MR0.BIT.OSR;// OSR selection
float temp;                      // temperature

while(1)
{
  while (1U == IR(DSAD0, ADI0))   // waiting for A/D conversion to end
  {
    /*----- Get DSAD0 data -----*/
    IR(DSAD0, ADI0) = 0;                          // Clear IR flag
    temp = (float)(((int32_t)((DSAD0.DR.LONG) << 8)) >> 8);   // sign extension

    /*----- Conversion to temperature -----*/
    temp = temp * temp * tc2r + temp * tc1r + tc0r;
  }
}
```

1.7 Disconnection Detection

RX23E is equipped with disconnection detection assist function in order to detect disconnection of measurement circuit. The disconnection detection assist function consists of the constant current source and the switch to supply current with measurement circuit.

This section describes the example of detecting disconnection of thermocouple measurement circuit which is illustrated in . shows the change in A/D conversion value when disconnection detection is carried out under the DSAD0 conversion conditions in .

As shown in , if disconnection detection assist current is enabled after disconnection occurred, the capacitor of the external circuit will be charged. As a result, the A/D conversion value will change to the maximum value. Therefore, if A/D conversion value shifts to the maximum by enabling disconnection detection assist current, it is judged that disconnection is occurring. The time in which the A/D conversion value stays at the maximum is determined by the time constant by the external circuit for disconnection detection assist current and PGA gain.

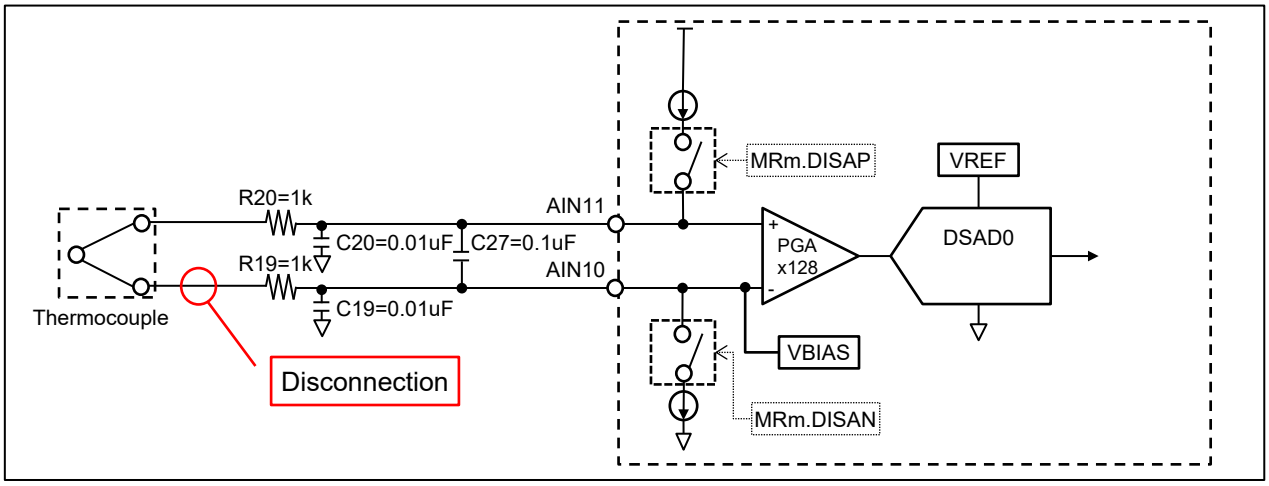


Figure 1-11 Example of thermocouple measurement circuit

Table 1-10 Example of DSAD0 conversion condition

Item	Setting		Remarks
	sensor measurement	disconnection detection	
Input pin	+: AIN10 –: AIN11		
PGA gain	x128		
Reference voltage	REFOUT – AVSS0		
Disconnection detection assist current	4μA		MR0.DISC = 2
Positive Input Signal Disconnect Detection Assist	OFF(0)	ON(1)	RX23E-A:MR0.DISAP, MR0.DISAN RX23E-B: MR0.DISA
Negative Input Signal Disconnect Detection Assist	OFF(0)	ON(1)	

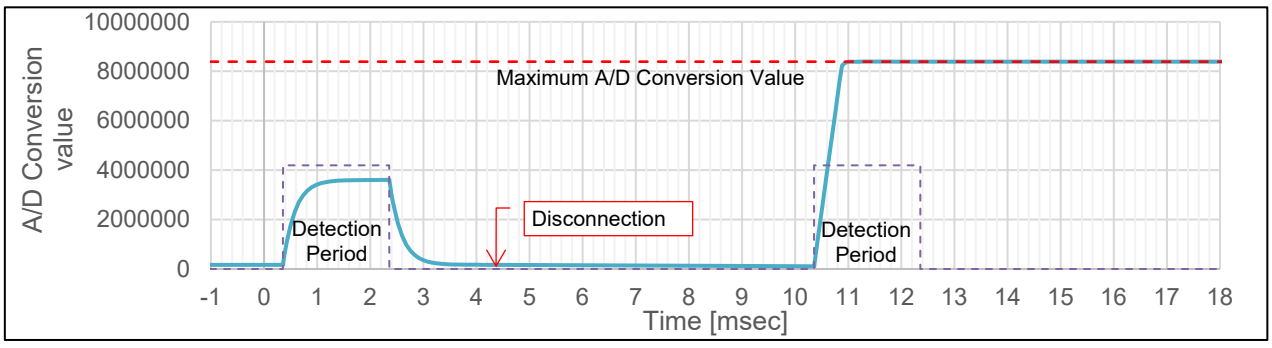


Figure 1-12 Example of A/D conversion value change when disconnection is detected

2. Hardware Design Considerations

2.1 Input into DSAD・AFE

RX23E is equipped with Analog input pins shown in , which can be used for differential input/pseudo-differential input or single-ended input. When using DSAD, choose AINP (input selection pin on + side) or AINM (input selection pin on – side).

Table 2-1 Analog input pin

Item	RX23E-A	RX23E-B	
	5V input	5V input	±10V input
Input pin count at max	12	16	4
Differential input count at max	6	8	2
Single-ended input count at max	11	16	4

2.1.1 Input Voltage Range

Input voltage which is put into DSAD must be within the absolute input voltage range and differential input voltage range. If the input voltage is outside the input voltage range, it can not be measured correctly.

For the 5V input pin, set AINP input voltage V_{AINP} and AINM input voltage V_{AINM} under the absolute input voltage range AVCC+V_{HRP} and above AVSS+V_{HRN}. V_{HRP} and V_{HRN} refer to headroom voltage. When analog input buffer BUF is not used, they are described with the equations, V_{HRP}= +50mV, V_{HRN}= -50mV. On the other hand, when BUF is used, they are given by V_{HRP}= -100mV, V_{HRN}= +100mV. Please note that the absolute input voltage range becomes narrow when BUF is used.

Set differential input voltage, V_{IN}=V_{AINP}-V_{AINM}, within the differential input voltage range ±VREF/GAIN. However, when PGA is used and GAIN is 1x, the differential input voltage range will be ±VREF or ± (AVCC0-AVSS0-0.5V), whichever is narrower. If voltage above the differential input voltage range is entered, AD value will be saturated.

e.g. : When ±VREF=±(AVCC0 – AVSS0) =±5V, differential input voltage range will be ±4.5V.

According to the above, shows the input voltage range in the case of AVCC0=5V, AVSS0=0V, VREF=2.5V, PGA enabled (1, 2, 4, 128x). The input voltage range which can be measured without AD value saturated is limited inside of the hexagon illustrated in .

For the ±10V input pin, set the AINP input voltage V_{AINP} and AINM input voltage V_{AINM} within AVSS0± 10V. The differential voltage input range will be limited to the narrower of ±VREF/GAIN and ±20V.

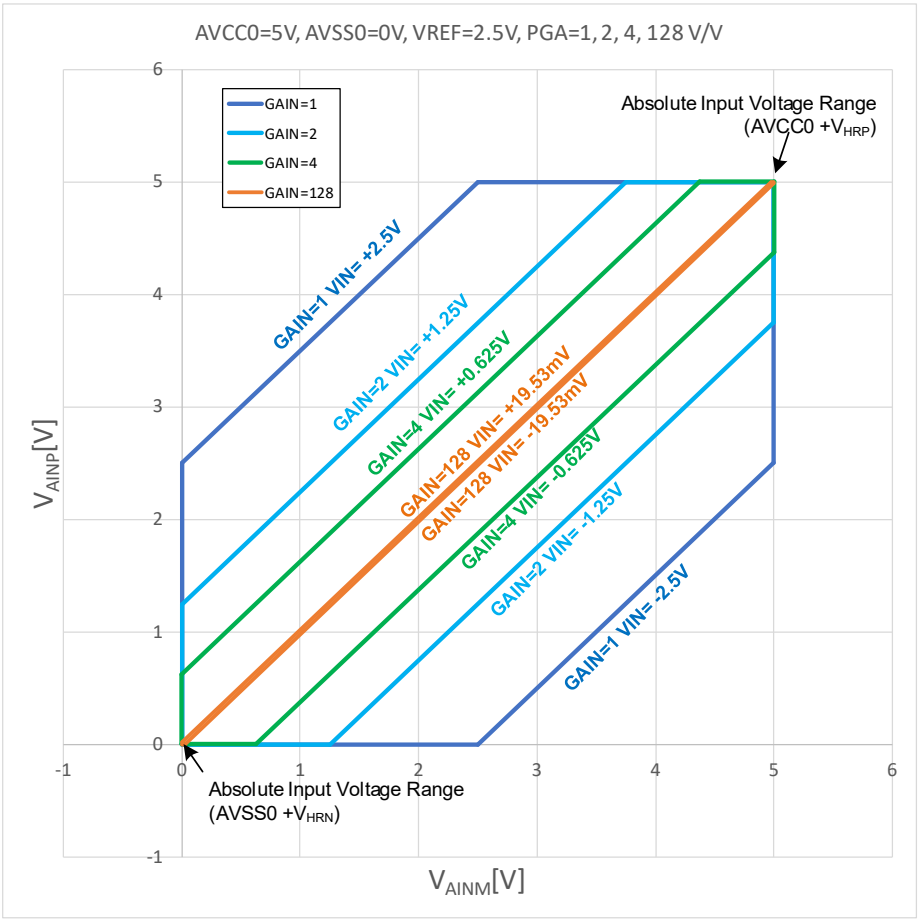


Figure 2-1 Input voltage range to DSAD (for 5V input pin)

2.1.2 Selection of Input Method

(1) Single-ended mode

shows the example of voltage measurement in single-ended mode.

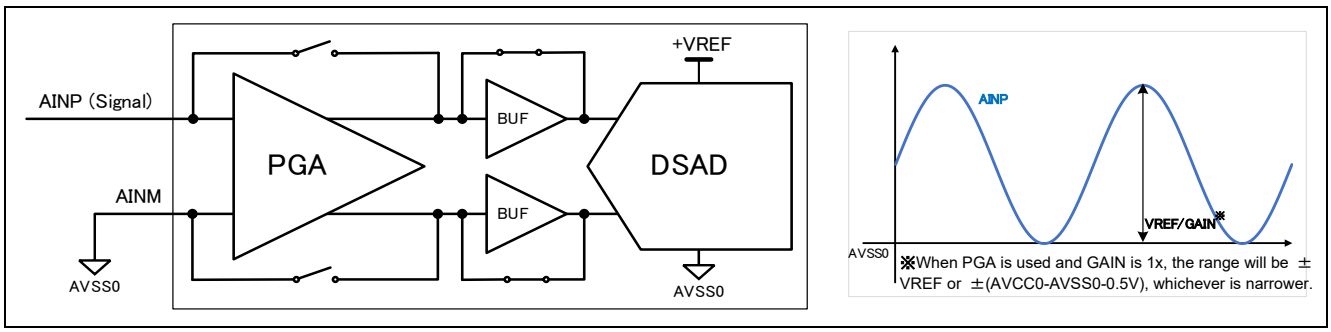


Figure 2-2 Example of voltage measurement in single-ended mode

When using DSAD in single-ended mode, select one out of 12 input pins as AINM. If the selected pin is connected to AVSS0, the voltage between AINP and AVSS0 can be measured by choosing as AINP from remaining 11 pins. Although the single-ended mode has some influence such as deterioration of Common Mode Rejection Ratio (CMRR) characteristic, it enables to process the most input signals.

(2) Pseudo-differential input mode

illustrates the example of voltage measurement in pseudo-differential input mode.

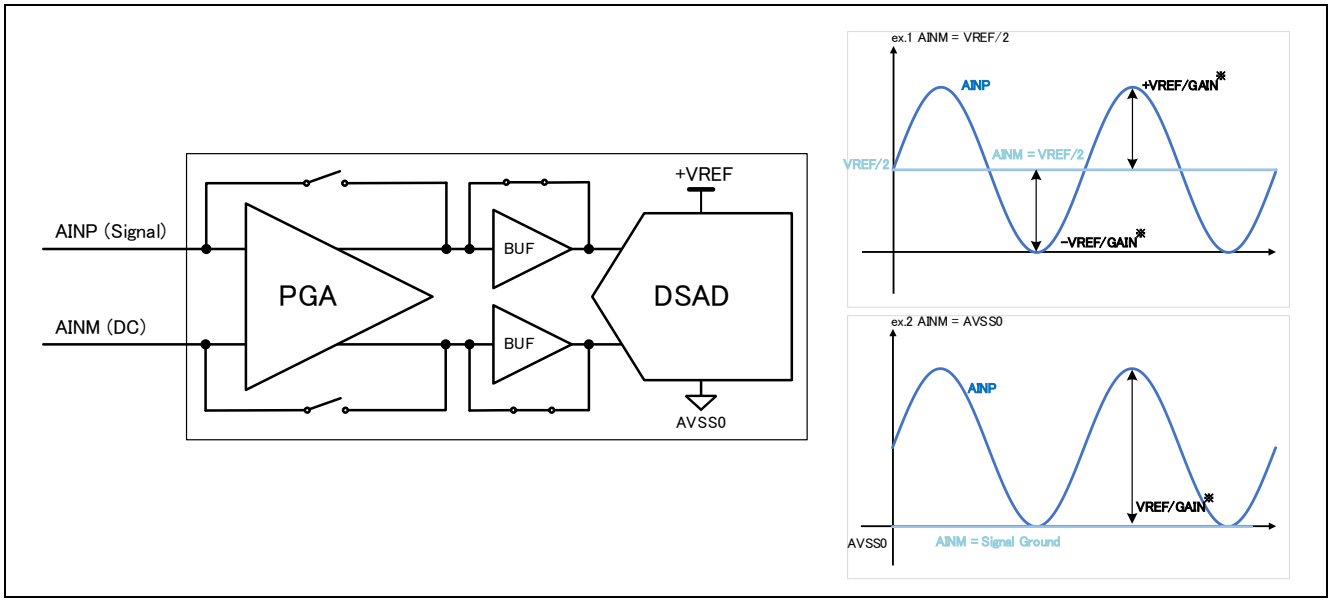


Figure 2-3 Example of voltage measurement in pseudo-differential input mode

In pseudo-differential input mode, while keeping DC voltage on one pin, enter signal to another pin. In DSAD, A/D conversion is performed for the difference between the signal and the DC voltage, it is called pseudo-differential. If AINM is connected with AVSS0, this mode operates in the same way as the single-ended mode. The difference from the single-ended mode is that AINM is apart from the ground loop, which enables to remove common-mode noise. However, since, in general, impedance to common-mode noise source seen from AINP and AINM is different in pseudo-differential input mode due to various factors such as influence of signal source impedance, CMRR characteristic is less good compared to when operated in (true) differential input mode.

(3) Differential input mode

illustrates the example of voltage measurement in (true) differential input mode.

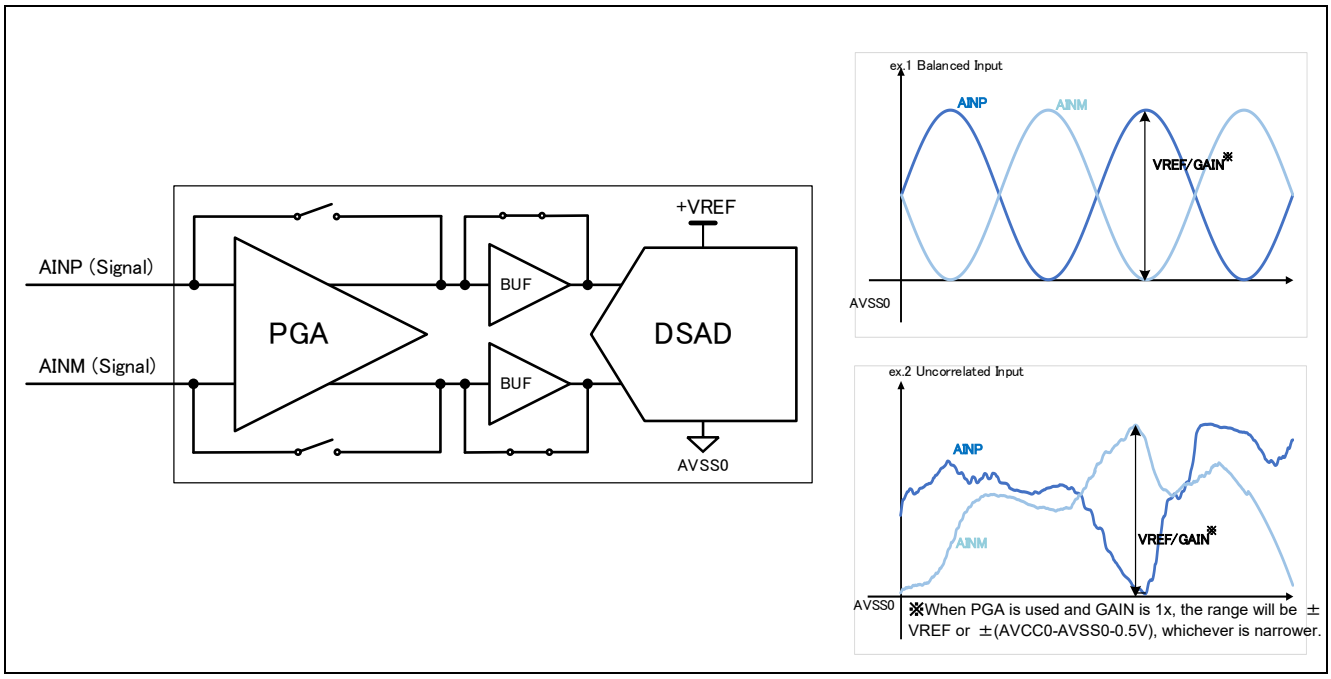


Figure 2-4 Example of voltage measurement in differential input mode

In differential input mode, balanced signal and differential voltage of independent voltage can be measured. This mode demonstrates the highest CMRR characteristic. In differential input and pseudo-differential input mode two pins next to each other are used.

In differential input mode and pseudo-differential input mode, it is recommended that two pins next to AINP and AINM be used in a pair. Using two pins next to each other can strengthen the connection between the two pins. In addition, by matching the impedance of wiring, deterioration of CMRR characteristic can be reduced. Moreover, laying shield wiring between the signal and other signal can reduce crosstalk with other signals.

2.2 Anti-aliasing Filter

illustrates the example of configuring filter circuit for DSAD input

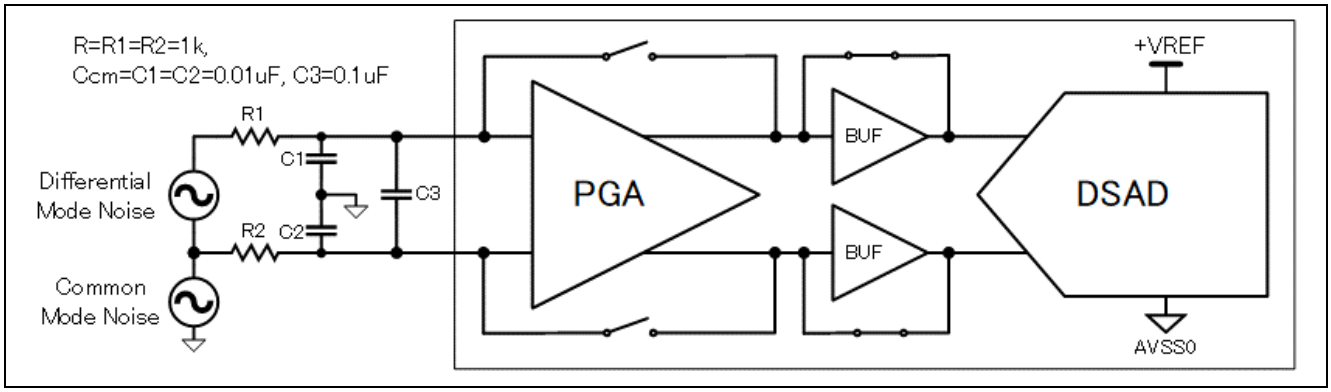


Figure 2-5 Example of configuring filter circuit for DSAD input

If there is a possibility that noise with frequency components around the passband might enter, anti-aliasing filter needs to be added. If oversampling ratio is large, there is a big difference between the output data rate and modulator (sampling) frequency. Therefore, cutoff frequency of anti-aliasing filter can be set lower enough than Nyquist frequency, f_{MOD} / 2. Thus, simple configuration with primary filter such as RC filter is possible.

In , cutoff frequency of low-pass filter for common mode noise, f_{cm} and that of low-pass filter for differential mode noise, f_{diff} can be described with the below equations.

$$f_{cm} = \frac{1}{2\pi R C_{cm}} = 15.9\ [\mathrm{kHz}]$$

$$f_{diff} = \frac{1}{2\pi R (C_{cm} + 2C_3)} = 757.9\ [\mathrm{Hz}]$$

illustrates gain frequency characteristic of low-pass filter when f_{diff} =757.9Hz and that of decimation filter when RX23E-A output data rate is 956.5625SPS (oversampling ratio 512). The figure shows that even if the cutoff frequency of differential low-pass filter (757.9 Hz) is configured around the data rate (956.5625 SPS), adequate amount of attenuation can be secured for the passband around f_{MOD}.

As for the filter for the common mode noise, consider CMRR deterioration caused by variation in parts, temperature characteristics, DC bias characteristics, AC voltage characteristics, and so on. Consider using parts with small tolerance when CMRR characteristic is important. Otherwise CMRR characteristic in high frequency band deteriorates due to the variation in capacitor characteristics.

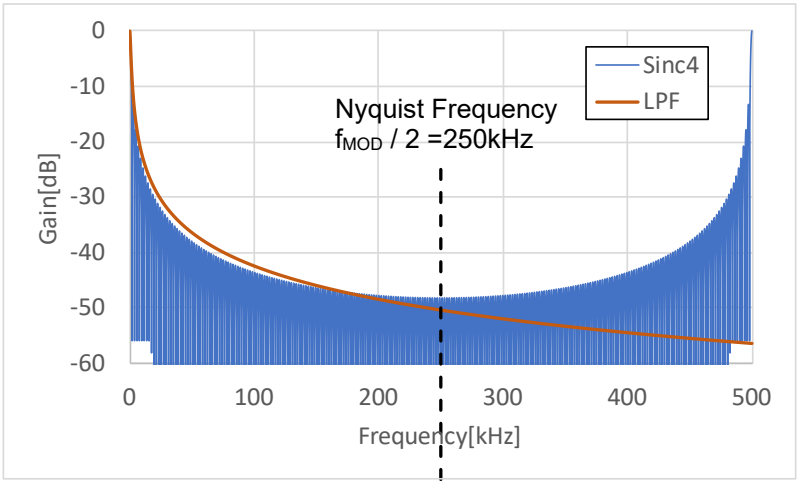


Figure 2-6 Gain frequency characteristic of low-pass filter and decimation filter (RX23E-A: SINC4)

2.3 Circuit Design and Board Layout

In order to bring out the DSAD performance fully, it is necessary to properly set power supply, ground layout and signal wiring. This section describes matters to be considered regarding circuit design and board design.

2.3.1 Signal wiring

(1) Crosstalk

In order to prevent crosstalk, do not arrange tiny analog signal line near the signal which significantly varies and consumes large current such as digital signal and output of switching power supply. Also, secure space between the wiring of tiny signal and the wiring which becomes noise source. Also shorten the range where wires are close each other. It is also effective to arrange shields with ground potential pattern.

It is necessary to keep the endpoint of shield pattern closed and connect with ground plane with appropriate intervals using ground via. When the endpoint is kept open, it can not perform as a shield for high frequency signal.

Wire by bringing signals which makes a pair close, when using DSAD in differential input mode or pseudo-differential Input mode. Coupling between differential signals is strengthened, which can heighten the tolerance toward the common mode noise.

shows the example of shield wiring and differential signal wiring.

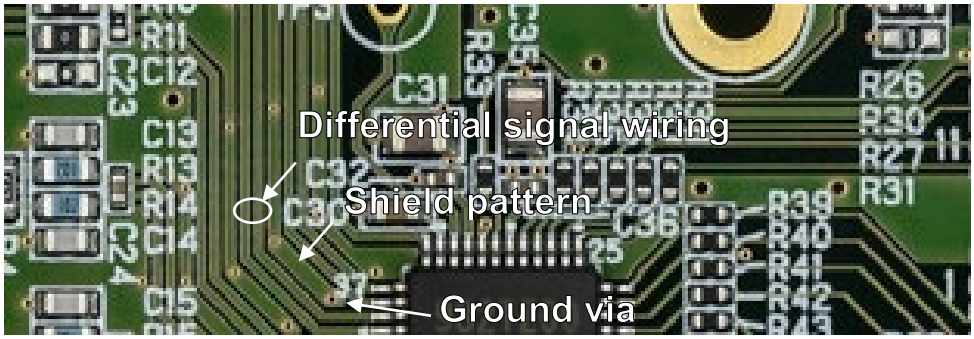


Figure 2-7 Example of shield wiring and differential signal wiring

(2) Temperature gradient

Be careful about the temperature gradient on the board, when measuring tiny signal of μV order is required such as thermocouple measurement with high precision. Since board pattern and soldered part of component are where different types of metals are connected like those of thermocouple, they generate thermoelectromotive force corresponding to the temperature difference. Therefore, be sure that the signal line which is the subject of high precision measurement does not have the temperature gradient. For the countermeasure, in general, the following methods are available.

- Reduce heat generation

If low energy consumption parts are chosen, generated heat itself can be reduced. It is also effective to reduce power supply voltage depending on the situation.

- Appropriately arrange heat dissipation parts

By mounting heat dissipation parts such as heat sink on heat source, heat can be dissipated into the surrounding air. By doing so, heat is dissipated, and local temperature gradient can be prevented. Power supply IC enables to have board plane function as a heat sink by arranging thermal via on it.

- Thermal insulation

It is also effective to insulate weak signal wiring from heat sources. The area on the board where there is no solid part has high insulation effect. By separating the plane to create the area where there is no solid part, it's possible to reduce the heat generated from heat sources which exposes the weak signal wiring. Not only such kind of insulation method, it's also effective to arrange the heat sources away from the weak signal wiring. Since heat sources are not only on the board but also outside the board, it's important to keep it away from those heat sources.

2.3.2 Power Supply Noise

Consider the effect caused by noise. Although DSAD on RX23E has the Power Supply Rejection Ratio: PSRR characteristic of about 80dB, in high precision application, power supply variation needs to be minimum. In order to reduce the power supply noise, there are methods such as appropriate selection of the power source, power supply decoupling and power supply layout

(1) Select power source

When selecting LDO, switching regulator or other DC power sources, be careful about the performance characteristic of each product, especially output voltage ripple. Avoid using the switching regulator in high precision application. The reason for this is although switching power sources are small, inexpensive and highly efficient, they generate large noise. However, when using the switching power source, thoroughly evaluate the effect caused by the noise from it before using it.

When using power source device, be sure to follow the design guideline by each device manufacture. When using the switching power source as a power source, be careful about the switching frequency. Avoid using the device which uses switching frequency around modulator clock frequency of DSAD, f_{MOD}.

(2) Power source decupling

and illustrates the layout images of power source decoupling of LDO and RX23E, respectively.

Place a capacitor with adequate capacity near the output of each power source. Appropriate decoupling capacitor helps reduce the ripple noise outputted by power source and the effect by load fluctuation. Place capacitors near input pins of VCC, VSS, VCL, AVCC0, and AVSS0 on RX23E. When using REFOUT, place the capacitor near the REFOUT pin.

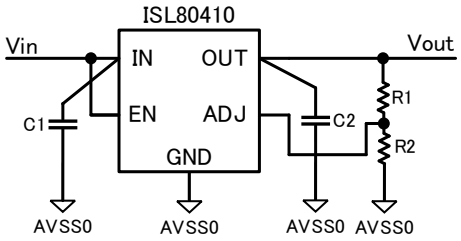
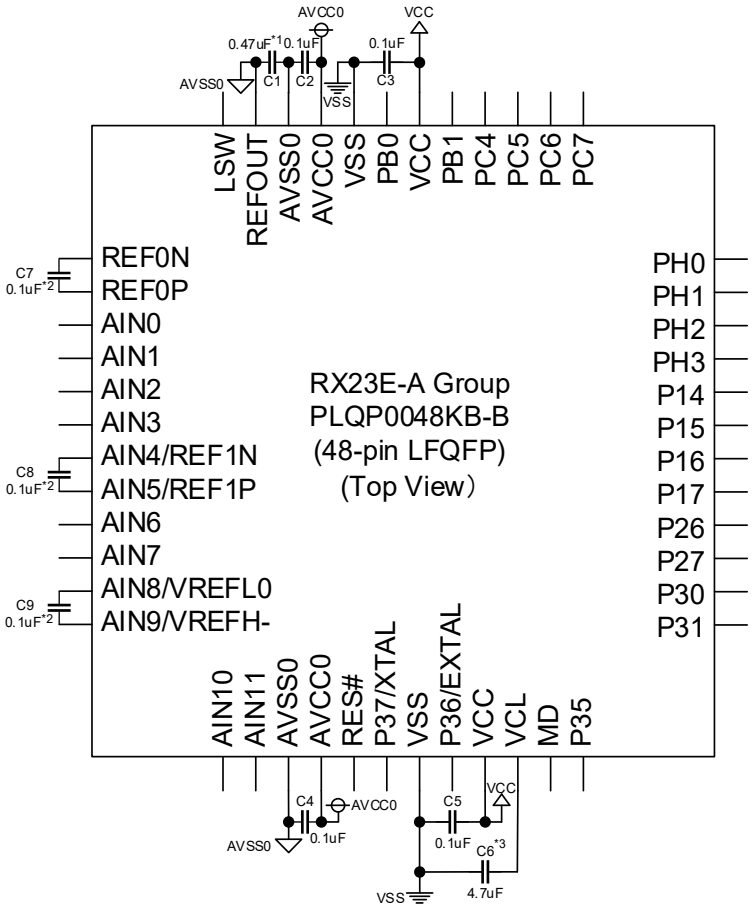


Figure 2-8 Example of power source decoupling of LDO



Note. Place the capacitors close to the pin

Note 1. Connect the REFOUT pin to AVSS0 via a 0.47-uF capacitor when using the internal reference voltage (VREF)

Note 2. Connect the capacitor between each pair of the external reference input pins, when using the external reference. The values are for reference. Determine the values based on the characteristics of the power-supply circuit.

Note 3. Do not apply the power supply voltage to the VCL pin. Use a 4.7-uF multilayer ceramic capacitor for the VCL pin

Figure 2-9 Example of power source decoupling (RX23E-A)

2.3.3 Component Layout

illustrates the example of the board layout using RX23E.

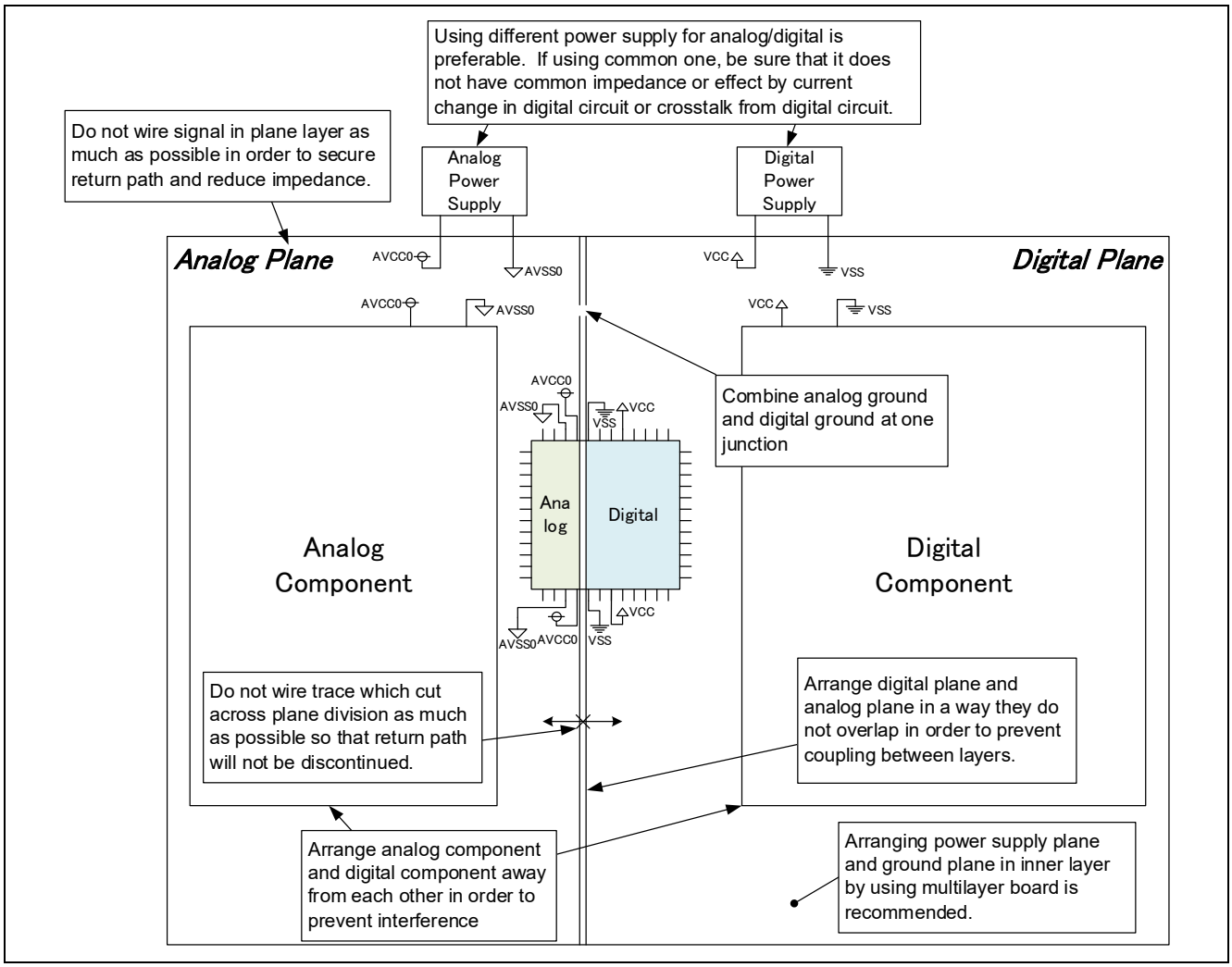


Figure 2-10 Example of board layout

Be sure that the analog power supply is not affected by the digital power supply and digital signals. Electric potential can be kept stable by selecting multilayer board and setting up power source and GND plane. As an example of 4-layer board, if configuring signal layer, GND layer, power source layer and signal layer, from the top, the capacity between layers works as a capacitor, thus noise can be reduced. Do not wire other traces on plane layer as much as possible. Plane will be separated by trace and via and then increase in impedance could reduce voltage, and if discontinuity of return path occurs, noise could enter in a roundabout way. Arrange digital signal and digital plane so that they will not overlap those of analog. Even if they are arranged in a different layer, crosstalk could occur between layers.

In , analog and digital power supplies are supplied from outside the board, and analog and digital grounds are combined at one junction. In this case, the junction is the reference potential, and signals between analog-digital and DC component of return current of power supply passes through the junction. In general, the junction is near the power source or RX23E. If they are combined near the power supply, the loop of power routing between analog and digital will become minimum.

If they are combined near RX23E, the potential difference between AVSS0 and VSS pins on RX23E can be minimum, thus coupling of digital noise transmitted to the analog block can be minimum via stray capacitance within RX23E.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.26.19	-	First release
2.00	Feb.16.24	-	Addition of descriptions for RX23E-B

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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