RX21A Group

Example Settings for Simultaneous Conversion on Seven Channels of 24-Bit ΔΣ A/D Converter

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Abstract

The RX21A has an on-chip 24-bit A/D converter that employs ΔΣ modulation and supports analog input on up to seven channels. It is also possible to assign individual converter units to single input channels and control the channels at independent timings. In the sample program presented here, the multi-function timer pulse unit 2 (MTU2a) is used to generate the A/D conversion trigger, and conversion operation takes place simultaneously on all seven channels of the ΔΣ A/D converter.

Products

RX21A (R5F521A8BDFP)

RX21A Group microcontrollers are available in versions with 64-pin, 80-pin, and 100-pin packages. The software described in this application note for performing simultaneous conversion on seven channels supports the 100-pin package version of the RX21A. When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

In the sample program, MTU2a channel 0 is used and voltages applied to the ANDSn (n = 0 to 6) pins are A/D converted successively at regular intervals on all seven channels of the ΔΣ A/D converter simultaneously.

The following functions are used by the sample program:

- Clock generation circuit
- Low power consumption function
- Register write protection function
- Interrupt controller (ICUb)
- Multi-function timer pulse unit 2 (MTU2a)
- Event link controller (ELC)
- 24-bit ΔΣ A/D converter (DSAD)

The specifications of the sample software are as follows:

- MTU2a channel 0 operates in PWM1 mode.
- The ELC function is employed to perform A/D conversion by using the MTU2a channel 0 compare match signal as the A/D conversion trigger.
- The output interval of the compare match signal is set at 81.92 μs, the minimum A/D conversion period of the DSAD.
- A/D conversion is performed on differential voltages applied on pins ANDS0 to ANDS3 and on single-ended voltages applied on pins ANDS4 to ANDS6.
- The built-in programmable gain amplifier (PGA) of the DSAD is set to ×1. The input voltage range of both the differential voltages and single-ended voltages is −500 mV to +500 mV.
- When A/D conversion completes, the A/D conversion result is stored in RAM by an interrupt handler.

Figure 1 illustrates the signal flow during ΔΣ A/D conversion triggered by the MTU2a.

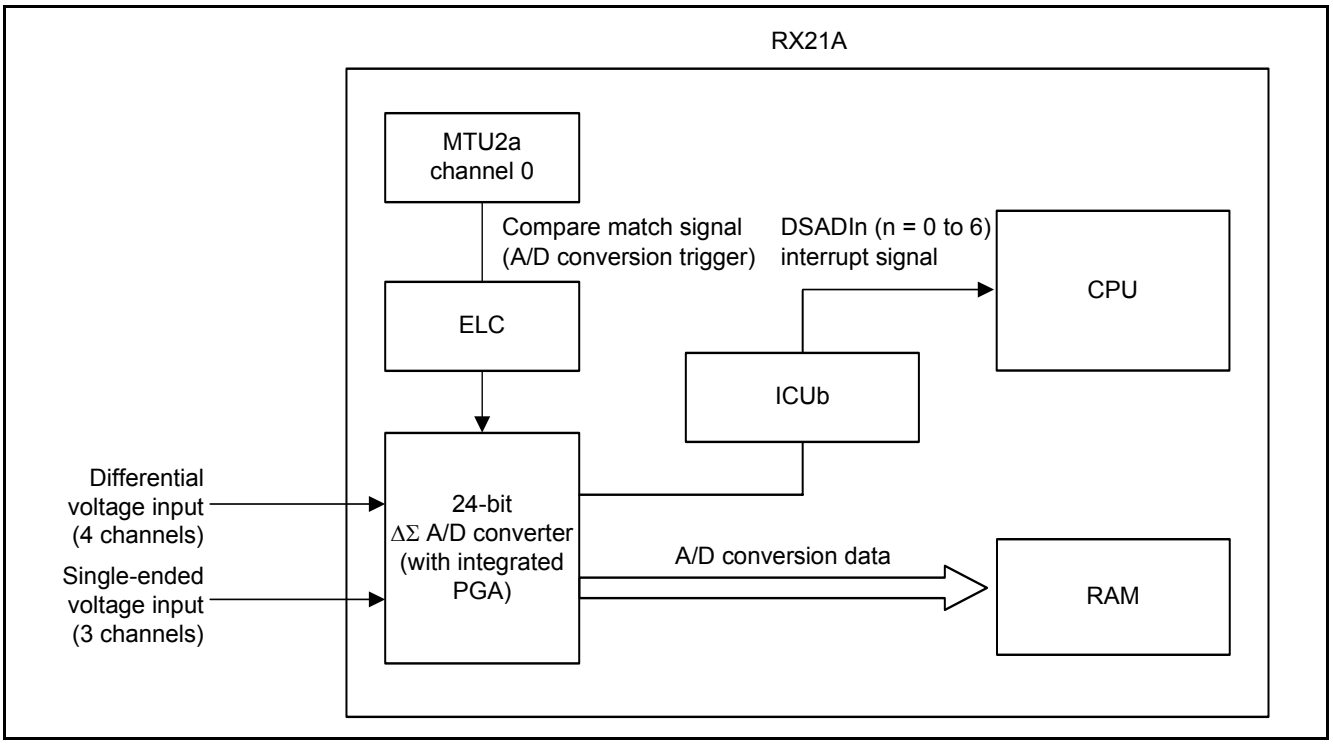


Figure 1 Signal Flow During ΔΣ A/D Conversion Triggered by MTU2a

2. Operating Conditions

Table 1 lists the operating conditions of the sample program. Figure 2 shows the hardware configuration.

Table 1 Operating Conditions

Item	Description	
Operating frequency	Input clock:	20 MHz (crystal oscillator)
	PLL clock:	100 MHz (The input clock is divided by 2, then multiplied by 10.)
	System clock (ICLK):	50 MHz (PLL clock divided by 2)
	FlashIF clock (FCLK):	25 MHz (PLL clock divided by 4)
	External bus clock (BCLK):	25 MHz (PLL clock divided by 4)
	Peripheral module clock A (PCLKA):	50 MHz (PLL clock divided by 2)
	Peripheral module clock B (PCLKB):	25 MHz (PLL clock divided by 4)
	Peripheral module clock C (PCLKC):	25 MHz (PLL clock divided by 4)
	Peripheral module clock D (PCLKD):	25 MHz (PLL clock divided by 4)
Operating voltage	Digital power supply voltage (VCC):	3.3 V
	Analog power supply voltage (AVCC0):	3.3 V
	Analog power supply voltage (AVCCA):	3.3 V
Operating mode	Single-chip mode	
Endian mode	Little-endian	

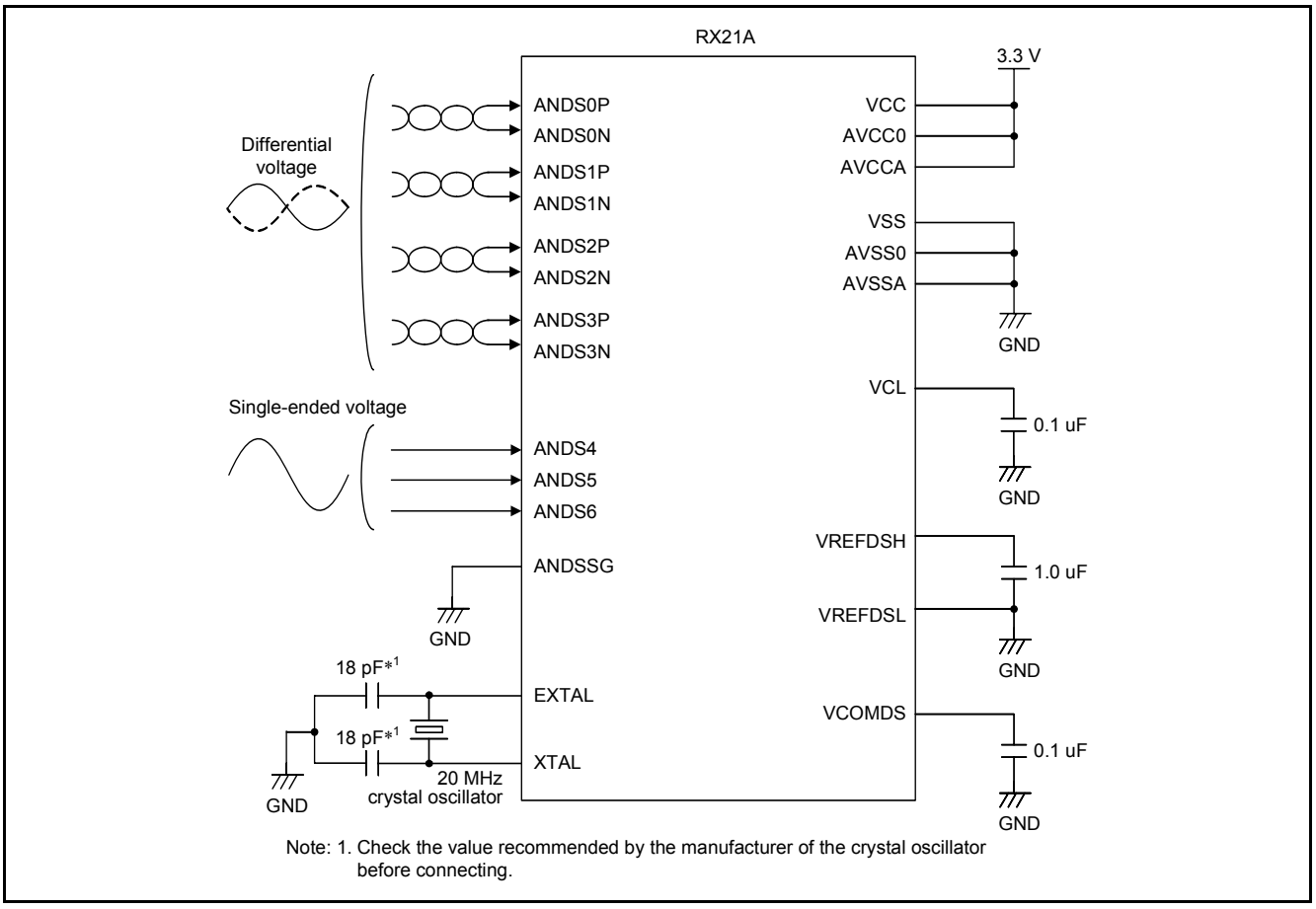


Figure 2 Hardware Configuration

3. Development Environment

Table 2 lists the components of the development environment for the sample code.

Table 2 Development Environment

Item	Description
Development tool	Renesas Electronics CubeSuite+, Ver. 1.03.00
Device information file	Renesas Electronics RX Device Dependent Information for CubeSuite+, Ver. 1.00.04
C/C++ compiler	Renesas Electronics RX Compiler CC-RX for CubeSuite+, Ver. 1.02.01
Emulator	Renesas Electronics E1 emulator
Evaluation board	Hokuto Electronic Co., Ltd., HSBRX21AP-B (mounted with R5F521A8BDFP)

4. Operation

Figure 3 is an operation timing chart of the sample program. Table 3 lists the processing performed in software and in hardware.

MTU2a channel 0 outputs compare match signal 0B at intervals of 81.92 µs. This signal is applied simultaneously to the seven DSAD channels as the A/D conversion trigger, causing A/D conversion to take place. The A/D conversion results are saved to the DSADDRn (n = 0 to 6) registers, and then they are stored in the RAM as part of the A/D conversion end interrupt handler routine.

For a detailed description of the operation of the DSAD, see RX21A Group User's Manual: Hardware.

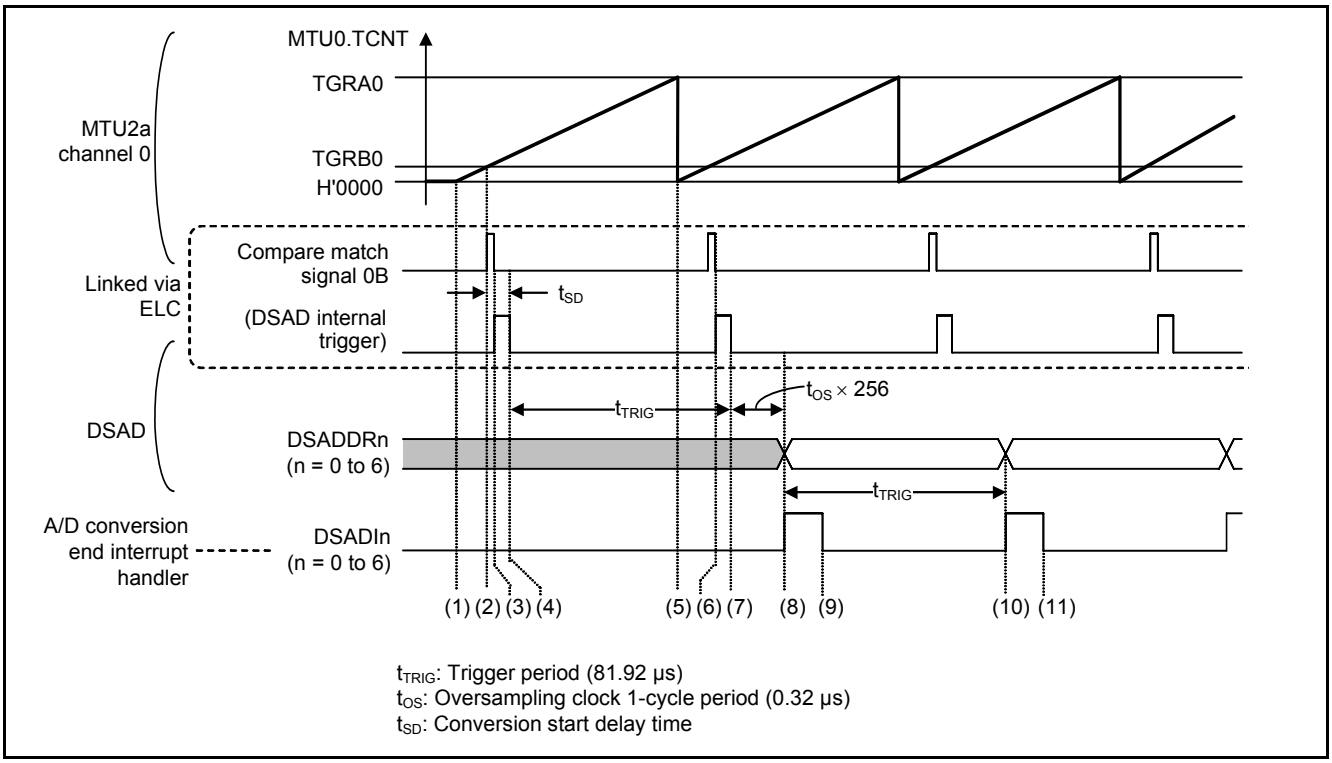


Figure 3 Operation Timing Chart

Table 3 Software and Hardware Processing

Number	Software Processing	Hardware Processing
(1)	Set CST0 bit in MTU0.TSTR to 1.	Start MTU0 counter.
(2)	—	TGRB0 compare match.
(3)	—	Apply 1st A/D conversion trigger to DSAD via ELC.
(4)	—	Start 1st A/D conversion start.*1
(5)	—	Clear TNCT at TGRA0 compare match.
(6)	—	Apply 2nd A/D conversion trigger.
(7)	—	Start 2nd A/D conversion start.
(8)	—	Store 1st A/D conversion results in DSADDRn. Set DSADIn flags.*2 (n = 0 to 6)
(9)	DSADIn interrupt handler • Store contents of DSADDRn registers in RAM. (Store 1st A/D conversion results in RAM.) • Clear DSADIn flags.	—
(10)	—	Store 2nd A/D conversion results in DSADDRn. Set DSADIn flags.
(11)	DSADIn interrupt handler • Store contents of DSADDRn registers in RAM. (Store 2nd A/D conversion results in RAM.) • Clear DSADIn flags.	—

Notes: 1. t_{SD} is determined by the synchronization timing of the trigger signal from the ELC, which operates on the peripheral module clock (PCLKB), and the oversampling clock. It is not a fixed value.

2. The A/D conversion time is the total of the synchronization timing t_{SD} and the filter operation period: $t_{SD} + t_{TRIG} + t_{OS} \times 256$.

5. Software

5.1 File Structure

Table 4 lists the file structure of the sample program.

Table 4 File Structure

File Name	Description
dbsct.c	Data section definition program (generated automatically by development tool)
intprg.c	Interrupt handler program (generated automatically by development tool)
resetprg.c	Reset program (generated automatically by development tool)
sbrk.c	Heap memory area reservation program (generated automatically by development tool)
sbrk.h	Heap size definition file (generated automatically by development tool)
stacksct.h	Stack area definition file (generated automatically by development tool)
typedefine.h	Integer type definition file (generated automatically by development tool)
vect.h	Vector definition file
vecttbl.c	Vector table initialization program
main.c	Main function program
main.h	Main function header file
iodefine.h	RX21A on-chip peripheral function register definition file

5.2 List of Functions

Table 5 lists the functions provided as part of the sample code. Figure 4 shows the layered structure of the functions.

Table 5 List of Functions

Function Name	Outline
main	Calls initialization functions for system, DSAD, MTU2a, and ELC, and starts MTU2a channel 0 timer.
system_init	Initializes system clock and cancels module stop.
dsad_init	Initializes DSAD.
mtu0_init	Initializes MTU2a channel 0.
elc_init	Initializes ELC.
dsadi*n*_isr (*n* = 0 to 6)	DSAD conversion end interrupt handler Stores A/D conversion result in RAM and clears interrupt source. DSAD input channels 0 to 6 are processed equivalently.

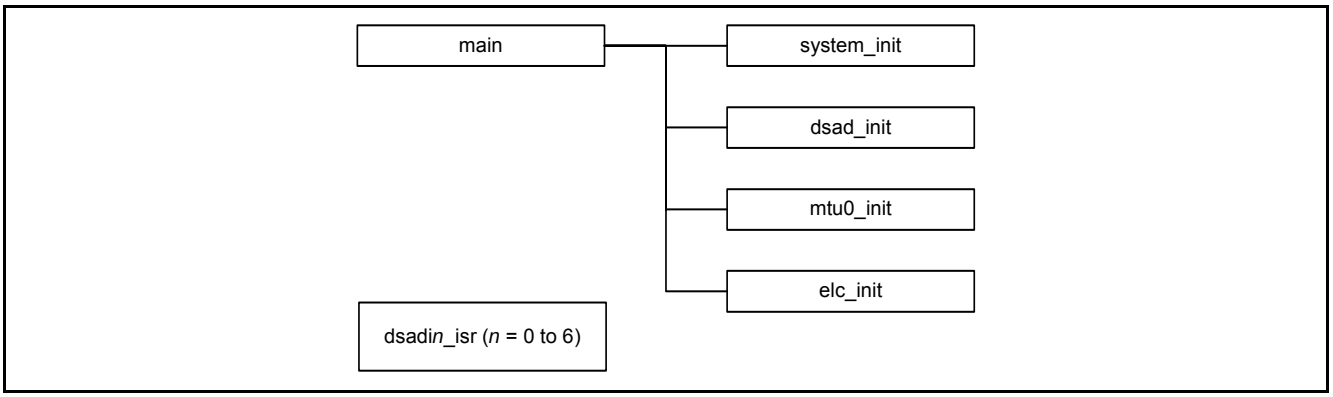


Figure 4 Layered Structure

5.3 RAM Used

Table 6 lists the RAM area used by the sample program.

Table 6 List of RAM Used

Type	Variable Name	Description	Used by Function
int32_t	g_dsad_data[7]	On-chip RAM area (4 bytes) for storing A/D conversion result (DSADDR0 to DSADDR6)	dsadi*n*_isr (*n* = 0 to 6)

Note: In addition to the above, RAM areas must be reserved for the user stack and interrupt stack.

5.4 Functions

5.4.1 main Function

(1) Outline of Function

This function calls initialization functions for the modules used (clock, DSAD, MTU2a, and ELC), and starts the MTU2a channel 0 timer.

(2) Arguments

None

(3) Return Values

None

(4) Internal Registers Used

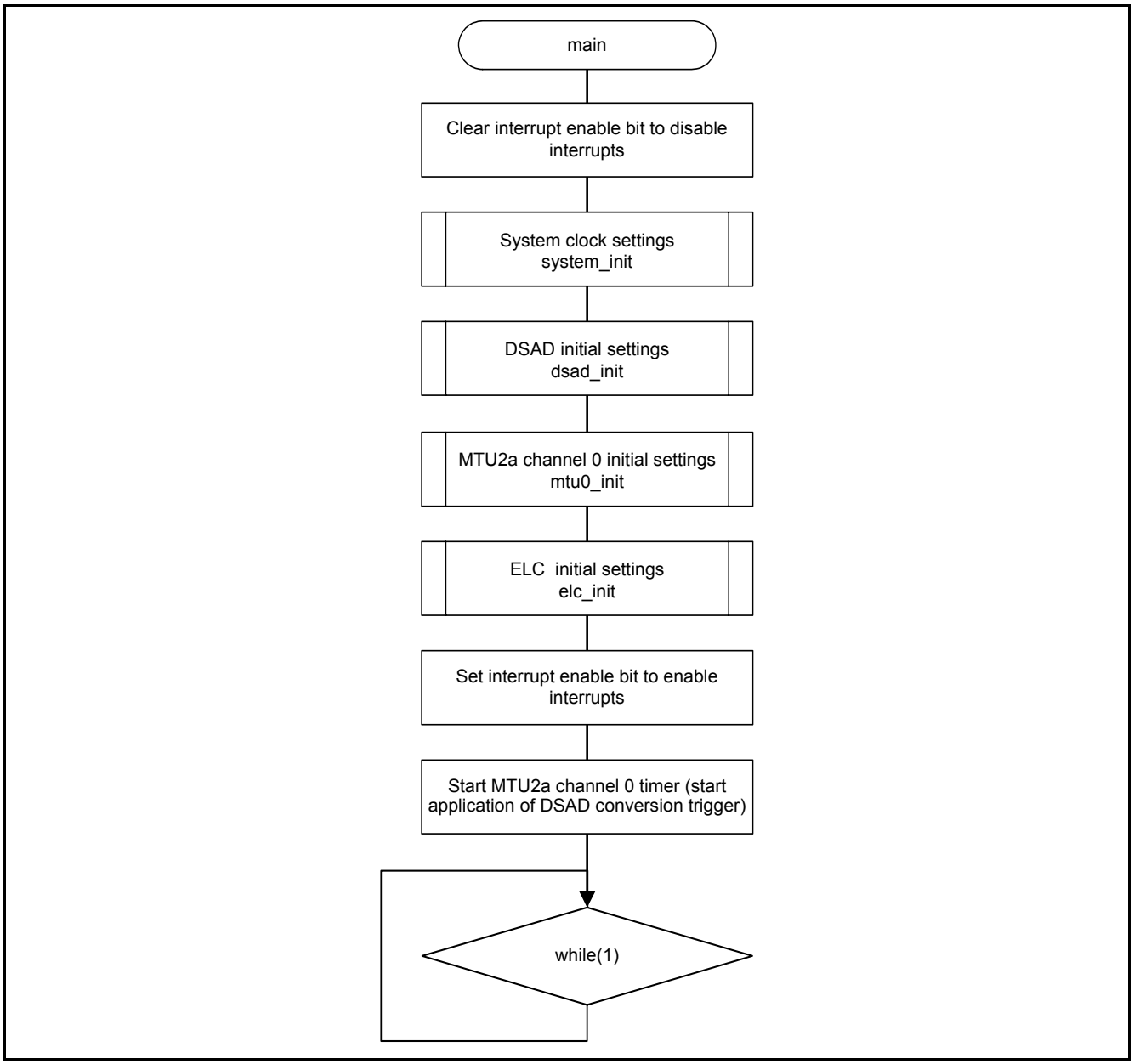
The internal registers used by the sample program are listed below. Note that the setting values shown are those used by the sample program and differ from the initial (default) values. Bits of the internal registers that are not listed may also have functions assigned to them. Therefore, be careful not to change the settings of bits other than those listed.

Timer start register (TSTR) **Number of bits: 8** **Address: 0008 8680h**

The TSTR register starts or stops TCNT operation in MTU0 to MTU4.

Bit	Symbol	Setting Value	R/W	Function
b0	CST0	1	R/W	MTU0.TCNT performs count operation.

(5) Flowchart


main
Clear interrupt enable bit to disable interrupts
System clock settings
system_init
DSAD initial settings
dsad_init
MTU2a channel 0 initial settings
mtu0_init
ELC initial settings
elc_init
Set interrupt enable bit to enable interrupts
Start MTU2a channel 0 timer (start application of DSAD conversion trigger)
while(1)

5.4.2 system_init Function

(1) Outline of Function

Initializes the system clock and cancels module stop.

(2) Arguments

None

(3) Return Values

None

(4) Internal Registers Used

The internal registers used by the sample program are listed below. Note that the setting values shown are those used by the sample program and differ from the initial (default) values. Bits of the internal registers that are not listed may also have functions assigned to them. Therefore, be careful not to change the settings of bits other than those listed.

Protect register (PRCR) **Number of bits: 16** **Address: 0008 03FEh**

The PRCR register protects important registers so that their contents cannot be overwritten.

Bit	Symbol	Setting Value	R/W	Function
b0	PRC0	1	R/W	Protect bit 0. Enables or disables writing to registers related to the clock generation circuit. 0: Write disabled 1: Write enabled
b1	PRC1	1	R/W	Protect bit 1. Enables or disables writing to registers related to operating modes, the low power consumption function, and software reset. 0: Write disabled 1: Write enabled
b15 to b8	PRKEY[7:0]	A5h	R/W	PRC key code bits. Enables or disables overwriting of bits PRC0, PRC1, and PRC3. When writing a value to one or more of the PRCi bits (I = 0, 1, or 3), write A5h to this bit field. If the value written to the PRKEY[7:0] bits is other than A5h, the values of the PRCi bits do not change even when a write to the PRCR register is executed.

System clock control register (SCKCR) Number of bits: 32 Address: 0008 0020h

The SCKCR register is used to select the frequencies of the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), FlashIF clock (FCLK) and bus clock (BCLK).

Bit	Symbol	Setting Value	R/W	Function
b3 to b0	PCKD[3:0]	0010b	R/W	Selects the peripheral module clock (PCLKD) frequency.*1 Selects a division ratio of 4 for the PCLKD clock source.
b7 to b4	PCKC[3:0]	0010b	R/W	Selects the peripheral module clock (PCLKC) frequency.*1 Selects a division ratio of 4 for the PCLKD clock source.
b11 to b8	PCKB[3:0]	0010b	R/W	Selects the peripheral module clock (PCLKB) frequency.*1 Selects a division ratio of 4 for the PCLKB clock source.
b15 to b12	PCKA[3:0]	0001b	R/W	Selects the peripheral module clock (PCLKA) frequency.*1 Selects a division ratio of 2 for the PCLKA clock source.
b19 to b16	BCK[3:0]	0010b	R/W	Selects the external bus clock (BCLK) frequency.*2 Selects a division ratio of 4 for the BCLK clock source.
b23 to b20	—	0000b	R/W	These bits are read as 0. The write value should be 0.
b27 to b24	ICK[3:0]	0001b	R/W	Selects the system clock (ICLK) frequency.*1 Selects a division ratio of 2 for the ICLK clock source.
b31 to b28	FCK[3:0]	0010b	R/W	Selects the FlashIF clock (FCLK) frequency.*1 Selects a division ratio of 4 for the FCLK clock source.

Notes: 1. A setting of division by one is prohibited when the PLL is selected.
2. The RX21A Group has no external bus, but the external bus clock (BCLK) select bits must be set. For details, see RX21A Group User's Manual: Hardware.

System clock control register 3 (SCKCR3) Number of bits: 16 Address: 0008 0026h

The SCKCR3 register selects the clock source of the system clock.

Bit	Symbol	Setting Value	R/W	Function
b10 to b8	CKSEL[2:0]	100b	R/W	Clock source select bits Selects PLL as the clock source.

PLL control register (PLLCR) Number of bits: 16 Address: 0008 0028h

The PLLCR register contains operation settings for the PLL circuit. Writing to the PLLCR register is prohibited when the value of the PLLEN bit in PLLCR2 is 0 (PLL operates).

Bit	Symbol	Setting Value	R/W	Function
b1 to b0	PLIDIV[1:0]	01b	R/W	An input frequency division ratio of 2 is selected for the PLL clock source.
b12 to b8	STC[4:0]	01001b	R/W	A multiplication factor of 10 is selected for the PLL frequency.

PLL control register 2 (PLLCR2) **Number of bits: 8** **Address: 0008 002Ah**

The PLLCR2 register controls the operation of the PLL circuit. After changing the PLL operation setting by means of the PLLEN bit, wait for the PLL clock oscillation stabilization wait time (tPLLWT1 or tPLLWT2) to elapse before staring to use the PLL clock.

Bit	Symbol	Setting Value	R/W	Function
b0	PLLEN	0	R/W	Enables PLL operation.

Main clock oscillator control register (MOSCCR) **Number of bits: 8** **Address: 0008 0032h**

The MOSCCR register controls the operation of the main clock oscillator.

Bit	Symbol	Setting Value	R/W	Function
b0	MOSTP	0	R/W	Enables main clock oscillator operation.

High-speed on-chip oscillator control register (HOCOCR) **Number of bits: 8** **Address: 0008 0036h**

The HOCOCR register controls the operation of the high-speed on-chip oscillator (HOCO).

Bit	Symbol	Setting Value	R/W	Function
b0	HCSTP	1	R/W	Stops HOCO.

Module stop control register A (MSTPCRA) **Number of bits: 32** **Address: 0008 0010h**

The MSTPCRA register controls the module stop state of various on-chip modules.

Bit	Symbol	Setting Value	R/W	Function
b9	MSTPA9	0	R/W	Multi-function timer pulse unit module stop setting bit Cancels the module stop state.
b25	MSTPA25	0	R/W	DSAD module stop setting bit Cancels the module stop state.

Module stop control register B (MSTPCRB) **Number of bits: 32** **Address: 0008 0014h**

The MSTPCRB register controls the module stop state of various on-chip modules.

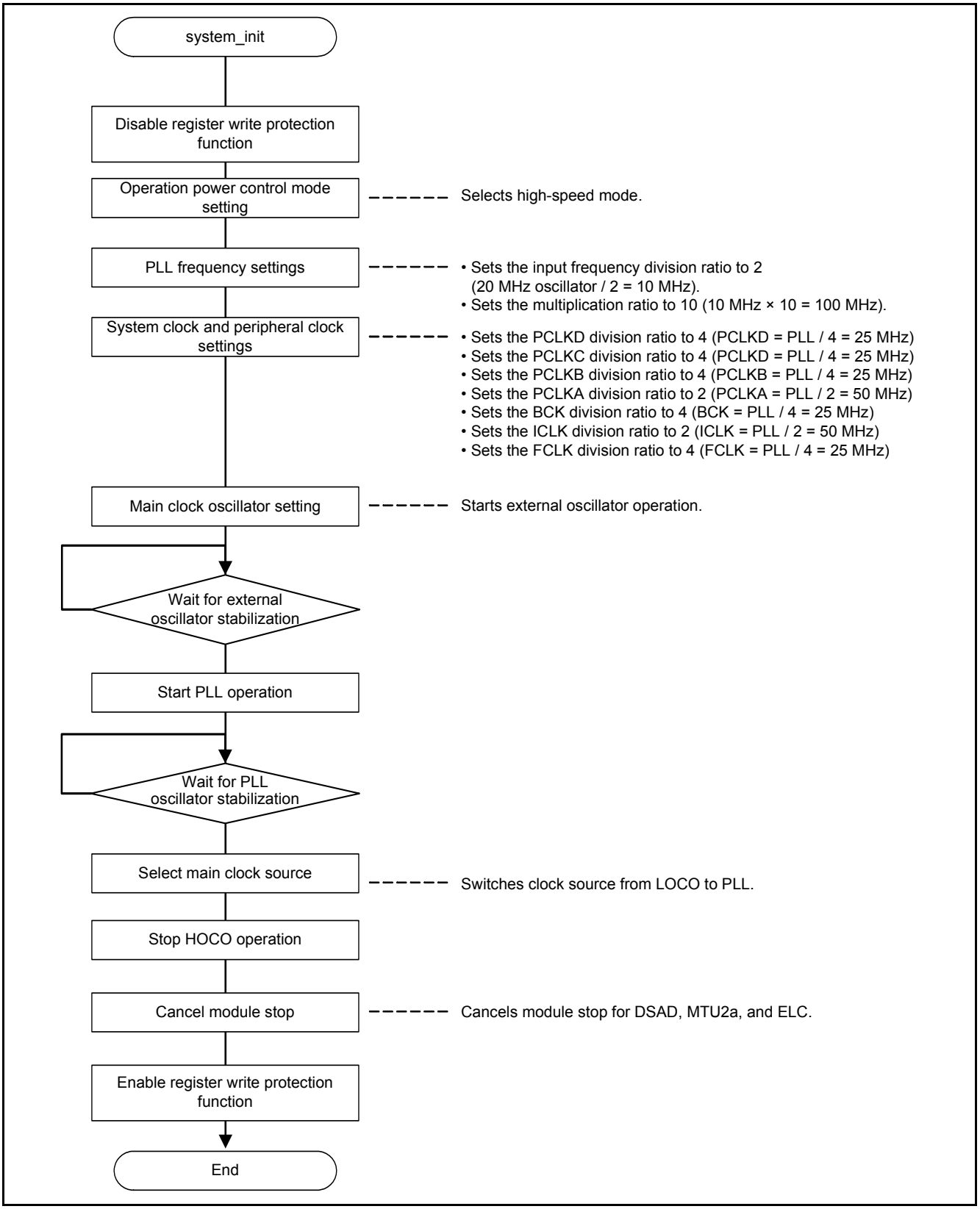
Bit	Symbol	Setting Value	R/W	Function
b9	MSTPB9	0	R/W	ELC module stop setting bit Cancels the module stop state.

Operating power control register (OPCCR) **Number of bits: 8** **Address: 0008 00A0h**

The OPCCR register used to reduce power consumption in normal operating mode, sleep mode, and all-module clock stop mode.

Bit	Symbol	Setting Value	R/W	Function
b2 to b0	OPCM[2:0]	000b	R/W	Operating power control mode select bits Selects high-speed operating mode.
b3	—			These bits are read as 0. The write value should be 0.
b4	OPCMTSF	0b		• Read 0: Transition completed 1: Transition in progress • Write The write value should be 0.
b7 to b5	—			These bits are read as 0. The write value should be 0.

(5) Flowchart


system_init
Disable register write protection function
Operation power control mode setting
Selects high-speed mode.
PLL frequency settings
• Sets the input frequency division ratio to 2 (20 MHz oscillator / 2 = 10 MHz).
• Sets the multiplication ratio to 10 (10 MHz × 10 = 100 MHz).
System clock and peripheral clock settings
• Sets the PCLKD division ratio to 4 (PCLKD = PLL / 4 = 25 MHz)
• Sets the PCLKC division ratio to 4 (PCLKD = PLL / 4 = 25 MHz)
• Sets the PCLKB division ratio to 4 (PCLKB = PLL / 4 = 25 MHz)
• Sets the PCLKA division ratio to 2 (PCLKA = PLL / 2 = 50 MHz)
• Sets the BCK division ratio to 4 (BCK = PLL / 4 = 25 MHz)
• Sets the ICLK division ratio to 2 (ICLK = PLL / 2 = 50 MHz)
• Sets the FCLK division ratio to 4 (FCLK = PLL / 4 = 25 MHz)
Main clock oscillator setting
Starts external oscillator operation.
Wait for external oscillator stabilization
Start PLL operation
Wait for PLL oscillator stabilization
Select main clock source
Switches clock source from LOCO to PLL.
Stop HOCO operation
Cancel module stop
Cancels module stop for DSAD, MTU2a, and ELC.
Enable register write protection function
End

5.4.3 dsad_init Function

(1) Outline of Function

This function makes initial settings to the DSAD module. The PGA gain is set to ×1 for the DSAD's differential input channels and single-ended input channels, and the on-chip BGR is selected as the source of the reference voltage.

(2) Arguments

None

(3) Return Values

None

(4) Internal Registers Used

The internal registers used by the sample program are listed below. Note that the setting values shown are those used by the sample program and differ from the initial (default) values. Bits of the internal registers that are not listed may also have functions assigned to them. Therefore, be careful not to change the settings of bits other than those listed.

ΔΣ A/D reference control register (DSADRCR) Number of bits: 8 Address: 0008 B402h

The ΔΣ A/D reference control register controls supply of the reference voltage to the ΔΣ A/D converter and controls the on-chip BGR.

Bit	Symbol	Setting Value	R/W	Function
b6	BGRE	1	R/W	Activates the BGR circuit.
b7	EXREF	0	R/W	Reference voltage is generated by the on-chip BGR circuit.

ΔΣ A/D control registers 0 to 6 (DSADCR0 to DSADCR6) Number of bits: 8
Addresses: DSADCR0 0008 B410h, DSADCR1 0008 B420h, DSADCR2 0008 B430h, DSADCR3 0008 B440h, DSADCR4 0008 B450h, DSADCR5 0008 B460h, DSADCR6 0008 B470h

The ΔΣ A/D control registers activate or stop the PGA and ΔΣ modulator of their corresponding channels.

Bit	Symbol	Setting Value	R/W	Function
b7	ADSE	1	R/W	Activates the PGA and ΔΣ modulator.

ΔΣ A/D gain select registers 0 to 3 (DSADGSR0 to DSADGSR3) Number of bits: 8
Addresses: DSADGSR0 0008 B412h, DSADGSR1 0008 B422h DSADGSR2 0008 B432h, DSADGSR3 0008 B442h

ΔΣ A/D gain select registers 0 to 3 select the gain of their corresponding differential input channels.

Bit	Symbol	Setting Value	R/W	Function
b2 to b0	GAIN[2:0]	000b	R/W	Sets the gain of the differential input channel to ×1.

ΔΣ A/D gain select registers 4 to 6 (DSADGSR4 to DSADGSR6) Number of bits: 8
Addresses: DSADGSR4 0008 B452h, DSADGSR5 0008 B462h, DSADGSR6 0008 B472h

ΔΣ A/D gain select registers 4 to 6 select the gain of their corresponding single-ended input channels.

Bit	Symbol	Setting Value	R/W	Function
b1 to b0	GAIN[1:0]	00b	R/W	Sets the gain of the single-ended input channel to ×1.

ΔΣ A/D reset register (DSADRSTR) Number of bits: 8 Address: 0008 B401h

The ΔΣ A/D reset register initializes the PGA and ΔΣ modulator units. Writing 1 to the DSRST bit initializes the PGA and ΔΣ modulator of all the channels. Perform this initialization before starting A/D conversion. Perform initialization after the startup time of the VREFDSH pin voltage, VCOMDS pin voltage, PGAs, and ΔΣ modulators has elapsed. Clearing takes place automatically 192 cycles of peripheral module clock B (PCLKB) after 1 is written to DSRST. Writing 0 to DSRST has no effect when it is set to 1. After initialization, confirm that DSRST has been cleared to 0 before starting A/D conversion.

Bit	Symbol	Setting Value	R/W	Function
b7	DSRST	1	R/W	Initializes the ΔΣ modulator units.

ΔΣ A/D control/status registers 0 to 6 (DSADCSR0 to DSADCSR6) Number of bits: 8
Addresses: DSADCSR0 0008 B411h, DSADCSR1 0008 B421h, DSADCSR2 0008 B431h, DSADCSR3 0008 B441h, DSADCSR4 0008 B451h, DSADCSR5 0008 B461h, DSADCSR6 0008 B471h

ΔΣ A/D control/status registers 0 to 6 enable or disable, on their corresponding channels, A/D conversion end interrupt requests, enable or disable data register overwrite interrupt requests, and A/D conversion start by trigger.

Bit	Symbol	Setting Value	R/W	Function
b3	TRGE	1	R/W	Enables A/D conversion start by trigger.
b4	ADIE	1	R/W	Enables DSADI interrupt at A/D conversion end.

Interrupt request enable register 19 (IER19) **Number of bits: 8** **Address: 0008 7219h**

This register enables or disables interrupt requests to the CPU and DMACA/DTC activation requests.

Bit	Symbol	Setting Value	R/W	Function
b7	IEN7	1	R/W	DSADI0 interrupt request enable bit Enables interrupt requests.

Interrupt request enable register 1A (IER1A) **Number of bits: 8** **Address: 0008 721Ah**

This register enables or disables interrupt requests to the CPU and DMACA/DTC activation requests.

Bit	Symbol	Setting Value	R/W	Function
b0	IEN0	1	R/W	DSADI1 interrupt request enable bit Enables interrupt requests.
b1	IEN1	1	R/W	DSADI2 interrupt request enable bit Enables interrupt requests.
b2	IEN2	1	R/W	DSADI3 interrupt request enable bit Enables interrupt requests.
b3	IEN3	1	R/W	DSADI4 interrupt request enable bit Enables interrupt requests.
b4	IEN4	1	R/W	DSADI5 interrupt request enable bit Enables interrupt requests.
b5	IEN5	1	R/W	DSADI6 interrupt request enable bit Enables interrupt requests.

Interrupt source priority register n (IPRn) (n = 207 to 213) **Number of bits: 8**

The IPRn registers specify the priority of their corresponding interrupt sources.

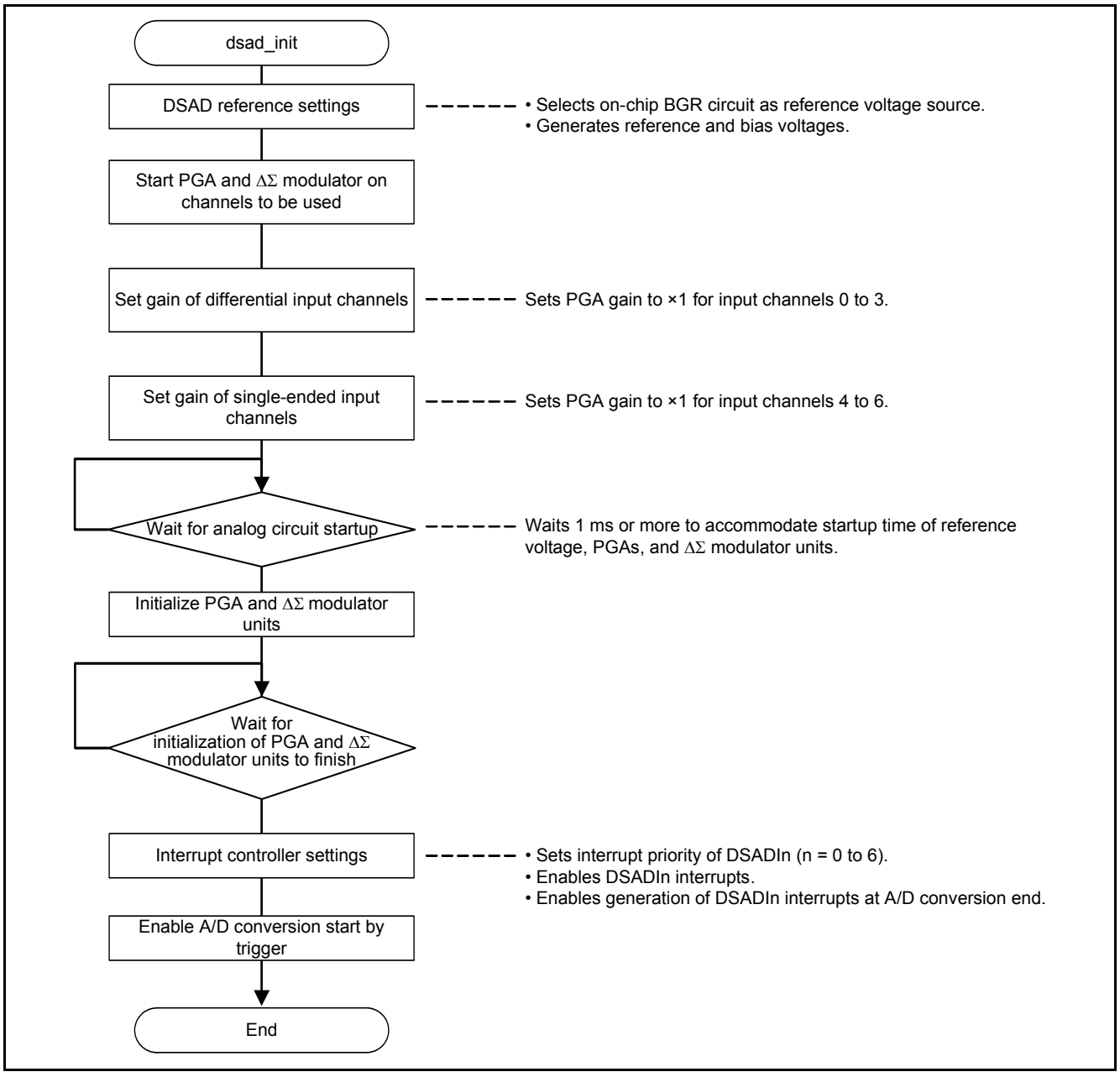
Bit	Symbol	Setting Value	R/W	Function
b3 to b0	IPR[3:0]	0111b	R/W	Specifies interrupt priority level 1.

Table 7 lists the interrupt source priority register used by the sample program.

Table 7 Interrupt Source Priority Registers

Interrupt Name	Interrupt Vector Number	Symbol	Address	Access Size
DSADI0	207	IPR207	0008 73CFh	8
DSADI1	208	IPR208	0008 73D0h	8
DSADI2	209	IPR209	0008 73D1h	8
DSADI3	210	IPR210	0008 73D2h	8
DSADI4	211	IPR211	0008 73D3h	8
DSADI5	212	IPR212	0008 73D4h	8
DSADI6	213	IPR213	0008 73D5h	8

(5) Flowchart


dsad_init
DSAD reference settings
• Selects on-chip BGR circuit as reference voltage source.
• Generates reference and bias voltages.
Start PGA and ΔΣ modulator on channels to be used
Set gain of differential input channels
Sets PGA gain to ×1 for input channels 0 to 3.
Set gain of single-ended input channels
Sets PGA gain to ×1 for input channels 4 to 6.
Wait for analog circuit startup
Waits 1 ms or more to accommodate startup time of reference voltage, PGAs, and ΔΣ modulator units.
Initialize PGA and ΔΣ modulator units
Wait for initialization of PGA and ΔΣ modulator units to finish
Interrupt controller settings
• Sets interrupt priority of DSADIn (n = 0 to 6).
• Enables DSADIn interrupts.
• Enables generation of DSADIn interrupts at A/D conversion end.
Enable A/D conversion start by trigger
End

5.4.4 mtu0_init Function

(1) Outline of Function

This function makes initial settings for MTU2a channel 0.

The following settings are applied to MTU2a channel 0: the operating mode is PWM mode 1, the PWM period is the DSAD's minimum conversion period of 81.92 μs, and the high duration is 1.0 μs.

(2) Arguments

None

(3) Return Values

None

(4) Internal Registers Used

The internal registers used by the sample program are listed below. Note that the setting values shown are those used by the sample program and differ from the initial (default) values. Bits of the internal registers that are not listed may also have functions assigned to them. Therefore, be careful not to change the settings of bits other than those listed.

Timer control register (TCR) Number of bits: 8 Address: MTU0.TCR 0008 8700h

TCR is an 8-bit readable/writable register that controls TCNT for each channel. Settings to the TCR register should be made when TCNT operation is stopped.

Bit	Symbol	Setting Value	R/W	Function
b2 to b0	TPSC[2:0]	000b	R/W	Counting takes place with no frequency division of the internal clock (PCLKB).
b4 to b3	CKEG[1:0]	00b	R/W	Counting takes place at the rising edge.
b7 to b5	CCLR[2:0]	001b	R/W	TCNT is cleared at TGRA compare match/input capture.

Timer mode register (TMDR) Number of bits: 8 Address: MTU0.TMDR 0008 8701h

TMDR is an 8-bit readable/writable register that specifies the operating mode for each channel. Settings to the TMDR register should be made when TCNT operation is stopped.

Bit	Symbol	Setting Value	R/W	Function
b3 to b0	MD[3:0]	0010b	R/W	Specifies PWM mode 1.

Timer general registers (TGR) Number of bits: 16
Addresses: MTU0.TGRA 0008 8708h, MTU0.TGRB 0008 870Ah

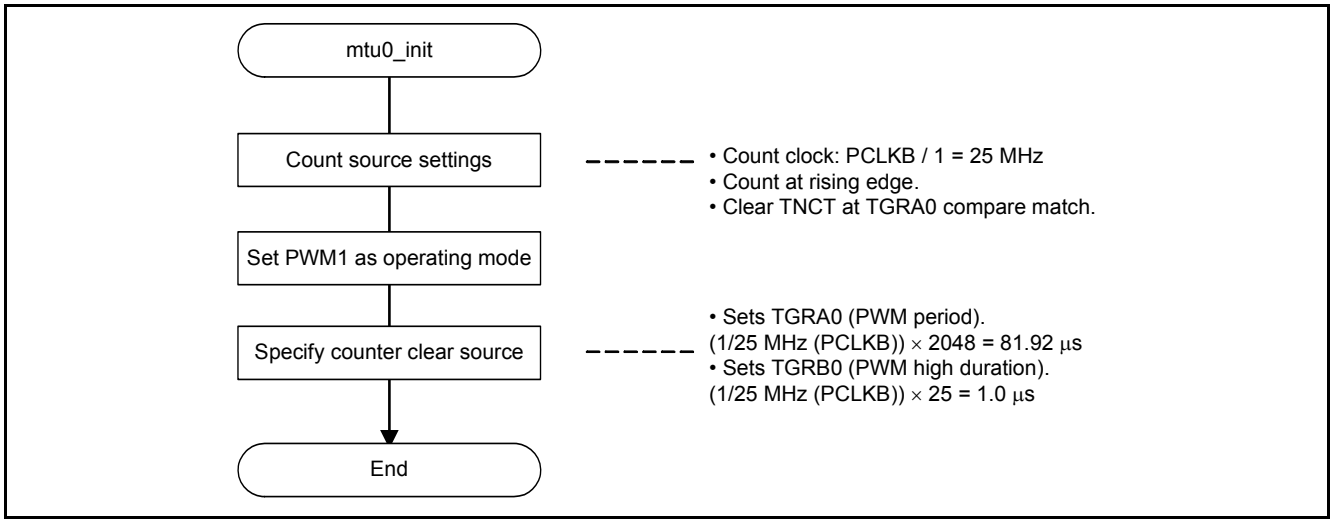
The TGR registers are 16-bit readable/writable registers. TGRA, TGRB, TGRC, and TGRD function as either output compare or input capture registers.

Note: Accessing the TGR registers in 8-bit units is prohibited. They must always be accessed in 16-bit units. The initial value of each TGR register is FFFFh.

Register Name	Setting Value	R/W	Function
MTU0.TGRA	07FFh	R/W	Specifies a value such that the PWM output period is 81.92 µs.

Register Name	Setting Value	R/W	Function
MTU0.TGRB	0018h	R/W	Specifies a value such that the PWM high duration is 1.0 µs.

(5) Flowchart



5.4.5 elc_init Function

(1) Outline of Function

This function makes initial settings for the ELC.

(2) Arguments

None

(3) Return Values

None

(4) Internal Registers Used

The internal registers used by the sample program are listed below. Note that the setting values shown are those used by the sample program and differ from the initial (default) values. Bits of the internal registers that are not listed may also have functions assigned to them. Therefore, be careful not to change the settings of bits other than those listed.

Event link control register (ELCR) Number of bits: 8 Address: 0008 B100h

The ELCR register controls the operation of the event link controller (ELC).

Bit	Symbol	Setting Value	R/W	Function
b7	ELCON	1	R/W	Enables all event links.

Event link setting register n (n = 0 to 6) Number of bits: 8
Addresses: ELSR30: 0008 B130h, ELSR31: 0008 B131h, ELSR32: 0008 B132h
ELSR33: 0008 B133h, ELSR34: 0008 B134h, ELSR35: 0008 B135h
ELSR36: 0008 B136h

Bit	Symbol	Setting Value	R/W	Function
b7 to b0	ELS[7:0]	0000 0010b (0002h)	R/W	Each ELSRn register specifies an event signal that is linked to its corresponding peripheral module. Specifies the MTU2 channel 0 compare match 0B signal.

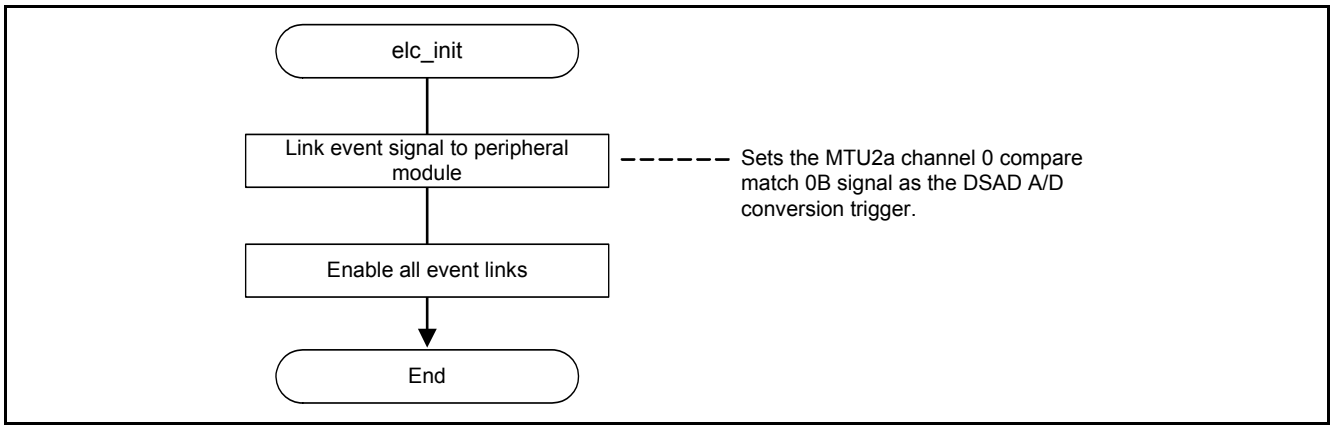
Each ELSRn register specifies an event signal that is linked to its corresponding peripheral module.

Table 8 lists the ELSRn registers and their corresponding peripheral modules.

Table 8 ELSRn Registers and Their Corresponding Peripheral Functions

Register Name (User's Manual)	Peripheral Function (Module)	Register Name in iodefine.h
ELSR30	24-bit ΔΣ A/D converter channel 0	ELSRB[0]
ELSR31	24-bit ΔΣ A/D converter channel 1	ELSRB[1]
ELSR32	24-bit ΔΣ A/D converter channel 2	ELSRB[2]
ELSR33	24-bit ΔΣ A/D converter channel 3	ELSRB[3]
ELSR34	24-bit ΔΣ A/D converter channel 4	ELSRB[4]
ELSR35	24-bit ΔΣ A/D converter channel 5	ELSRB[5]
ELSR36	24-bit ΔΣ A/D converter channel 6	ELSRB[6]

(5) Flowchart


elc_init
Link event signal to peripheral module
Sets the MTU2a channel 0 compare match 0B signal as the DSAD A/D conversion trigger.
Enable all event links
End

5.4.6 dsadi*n*_isr Function (*n* = 0 to 6)

(1) Outline of Function

This function stores the channel n conversion data in RAM (see 5.3) when the DSAD channel n conversion end interrupt occurs, then clears the interrupt request (DSADIn). Equivalent interrupt handling is performed for DSAD input channels 0 to 6.

(2) Arguments

None

(3) Return Values

None

(4) Internal Registers Used

The internal registers used by the sample program are listed below. Note that the setting values shown are those used by the sample program and differ from the initial (default) values. Bits of the internal registers that are not listed may also have functions assigned to them. Therefore, be careful not to change the settings of bits other than those listed.

Interrupt request register n (IRn) (n = interrupt vector number) **Number of bits: 8**

IRn is the interrupt request status register.

Bit	Symbol	Setting Value	R/W	Function
b0	IR	0	R/W	Interrupt request status flag This bit is set to 1 when an interrupt request occurs.

Table 9 lists the interrupt controller registers used by the sample program.

Table 9 Interrupt Controller Registers

Interrupt Name	Interrupt Vector Number	Symbol	Address	Access Size
DSADI0	207	IR207	0008 70CFh	8
DSADI1	208	IR208	0008 70D0h	8
DSADI2	209	IR209	0008 70D1h	8
DSADI3	210	IR210	0008 70D2h	8
DSADI4	211	IR211	0008 70D3h	8
DSADI5	212	IR212	0008 70D4h	8
DSADI6	213	IR213	0008 70D5h	8

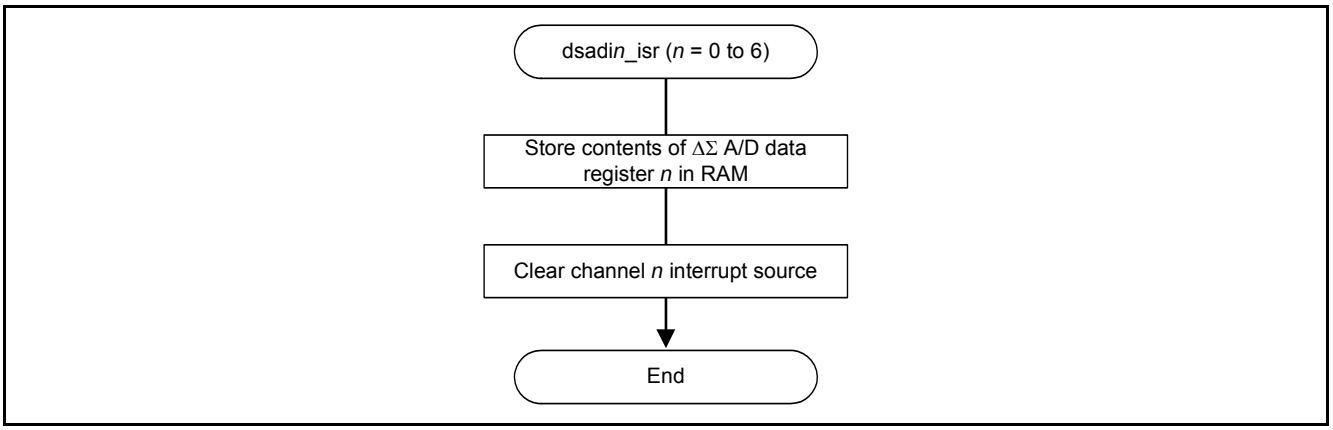
ΔΣ A/D data registers 0 to 6 (DSADDR0 to DSADDR6) **Number of bits: 8**

Addresses: DSADDR0 0008 B414h, DSADDR1 0008 B424h, DSADDR2 0008 B434h, DSADDR3 0008 B444h, DSADDR4 0008 B454h, DSADDR5 0008 B464h, DSADDR6 0008 B474h

ΔΣ A/D conversion data registers 0 to 6 are 32-bit read-only registers for storing the results of A/D conversion. A single register is provided for each analog input channel, and after A/D conversion on an analog input channel completes, the result is stored in the corresponding register. The stored data is retained until a new result is stored after the next A/D conversion completes. Reading from the register is always enabled. Writing is disabled. The data converted by A/D conversion is represented as a maximum of 26-bit signed data (two's complement), according to the conversion period, and is stored in bits 25 to 0 in the data register. The sign of the conversion data is stored in bits 31 to 26 in the data register.

Register Name	Setting Value	R/W	Function
DSADDRn (n = 0 to 6)	—	R	Stores the A/D conversion result as signed data (two's complement). The contents of the register are read as a longword.

(5) Flowchart



6. Usage Notes

6.1 ΔΣ A/D Converter Usage Notes

For usage notes on the ΔΣ A/D converter, see RX21A Group User's Manual: Hardware.

6.2 Execution Time of Interrupt Handling

The sample program uses interrupts DSADI0 to DSADI6 to generate the timer period (81.92 µs in this case) used as the DSAD conversion trigger. Keep the following points in mind in order to maintain the interrupt generation interval:

- When adding handling routines for interrupts DSADI0 to DSADI6, make sure that the total time required for interrupt handling is less than the timer period.
- When adding handling routines for interrupts other than DSADI, examine the interrupt priority sequence carefully.
- If the total time required for handling all the interrupts exceeds the timer period, adjust the timer period used as the DSAD conversion trigger.

7. Reference Documents

- Product Documentation
  The latest versions of the following documents are available on the Renesas Electronics Web site.
  [1] RX21A Group User's Manual: Hardware
  [2] RX Family User's Manual: Software
  [3] RX Family C/C++ Compiler Package User's Manual
- Technical Updates/Technical News
  The latest information is available on the Renesas Electronics Web site.
- Hokuto Electronic Co., Ltd., Web Site
  Product information on controller boards is available on the Hokuto Electronic Web site.
  http://www.hokutodenshi.co.jp/
  The content of this application note has been verified using the HSBRX21AP-B (mounted with R5F521A8BDFP).

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REVISION HISTORY	RX21A Group Application Note Example Settings for Simultaneous Conversion on Seven Channels of 24-Bit ΔΣ A/D Converter

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 20, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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