

# RX Family, H8SX Family

## Points of Difference between RCAN-TL1 (H8SX Family) and CAN (RX Family)

### Summary

This application note is intended as a reference document for customers using the controller area network (RCAN-TL1) module on the H8SX Family who are considering migrating to the RX Family. It details points of difference between the RCAN-TL1 module of the H8SX Family and the CAN module of the RX Family.

Of the products listed as target devices, this application note compares the CAN modules of the groups listed in Table 1. For details of devices not listed in Table 1, refer to the applicable user's manual.

In addition, the RSCAN module of the RX200 Series is not covered in this application note because it completely lacks software compatibility with the CAN module used as the comparison source. Refer to section 5, Related Documents, regarding differences between RSCAN and CAN modules of RX Family MCUs.

**Table 1 CAN Specification Comparison Target Devices**

| Subject of Comparison | Family      | Group                       | CAN Module |
|-----------------------|-------------|-----------------------------|------------|
| Comparison source     | H8SX Family | H8SX/1720S Group            | RCAN-TL1   |
| Comparison target     | RX Family   | RX65N Group and RX651 Group | CAN        |

### Target Devices

Devices among the following products equipped with CAN modules.

Devices with RCAN-TL1 modules

H8SX/1720S Group

Devices with CAN modules

RX600 Series and RX700 Series

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## 1. Differences between Functions

Differences between functions are shown below. Items that exist only on one group but not the other or that exist on both groups but with points of difference are indicated in **red**.

**Table 1.1 Differences between Functions of H8SX/1720S (RCAN-TL1) and RX65N (CAN)**

| Item              |                                                                                               | H8SX/1720S (RCAN-TL1)                                                                                                                                                                                                            | RX65N (CAN)                                                                                                                                                                                                                                                      |
|-------------------|-----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Protocol          |                                                                                               | Bosch 2.0B active compatible (ISO 11898-1 standard)                                                                                                                                                                              |                                                                                                                                                                                                                                                                  |
|                   |                                                                                               | Time trigger compatible (ISO 11898-4 standard)                                                                                                                                                                                   | No                                                                                                                                                                                                                                                               |
| Bit rate          | Communication speed                                                                           | Max. 1 Mbps                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                  |
|                   | Bit rate equation                                                                             | $fCLK / (2 \times (BRP + 1) \times (TSEG1 + TSEG2 + 1))$ <p>fCLK: Peripheral bus clock</p> <p>BRP: Baud rate prescaler (fCLK divided by (2 × (setting value + 1)))</p> <p>TSEG1 and TSEG2: Time segment 1 and time segment 2</p> | $fCAN / ((BRP + 1) \times (1 + TSEG1 + TSEG2))$ <p>fCAN: <b>Peripheral clock or main clock</b></p> <p>BRP: Baud rate prescaler (<b>fCAN divided by (setting value + 1)</b>)</p> <p>TSEG1 and TSEG2: Time segment 1 and time segment 2</p>                        |
| Channels          |                                                                                               | 2 channels                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                  |
| ID Format         |                                                                                               | Specify standard ID or extended ID can be by the MBj.IDE bit of each mailbox.                                                                                                                                                    | <ul style="list-style-type: none"> <li>Specify ID format of all mailboxes with ID format mode bit (IDFM)</li> <li>When Mixed ID mode is selected in ID format mode bit (IDFM), specify standard ID or extended ID by the MBj.IDE bit of each mailbox.</li> </ul> |
| Mailboxes         | Buffer configuration                                                                          | 32 buffers per channel (receive-only × 1, settable for transmission/reception × 31)                                                                                                                                              | 32 buffers per channel (settable for transmission/reception × 32)                                                                                                                                                                                                |
|                   | FIFO mailbox mode                                                                             | No                                                                                                                                                                                                                               | Settable for transmission/reception × 24, ability to set 4 FIFO stages for transmission and 4 FIFO stages for reception                                                                                                                                          |
|                   | 64 mailboxes function (One channel of 64 mailboxes configured from two channels of mailboxes) | Yes                                                                                                                                                                                                                              | No                                                                                                                                                                                                                                                               |
|                   | ID reorder                                                                                    | Yes<br>Note: Function compatible with HCAN2                                                                                                                                                                                      | No                                                                                                                                                                                                                                                               |
| Data transmission | Transmission priority selection                                                               | Mailbox (buffer) number order (high-to-low)<br>Message priority (identifier) high-to-low order                                                                                                                                   | Mailbox (buffer) number order ( <b>low-to-high</b> )<br>Message priority (identifier) high-to-low order                                                                                                                                                          |

| Item                    |                                                        | H8SX/1720S (RCAN-TL1)                                                                   | RX65N (CAN)                                                                                                                                                                                                               |
|-------------------------|--------------------------------------------------------|-----------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                         | Ability to cancel transmission requests                | Supported                                                                               | Supported<br><b>Note:</b> The register manipulation method differs. Refer to 2.5, Mailbox Transmission/Reception Setting Details.                                                                                         |
|                         | One-shot transmission function                         | No                                                                                      | Single transmission only (no retransmission even in case of CAN bus error or arbitration lost)                                                                                                                            |
| Data reception          | Data frame and remote frame reception                  | Ability to receive both data frames and remote frames                                   | Ability to receive <b>either</b> data frames <b>or</b> remote frames<br><b>Note:</b> In FIFO mailbox mode, reception of both types of frames can be enabled by setting the FIDCR0.RTR and FIDCR1.RTR bits in combination. |
|                         | Message ID masking function                            | Ability to make masking settings per mailbox (has masking setting field in the mailbox) | Ability to make 8 masking settings (each affecting 4 mailboxes).<br><b>All mailboxes are covered.</b>                                                                                                                     |
|                         | Selectable between overwrite mode and overrun mode     | Selectable                                                                              |                                                                                                                                                                                                                           |
|                         | One-shot reception function                            | No                                                                                      | Single reception only (Mailbox does not operate for reception after reception completes.)                                                                                                                                 |
| Transmission interrupts | Message transmission completion interrupt              | Yes                                                                                     |                                                                                                                                                                                                                           |
|                         | Message transmission cancellation completion interrupt | Yes                                                                                     | No<br><b>Note:</b> It is possible to use the transmission abort complete flag (TRMABT) for confirmation.                                                                                                                  |
|                         | Transmit FIFO interrupt                                | No                                                                                      | Yes                                                                                                                                                                                                                       |
| Reception interrupts    | Message reception interrupt                            | Yes                                                                                     |                                                                                                                                                                                                                           |
|                         | Remote frame reception interrupt                       | Yes                                                                                     | Yes<br><b>Note:</b> A message reception interrupt request is generated when a remote frame is received by a mailbox for which remote frame was selected by the remote transmission request bit (RTR).                     |
|                         | Reception FIFO interrupt                               | No                                                                                      | Yes                                                                                                                                                                                                                       |

| Item             |                                                                                                                        | H8SX/1720S (RCAN-TL1)                                                                              | RX65N (CAN)                                                                                                                                        |
|------------------|------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Error interrupts | Error passive interrupt (TEC $\geq$ 128 or REC $\geq$ 128)                                                             | Yes                                                                                                |                                                                                                                                                    |
|                  | Bus-off entry interrupt (TEC $\geq$ 256)                                                                               | Yes                                                                                                |                                                                                                                                                    |
|                  | Bus-off recovery interrupt (normal recovery from bus-off state (detection of 11 consecutive recessive bits 128 times)) | Yes                                                                                                |                                                                                                                                                    |
| Error interrupts | Error warning interrupt (TEC $\geq$ 96 or REC $\geq$ 96)                                                               | Yes<br>(Separate interrupts are generated for transmission errors and reception errors.)           | Yes<br>(Combined interrupts are generated for transmission errors and reception errors.)                                                           |
|                  | Overload frame transmission interrupt                                                                                  | Yes                                                                                                |                                                                                                                                                    |
|                  | Unread message overwrite interrupt                                                                                     | Yes                                                                                                | No<br>Note: It is possible to use the message lost flag (MSGLOST) for confirmation.                                                                |
|                  | Reception overrun interrupt                                                                                            | Yes                                                                                                |                                                                                                                                                    |
|                  | Bus lock interrupt (detection of 32 consecutive dominant bits on CAN bus)                                              | No                                                                                                 | Yes                                                                                                                                                |
|                  | Bus error interrupt (detection of stuff error, form error, etc., on CAN bus)                                           | No                                                                                                 | Yes                                                                                                                                                |
| Other interrupts | Reset processing interrupt                                                                                             | An interrupt is generated by a transition to reset mode due to a software reset or hardware reset. | No<br>Note: It is possible to use the power-on reset detect flag (PORF) or deep software standby reset flag (DPSRSTF) to determine the reset type. |
|                  | Halt interrupt                                                                                                         | An interrupt is generated by a transition to halt mode.                                            | No                                                                                                                                                 |
|                  | Sleep interrupt                                                                                                        | An interrupt is generated by a transition to sleep mode.                                           | No                                                                                                                                                 |
|                  | Start of new system matrix interrupt                                                                                   | An interrupt is generated when a message is sent or receive complete in the next system matrix.    | No                                                                                                                                                 |
|                  | Timer compare match interrupt                                                                                          | An interrupt is generated by a TCMR0 to TCMR3 compare match.                                       | No                                                                                                                                                 |
|                  | Timer overrun interrupt                                                                                                | An interrupt is generated by a timer (TCNTR) overrun.                                              | No                                                                                                                                                 |

| Item                                          |                                     | H8SX/1720S (RCAN-TL1)                                                                                                                                                                                                                                                                                                                                                                                                 | RX65N (CAN)                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                               | Next_is_Gap reception interrupt     | An interrupt is generated by receiving a time reference message with Next_is_Gap.                                                                                                                                                                                                                                                                                                                                     | No                                                                                                                                                                                                                                                                                                                                                                                                         |
|                                               | Message error interrupt             | An interrupt is generated by the occurrence of a message error when in test mode.                                                                                                                                                                                                                                                                                                                                     | No                                                                                                                                                                                                                                                                                                                                                                                                         |
|                                               | CAN bus operation interrupt         | An interrupt is generated when CAN bus operation (dominant bit detection) occurs when in sleep mode.                                                                                                                                                                                                                                                                                                                  | No                                                                                                                                                                                                                                                                                                                                                                                                         |
| Hardware reset                                | Initialized registers               | All registers except message control field 0 (CONTROL0), local acceptance filter mask (LAFM), and message data fields (MSG_DATA_0 to MSG_DATA_7) allocated in RAM among the mailboxes                                                                                                                                                                                                                                 | All registers except MKRk, FIDCR, MKIVLR, MIER, TFPCR, RFPCR, CSSR, AFSR, and mailboxes.                                                                                                                                                                                                                                                                                                                   |
|                                               | State transition after reset        | Configuration mode (reset mode)                                                                                                                                                                                                                                                                                                                                                                                       | Sleep mode                                                                                                                                                                                                                                                                                                                                                                                                 |
|                                               | Initial setting process after reset | Perform in configuration mode (reset mode).                                                                                                                                                                                                                                                                                                                                                                           | Perform in reset mode after cancelling sleep mode.                                                                                                                                                                                                                                                                                                                                                         |
| Software reset                                | Initialized registers               | All registers except MCR0 bit.<br><br>(Except message control field 0 (CONTROL0), local acceptance filter mask (LAFM), and message data fields (MSG_DATA_0 to MSG_DATA_7) allocated in RAM among the mailboxes)                                                                                                                                                                                                       | MCTLj, STR (except SLPST and TFST bits), EIFR, RECR, TECE, TSR, MSSR, MSMR, RFCR, TFCR, TCR, and ECSR (except EDPM bit)                                                                                                                                                                                                                                                                                    |
| Default state (error active or error passive) | Transition method                   | Transition by means of control register                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                            |
| Bus-off state                                 | Transition method                   | Transition when transmission error counter TEC ≥ 256                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                            |
|                                               | Mode transition after recovery      | Three types of transitions are available:<br>1) Transition to error active at detection of 11 consecutive recessive bits 128 times in bus-off state<br>2) Switch to halt mode after transition to bus-off state (interrupt generated)<br>3) When a transition has been made from error passive mode to bus-off state, transition to error passive mode again at detection of 11 consecutive recessive bits 128 times. | Four selections are available:<br>1) Transition to error active at detection of 11 consecutive recessive bits 128 times in bus-off state<br>2) Switch to halt mode after transition to bus-off state (no interrupt)<br>3) Switch to halt mode when bus-off recovery occurs (interrupt generated)<br>4) Selection of manual transition (by a program) to error active state or halt mode from bus-off state |
| Configuration mode (reset mode)               | Transition method                   | Transition after hardware reset or by means of control register                                                                                                                                                                                                                                                                                                                                                       | Transition by means of control register                                                                                                                                                                                                                                                                                                                                                                    |

| Item                       |                                                                        | H8SX/1720S (RCAN-TL1)                                                                                                                                                                                                                                                                                       | RX65N (CAN)                                                                                                                                                                            |
|----------------------------|------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Sleep mode                 | Transition method                                                      | Transition by means of control register                                                                                                                                                                                                                                                                     | Transition by means of control register <b>or after a reset</b>                                                                                                                        |
|                            | Mode transition after cancellation                                     | Transition to error active state by means of control register setting or CAN bus operation (dominant bit) detection<br>Transition to halt mode by means of control register setting                                                                                                                         | <b>Transition to reset mode or halt mode by means of control register setting</b>                                                                                                      |
| Halt mode                  | Transition method                                                      | Transition by means of control register                                                                                                                                                                                                                                                                     |                                                                                                                                                                                        |
| Error status monitoring    | CAN bus error status monitoring                                        | Not supported (no dedicated flags)                                                                                                                                                                                                                                                                          | <b>Ability to monitor generation of CAN bus errors such as stuff errors, form errors, and ACK errors</b>                                                                               |
|                            | Reading the error counter                                              | Ability to read reception and transmission error counters                                                                                                                                                                                                                                                   |                                                                                                                                                                                        |
| DTC/DMAC transfer function |                                                                        | Ability to start the DMAC when a message is received<br>Only mailbox 0 is covered.                                                                                                                                                                                                                          | <b>No</b>                                                                                                                                                                              |
| Time stamp function        |                                                                        | <ul style="list-style-type: none"> <li>Time stamp function using a 16-bit counter</li> <li><b>Ability to set the source clock divisions to a maximum of 64 divisions</b></li> <li><b>Interrupt using compare match</b></li> </ul>                                                                           | <ul style="list-style-type: none"> <li>Time stamp function using a 16-bit counter</li> <li><b>Ability to select reference clock among 1-, 2-, 4- and 8-bit time periods</b></li> </ul> |
| Time trigger function      |                                                                        | <ul style="list-style-type: none"> <li>6-bit basic cycle counter for time trigger transmission</li> <li>Registers for time trigger exist</li> <li>Time trigger transmission and period transmission also supported</li> <li>Basic cycle counter can be embedded into a CAN frame and transmitted</li> </ul> | <b>No</b>                                                                                                                                                                              |
| Software support unit      |                                                                        | No                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"> <li><b>Acceptance filter support</b></li> <li><b>Mailbox search support</b></li> <li><b>Channel search support</b></li> </ul>                       |
| Test control               | Self-diagnostic function                                               | <ul style="list-style-type: none"> <li>Listen-only mode</li> <li>Self-test mode 1 (external loopback)</li> <li>Self-test mode 2 (internal loopback)</li> <li><b>Write error counter</b></li> <li><b>Error passive mode</b></li> </ul>                                                                       | <ul style="list-style-type: none"> <li>Listen-only mode</li> <li>Self-test mode <b>0</b> (external loopback)</li> <li>Self-test mode <b>1</b> (internal loopback)</li> </ul>           |
| PORT interface             | Enable/disable transmit/receive pins and monitor transmit/receive pins | Yes                                                                                                                                                                                                                                                                                                         | <b>No</b><br><b>Note: (Substitutes)</b><br><b>Enable/disable transmit/receive pins with MPC settings and monitor transmit/receive pins with PIDR registers</b>                         |

| Item        |                                               | H8SX/1720S (RCAN-TL1) | RX65N (CAN) |
|-------------|-----------------------------------------------|-----------------------|-------------|
| Module stop | Clock supply by means of module stop register | Yes                   |             |

## 2. Differences between Registers

Differences between registers are shown below. Items that exist only on one group but not the other or that exist on both groups but with points of difference are indicated in **red**.

### 2.1 Registers

**Table 2.1 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Registers**

| Item                                                    | H8SX/1720S (RCAN-TL1)                                                             | RX65N (CAN)                                                                                                                                                                                                       |
|---------------------------------------------------------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Control register                                        | Master control register (MCR)                                                     | Control register (CTLR)                                                                                                                                                                                           |
| Status flags                                            | General status register (GSR)                                                     | <ul style="list-style-type: none"> <li>Status register (STR)</li> <li>Error interrupt factor judge register (EIFR)</li> </ul>                                                                                     |
| Bit timing and communication speed settings             | Bit configuration register 0, 1 (BCR0, BCR1)                                      | Bit configuration register (BCR)                                                                                                                                                                                  |
| Mailbox transmission/reception settings                 | MBC[2:0] bit in message control field (CONTROL1)                                  | RECREQ and TRMREQ bits in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                        |
| Transmit wait settings                                  | Transmit pending register 0, 1 (TXPR0, TXPR1)                                     | TRMREQ bit in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                                    |
| Transmission completion status flags                    | Transmit acknowledge register 0, 1 (TXACK0, TXACK1)                               | SENTDATA bit in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                                  |
| Transmit wait cancel settings                           | Transmit cancel register 0, 1 (TXCR0, TXCR1)                                      | TRMREQ bit in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                                    |
| Transmit message cancellation completion status flags   | Abort acknowledge register 0, 1 (ABACK0, ABACK1)                                  | SENTDATA and TRMABT bits in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                      |
| Receive complete status flags                           | Data frame receive pending register 0, 1 (RXPR0, RXPR1)                           | NEWDATA bit in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                                   |
| Remote frame receive complete status flags              | Remote frame receive pending register 0, 1 (RFPR0, RFPR1)                         | —                                                                                                                                                                                                                 |
| Interrupt source status flags                           | Interrupt request register (IRR)<br>Note: Write 1 to clear a flag.                | <ul style="list-style-type: none"> <li>RECREQ and TRMREQ bits in message control register j (MCTLj) (j = 0 to 31)</li> <li>Error interrupt factor judge register (EIFR)</li> </ul> Note: Write 0 to clear a flag. |
| Mailbox (buffer) interrupt request enable/disable flags | Mailbox interrupt mask register 0, 1 (MBIMR0, MBIMR1)                             | Mailbox interrupt enable register (MIER)                                                                                                                                                                          |
| Interrupt source request enable/disable flags           | Interrupt mask register (IMR)                                                     | <ul style="list-style-type: none"> <li>Interrupt request enable register m (IERm)</li> <li>Error interrupt enable register (EIER)</li> </ul>                                                                      |
| Reception error counter                                 | Receive error counter (REC)                                                       | Receive error count register (RECR)                                                                                                                                                                               |
| Transmission error counter                              | Transmit error counter (TEC)                                                      | Transmit error count register (TECR)                                                                                                                                                                              |
| Overwrite status flags                                  | Unread message status register 0, 1 (UMSR0, UMSR1)                                | MSGLOST bit in message control register j (MCTLj) (j = 0 to 31)                                                                                                                                                   |
| Settings for filtering using receive message identifier | Local acceptance filter masks (LAFML and LAFMH) for mailbox (MB[N]) (N = 0 to 31) | <ul style="list-style-type: none"> <li>Mask register k (MKRk) (k = 0 to 7)</li> <li>Mask invalid register (MKIVLR)</li> </ul>                                                                                     |

| Item                                           | H8SX/1720S (RCAN-TL1)                                     | RX65N (CAN)                                                                                                                                     |
|------------------------------------------------|-----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| Mailboxes                                      | Mailbox (MB[N]) (N = 0 to 31)                             | Mailbox register j (MBj)<br>(j = 0 to 31)                                                                                                       |
| Module stop control                            | Module stop control register E (MSTPCRE)                  | Module stop control register B (MSTPCRB)<br>Note: Settings must be made to the protect register (PRCR) before making settings to this register. |
| FIFO received ID compare settings              | —                                                         | FIFO received ID compare registers 0 and 1 (FIDCR0 and FIDCR1)                                                                                  |
| Receive FIFO enable/disable settings           | —                                                         | Receive FIFO control register (RFCR)                                                                                                            |
| Receive FIFO pointer control settings          | —                                                         | Receive FIFO pointer control register (RFPCR)                                                                                                   |
| Transmit FIFO control settings                 | —                                                         | Transmit FIFO control register (TFCR)                                                                                                           |
| Mailbox search mode settings                   | —                                                         | Mailbox search mode register (MSMR)                                                                                                             |
| Mailbox search status register                 | —                                                         | Mailbox search status register (MSSR)                                                                                                           |
| Channel search mode settings                   | —                                                         | Channel search support register (CSSR)                                                                                                          |
| Multiple received ID masking function support  | —                                                         | Acceptance filter support register (AFSR)                                                                                                       |
| CAN bus error monitoring                       | —                                                         | Error code store register (ECSR)                                                                                                                |
| CAN test mode control                          | TST[2:0] bit of master control register (MCR)             | Test control register (TCR)                                                                                                                     |
| Timer control                                  | Time trigger control register0 (TTCR0)                    | TSRC and TSPS[1:0] bits in control register (CTLR)<br>Note: Counter reset and prescaler selection only                                          |
| Timer status                                   | Timer status register (TSR)                               | —                                                                                                                                               |
| Timer counter                                  | Timer counter register (TCNTR)                            | Time stamp register (TSR)                                                                                                                       |
| Cycle time                                     | Cycle time register (CYCTR)                               | —                                                                                                                                               |
| Timer counter at SOF of time reference message | Reference mark register (RFMK)                            | —                                                                                                                                               |
| Cycle counter for time trigger transmission    | Cycle counter register (CCR)                              | —                                                                                                                                               |
| Maximum value of cycle counter                 | Cycle maximum/Tx-Enable Window register (CMAX_TEW)        | —                                                                                                                                               |
| Offset setting for Tx-trigger time (TTT)       | Reference trigger offset register (RFTROFF)               | —                                                                                                                                               |
| Compare match with timer counter or cycle time | Timer compare match register 0 to 2 (TCMR0, TCMR1, TCMR2) | —                                                                                                                                               |
| Specify compare match with cycle counter       | Tx-trigger time selection register (TTTSEL)               | —                                                                                                                                               |

## 2.2 Control Register Details

Table 2.2 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Control Registers

| H8SX/1720S (RCAN-TL1)         |                             |                                                                                                                             | RX65N (CAN)             |                                       |                                                                                                                                                                                                                                                              |
|-------------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|-------------------------|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                        | Bit Name                    | Function                                                                                                                    | Symbol                  | Bit Name                              | Function                                                                                                                                                                                                                                                     |
| Master control register (MCR) |                             |                                                                                                                             | Control register (CTLR) |                                       |                                                                                                                                                                                                                                                              |
| MCR0                          | Reset request               | 0: Normal operating mode<br>1: Reset mode (initial value)                                                                   | CANM [1:0]              | CAN operating mode select bits        | 0 0: Normal operating mode<br>0 1: Reset mode (initial value)<br>1 0: Halt mode<br><b>1 1: Reset mode (forcible transition)</b><br><b>Note:</b><br><b>Forcible transition is a transition mode that does not wait for transmission to finish.</b>            |
| MCR1                          | Halt request                | 0: Normal operating mode (initial value)<br>1: Halt mode                                                                    |                         |                                       |                                                                                                                                                                                                                                                              |
| MCR2                          | Message transmission method | 0: Message ID priority (initial value)<br>1: Mailbox number priority (high-to-low)                                          | TPM                     | Transmission priority mode select bit | 0: Message ID priority (initial value)<br>1: Mailbox number priority                                                                                                                                                                                         |
| MCR5                          | Sleep mode                  | 0: Sleep mode released (initial value)<br>1: Sleep mode                                                                     | SLPM                    | CAN sleep mode bit                    | 0: Sleep mode released<br>1: Sleep mode (initial value)<br><b>Note:</b><br><b>Automatic transition to sleep mode after a hardware reset.</b>                                                                                                                 |
| MCR7                          | Auto-wake mode              | 0: Sleep mode release by CAN bus operation disabled (initial value)<br>1: Sleep mode release by CAN bus operation enabled   | —                       | —                                     | —                                                                                                                                                                                                                                                            |
| MCR6                          | Halt during bus off         | 0: Disables transition to halt mode during bus off (initial value)<br>1: Enables transition to halt mode during bus off     | BOM[1:0]                | Bus-off recovery mode bit             | 0 0: Normal operating mode (initial value)<br>0 1: Automatically switch to halt mode with bus-off entry<br><b>1 0: Automatically switch to halt mode with bus-off recovery</b><br><b>1 1: Can transition to halt mode before bus-off recovery by program</b> |
| MCR14                         | Auto halt bus off           | 0: Do not transition to halt mode during bus-off (initial value)<br>1: Transition to halt mode during bus-off when MCR6 = 1 |                         |                                       |                                                                                                                                                                                                                                                              |

| H8SX/1720S (RCAN-TL1)         |            |                                                                                                                                                                                                                                                                          | RX65N (CAN)                 |                           |                                                                                                                                                                                                                                  |
|-------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                        | Bit Name   | Function                                                                                                                                                                                                                                                                 | Symbol                      | Bit Name                  | Function                                                                                                                                                                                                                         |
| MCR15                         | ID reorder | 0: Sequence of mailbox control 0 and LAFM has same order as HCAN2<br>1: Sequence of message control in a mailbox has different order from HCAN2 (initial value)                                                                                                          | —                           | —                         | —                                                                                                                                                                                                                                |
| —                             | —          | —                                                                                                                                                                                                                                                                        | IDFM<br>[1:0]               | ID Format Mode Select bit | 0 0: Standard ID mode<br>0 1: Extended ID mode<br>1 0: Mixed ID mode<br>1 1: (setting prohibited)<br>Note:<br>When Mixed ID mode is selected in IDFM bit, specify standard ID or extended ID by the MBj.IDE bit of each mailbox. |
| Master control register (MCR) |            |                                                                                                                                                                                                                                                                          | Test control register (TCR) |                           |                                                                                                                                                                                                                                  |
| TST[2:0]                      | Test mode  | 0 0 0: Normal operating mode (initial value)<br>0 0 1: Listen-only mode<br>0 1 0: Self test mode 1 (external)<br>0 1 1: Self test mode 2 (internal)<br>1 0 0: Write error counter<br>1 0 1: Error passive mode<br>1 1 0: Setting prohibited<br>1 1 1: Setting prohibited | TSTM[1:0]                   | CAN test mode select bit  | 0 0: Other than test mode (initial value)<br>0 1: Listen-only mode<br>1 0: Self-test mode 0 (external loopback)<br>1 1: Self-test mode 1 (internal loopback)                                                                     |
| —                             | —          | —                                                                                                                                                                                                                                                                        | TSTE                        | CAN test mode enable bit  | 0: CAN test mode disabled<br>1: CAN test mode enabled                                                                                                                                                                            |

## 2.3 Status Flag Details

Table 2.3 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Status Flags

| H8SX/1720S (RCAN-TL1)         |                                       |                                                                                                                                         | RX65N (CAN)                                  |                                    |                                                                                                                                                                                                                                                                                                                                           |
|-------------------------------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                        | Bit Name                              | Function                                                                                                                                | Symbol                                       | Bit Name                           | Function                                                                                                                                                                                                                                                                                                                                  |
| General status register (GSR) |                                       |                                                                                                                                         | Error interrupt factor judge register (EIFR) |                                    |                                                                                                                                                                                                                                                                                                                                           |
| GSR0                          | Bus off flag                          | 0: Not in bus-off state (initial value)<br>1: Bus-off state (when TEC ≥ 256)<br><br>[Clearing condition]<br>Recovery from bus off state | BOEIF                                        | Bus-off entry detect flag          | 0: Not in bus-off state (initial value)<br>1: Bus-off state (when TEC ≥ 256)<br><br>[Clearing condition]<br>0 is written.                                                                                                                                                                                                                 |
| GSR1                          | Transmit/receive warning flag         | 0: Error warning not detected (initial value)<br>1: Error warning detected (when TEC ≥ 96 or REC ≥ 96)                                  | EWIF                                         | Error-warning detect flag          | 0: Error warning not detected (initial value)<br>1: Error warning detected (when TEC ≥ 96 or REC ≥ 96)                                                                                                                                                                                                                                    |
| General status register (GSR) |                                       |                                                                                                                                         | Status register (STR)                        |                                    |                                                                                                                                                                                                                                                                                                                                           |
| GSR2                          | Message transmission in progress flag | 0: Transmission in progress<br>1: Bus idle (initial value)                                                                              | TRMST                                        | Transmit status flag (transmitter) | 0: Bus idle or reception in progress (initial value)<br>1: Transmission in progress or bus-off state<br><br>Note:<br>The status can be checked by reading this bit in combination with RECST.<br>Bus idle:<br>TRMST = 0, RECST = 0<br>Transmission in progress:<br>TRMST = 1, RECST = 0<br>Reception in progress:<br>TRMST = 0, RECST = 1 |
|                               |                                       |                                                                                                                                         | RECST                                        | Receive status flag (receiver)     | 0: Bus idle or transmission in progress (initial value)<br>1: Reception in progress                                                                                                                                                                                                                                                       |
| GSR3                          | Reset status                          | 0: Normal operating state<br>1: Configuration mode (reset mode) (initial value)                                                         | RSTST                                        | CAN reset status flag              | 0: Not in CAN reset mode<br>1: CAN reset mode (initial value)                                                                                                                                                                                                                                                                             |

| H8SX/1720S (RCAN-TL1) |                      |                                                                         | RX65N (CAN) |                           |                                                                         |
|-----------------------|----------------------|-------------------------------------------------------------------------|-------------|---------------------------|-------------------------------------------------------------------------|
| Symbol                | Bit Name             | Function                                                                | Symbol      | Bit Name                  | Function                                                                |
| GSR4                  | Halt/sleep status    | 0: Not in halt mode or sleep mode (initial value)                       | HLTST       | CAN halt status flag      | 0: Not in CAN halt mode (initial value)<br>1: CAN halt mode             |
|                       |                      | 1: Halt mode or sleep mode                                              | SLPST       | CAN sleep status flag     | 0: Not in CAN sleep mode<br>1: CAN sleep mode (initial value)           |
| GSR5                  | Error passive status | 0: Not in error passive state (initial value)<br>1: Error passive state | EPST        | Error-passive status flag | 0: Not in error-passive state (initial value)<br>1: Error-passive state |

## 2.4 Bit Timing and Communication Speed Setting Details

Table 2.4 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Bit Timing and Communication Speed Settings

| H8SX/1720S (RCAN-TL1)               |                                           |                                                                                                                                                                                              | RX65N (CAN)                      |                                                      |                                                                                                                                                                                              |
|-------------------------------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                              | Bit Name                                  | Function                                                                                                                                                                                     | Symbol                           | Bit Name                                             | Function                                                                                                                                                                                     |
| Bit configuration register 1 (BCR1) |                                           |                                                                                                                                                                                              | Bit configuration register (BCR) |                                                      |                                                                                                                                                                                              |
| TSG1<br>[3:0]                       | Time segment 1<br>bits                    | b15 b12<br>0 0 0 0: (setting<br>prohibited)<br>(initial value)<br>0 0 0 1: (setting<br>prohibited)<br>0 0 1 0: (setting<br>prohibited)<br>0 0 1 1: 4Tq<br>0 1 0 0: 5Tq<br>:<br>1 1 1 1: 16Tq | TSEG1<br>[3:0]                   | Time segment 1<br>control bits                       | b31 b28<br>0 0 0 0: (setting<br>prohibited)<br>(initial value)<br>0 0 0 1: (setting<br>prohibited)<br>0 0 1 0: (setting<br>prohibited)<br>0 0 1 1: 4Tq<br>0 1 0 0: 5Tq<br>:<br>1 1 1 1: 16Tq |
| TSG2<br>[2:0]                       | Time segment 2<br>bits                    | b10 b8<br>0 0 0: (setting<br>prohibited)<br>(initial value)<br>0 0 1: 2Tq<br>:<br>1 1 1: 8Tq                                                                                                 | TSEG2<br>[2:0]                   | Time segment 2<br>control bits                       | b10 b8<br>0 0 0: (setting<br>prohibited)<br>(initial value)<br>0 0 1: 2Tq<br>:<br>1 1 1: 8Tq                                                                                                 |
| BSP                                 | Bit sample point<br>bit                   | 0: Bit sampling at<br>one point<br>(initial value)<br>1: Bit sampling at<br>three points                                                                                                     | —                                | —                                                    | —                                                                                                                                                                                            |
| SJW<br>[1:0]                        | Re-<br>Synchronization<br>jump width bits | b5 b4<br>0 0: 1Tq<br>(initial value)<br>0 1: 2Tq<br>1 0: 3Tq<br>1 1: 4Tq                                                                                                                     | SJW<br>[1:0]                     | Re-<br>synchronization<br>jump width<br>control bits | b13 b12<br>0 0: 1Tq<br>(initial value)<br>0 1: 2Tq<br>1 0: 3Tq<br>1 1: 4Tq                                                                                                                   |
| Bit configuration register 0 (BCR0) |                                           |                                                                                                                                                                                              | Bit configuration register (BCR) |                                                      |                                                                                                                                                                                              |
| BRP<br>[7:0]                        | Baud rate<br>prescaler bits               | Division ratio of $2 \times$<br>(setting value P + 1)<br>Note: The initial<br>value is 0 (division by<br>2)                                                                                  | BRP<br>[9:0]                     | Prescaler<br>division ratio<br>select bits           | Division ratio of<br>(setting value P + 1)<br>Note: The initial<br>value is 0 (division by<br>1)                                                                                             |

## 2.5 Mailbox Transmission/Reception Setting Details

**Table 2.5 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Mailbox Transmission/Reception Settings**

| H8SX/1720S (RCAN-TL1)                               |                               |                                                                                                                                                                                                                                    | RX65N (CAN)                                      |                              |                                                                                                                                                                                                                                            |
|-----------------------------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                                              | Bit Name                      | Function                                                                                                                                                                                                                           | Symbol                                           | Bit Name                     | Function                                                                                                                                                                                                                                   |
| Mailbox (MB[N]) (N = 0 to 31)                       |                               |                                                                                                                                                                                                                                    | Message control register j (MCTLj) (j = 0 to 31) |                              |                                                                                                                                                                                                                                            |
| MBC<br>[2:0]                                        | Mailbox configuration         | Refer to Table 2.6                                                                                                                                                                                                                 | TRMREQ                                           | Transmit mailbox request bit | 0: Not configured for transmission (initial value)<br>1: Configured as transmit mailbox<br>Note:<br>The transmission and reception configuration settings are separate.                                                                    |
|                                                     |                               |                                                                                                                                                                                                                                    | RECREQ                                           | Receive mailbox request bit  | 0: Not configured for reception (initial value)<br>1: Configured as receive mailbox<br>Note:<br>The transmission and reception configuration settings are separate.                                                                        |
| Transmission pending register 0, 1 (TXPR0, TXPR1)   |                               |                                                                                                                                                                                                                                    | Message control register j (MCTLj) (j = 0 to 31) |                              |                                                                                                                                                                                                                                            |
| TXPR0<br>[15:1]<br>TXPR1<br>[15:0]                  | Transmit wait register        | 0: Idle state (initial value)<br>1: Transmit wait<br>Notes:<br>Transmission starts when TXPR is set to 1.<br>The corresponding bit is cleared to 0 automatically after message transmission completion or cancellation completion. | TRMREQ                                           | Transmit mailbox request bit | 0: Not configured for transmission (initial value)<br>1: Configured as transmit mailbox<br>Notes:<br>Transmission starts when TRMREQ is set to 1.<br>The corresponding bit is not cleared to 0 even after message transmission completion. |
| Transmit acknowledge register 0, 1 (TXACK0, TXACK1) |                               |                                                                                                                                                                                                                                    | Message control register j (MCTLj) (j = 0 to 31) |                              |                                                                                                                                                                                                                                            |
| TXACK0<br>[15:1]<br>TXACK1<br>[15:0]                | Transmit acknowledge register | 0: Transmission in progress or no transmission (initial value)<br>1: Transmission complete<br><br>[Clearing condition]<br>1 is written.                                                                                            | SENTDATA                                         | Transmission complete flag   | 0: Transmission in progress or no transmission (initial value)<br>1: Transmission complete<br><br>[Clearing condition]<br>0 is written.                                                                                                    |

| H8SX/1720S (RCAN-TL1)                                     |                                       |                                                                                                                                                                                               | RX65N (CAN)                                      |                                  |                                                                                                                                                                                               |
|-----------------------------------------------------------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                                                    | Bit Name                              | Function                                                                                                                                                                                      | Symbol                                           | Bit Name                         | Function                                                                                                                                                                                      |
| Transmit cancel register 0, 1 (TXCR0, TXCR1)              |                                       |                                                                                                                                                                                               | Message control register j (MCTLj) (j = 0 to 31) |                                  |                                                                                                                                                                                               |
| TXCR0<br>[15:1]<br>TXCR1<br>[15:0]                        | Transmit cancel register              | 0: Transmit message cancellation idle state (initial value)<br>1: Transmit message canceled<br><br>[Clearing condition]<br>1 is written.                                                      | TRMREQ                                           | Transmit mailbox request bit     | 0: Not configured for transmission (initial value)<br>1: Configured as transmit mailbox<br>Note:<br>Transmission is canceled when the value of TRMREQ changes from 1 to 0.                    |
| Abort acknowledge register 0, 1 (ABACK0, ABACK1)          |                                       |                                                                                                                                                                                               | Message control register j (MCTLj) (j = 0 to 31) |                                  |                                                                                                                                                                                               |
| ABACK0<br>[15:1]<br>ABACK1<br>[15:0]                      | Abort acknowledge register            | 0: Cancellation failure due to transmission completion or no cancellation request (initial value)<br>1: Transmit message cancellation completion<br><br>[Clearing condition]<br>1 is written. | TRMABT                                           | Transmission abort complete flag | 0: Cancellation failure due to transmission completion or no cancellation request (initial value)<br>1: Transmit message cancellation completion<br><br>[Clearing condition]<br>0 is written. |
| Data frame receive pending register 0, 1 (RXPR0, RXPR1)   |                                       |                                                                                                                                                                                               | Message control register j (MCTLj) (j = 0 to 31) |                                  |                                                                                                                                                                                               |
| RXPR0<br>[15:0]<br>RXPR1<br>[15:0]                        | Data frame receive pending register   | 0: Reception in progress or no reception (initial value)<br>1: Data frame receive complete<br><br>[Clearing condition]<br>1 is written.                                                       | NEWDATA                                          | Reception complete flag          | 0: Reception in progress or no reception (initial value)<br>1: Data frame or remote frame receive complete<br><br>[Clearing condition]<br>0 is written.                                       |
| Remote frame receive pending register 0, 1 (RFPR0, RFPR1) |                                       |                                                                                                                                                                                               | —                                                |                                  |                                                                                                                                                                                               |
| RFPR0<br>[15:0]<br>RFPR1<br>[15:0]                        | Remote frame receive pending register | 0: Reception in progress or no reception (initial value)<br>1: Remote frame receive complete<br><br>[Clearing condition]<br>1 is written.                                                     | —                                                | —                                | —                                                                                                                                                                                             |

**Table 2.6 Mailbox Configuration (MBC[2:0]) Settings**

| <b>b2 b0</b> | <b>Data Frame Transmit/<br/>Remote Frame<br/>Transmit</b> | <b>Data Frame<br/>Receive</b> | <b>Remote Frame<br/>Receive</b> | <b>Remarks</b>                                                       |
|--------------|-----------------------------------------------------------|-------------------------------|---------------------------------|----------------------------------------------------------------------|
| 0 0 0        | Yes                                                       | No                            | No                              | Mailbox 0 cannot be used<br>Time-trigger transmission<br>can be used |
| 0 0 1        |                                                           | No                            | Yes                             | Can be used with ATX<br>Mailbox 0 cannot be used<br>LAFM can be used |
| 0 1 0        | No                                                        | Yes                           | Yes                             | Mailbox 0 can be used<br>LAFM can be used                            |
| 0 1 1        |                                                           | Yes                           | No                              | Mailbox 0 can be used<br>LAFM can be used                            |
| 1 0 0        | Setting prohibited                                        |                               |                                 |                                                                      |
| 1 0 1        |                                                           |                               |                                 |                                                                      |
| 1 1 0        |                                                           |                               |                                 |                                                                      |
| 1 1 1        | Mailbox inactive (initial value)                          |                               |                                 |                                                                      |

## 2.6 Interrupt Source Status Flag Details

Table 2.7 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Interrupt Source Status Flags

| H8SX/1720S (RCAN-TL1)            |                                     |                                                                                                                                                                                                                                                                        | RX65N (CAN)                                      |                            |                                                                                                                                                                 |
|----------------------------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                           | Bit Name                            | Function                                                                                                                                                                                                                                                               | Symbol                                           | Bit Name                   | Function                                                                                                                                                        |
| Interrupt request register (IRR) |                                     |                                                                                                                                                                                                                                                                        | Message control register j (MCTLj) (j = 0 to 31) |                            |                                                                                                                                                                 |
| IRR8                             | Mailbox empty interrupt flag        | 0: Transmission in progress or no transmission (initial value)<br>1: Transmission complete or transmission cancellation complete<br><br>[Clearing condition]<br>When all transmit acknowledge register (TXACK) and abort acknowledge register (ABACK) bits are cleared | SENTDATA                                         | Transmission complete flag | 0: Transmission in progress or no transmission (initial value)<br>1: Transmission complete<br><br>[Clearing condition]<br><b>0 is written.</b>                  |
| IRR1                             | Data frame received interrupt flag  | 0: Reception in progress or no reception (initial value)<br>1: Data frame receive complete<br><br>[Clearing condition]<br>When all data frame receive pending register (RXPR) bits for mailboxes are cleared                                                           | NEWDATA                                          | Reception complete flag    | 0: Reception in progress or no reception (initial value)<br>1: Data frame and remote frame receive complete<br><br>[Clearing condition]<br><b>0 is written.</b> |
| IRR2                             | Remote frame receive interrupt flag | 0: Reception in progress or no reception (initial value)<br>1: Remote frame receive complete<br><br>[Clearing condition]<br>When all mailbox bits in remote request register (RFPR) are cleared                                                                        |                                                  |                            |                                                                                                                                                                 |

| H8SX/1720S (RCAN-TL1)    |                                               |                                                                                                                                                                   | RX65N (CAN)                                  |                           |                                                                                                                                                                          |
|--------------------------|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                   | Bit Name                                      | Function                                                                                                                                                          | Symbol                                       | Bit Name                  | Function                                                                                                                                                                 |
| IRR12                    | Bus activity while in sleep mode              | 0: CAN bus idle state (initial value)<br>1: CAN bus operation in CAN sleep mode<br><br>[Clearing condition]<br>1 is written.                                      | —                                            | —                         | —                                                                                                                                                                        |
| Interrupt register (IRR) |                                               |                                                                                                                                                                   | Error interrupt factor judge register (EIFR) |                           |                                                                                                                                                                          |
| IRR3                     | Transmit error counter warning interrupt flag | 0: Error warning not detected (initial value)<br>1: Error warning detected (when TEC ≥ 96)<br><br>[Clearing condition]<br>1 is written.                           | EWIF                                         | Error-warning detect flag | 0: Error warning not detected (initial value)<br>1: Error warning detected (when TEC ≥ 96 or REC ≥ 96)<br><br>[Clearing condition]<br><b>0 is written.</b>               |
| IRR4                     | Receive error counter warning interrupt flag  | 0: Error warning not detected (initial value)<br>1: Error warning detected (when REC ≥ 96)<br><br>[Clearing condition]<br>1 is written.                           |                                              |                           |                                                                                                                                                                          |
| IRR5                     | Error passive interrupt flag                  | 0: Error passive state not detected (initial value)<br>1: Error passive state detected (when TEC ≥ 128 or REC ≥ 128)<br><br>[Clearing condition]<br>1 is written. | EPIF                                         | Error-passive detect flag | 0: Error passive state not detected (initial value)<br>1: Error passive state detected (when TEC ≥ 128 or REC ≥ 128)<br><br>[Clearing condition]<br><b>0 is written.</b> |
| IRR6                     | Bus off interrupt flag                        | 0: Not in bus-off state (initial value)<br>1: Bus-off state (when TEC ≥ 256)<br><br>[Clearing condition]<br>1 is written.                                         | BOEIF                                        | Bus-off entry detect flag | 0: Not in bus-off state (initial value)<br>1: Bus-off state (when TEC ≥ 256)<br><br>[Clearing condition]<br><b>0 is written.</b>                                         |

| H8SX/1720S (RCAN-TL1) |                                          |                                                                                                                                                                                                                                                                                             | RX65N (CAN) |                                         |                                                                                                                                                                                                                                     |
|-----------------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                | Bit Name                                 | Function                                                                                                                                                                                                                                                                                    | Symbol      | Bit Name                                | Function                                                                                                                                                                                                                            |
| IRR7                  | Overload frame                           | 0: Overload frame transmission not detected (initial value)<br>1: Overload frame transmission detected<br><br>[Clearing condition]<br>1 is written.                                                                                                                                         | OLIF        | Overload frame transmission detect flag | 0: Overload frame transmission not detected (initial value)<br>1: Overload frame transmission detected<br><br>[Clearing condition]<br><b>0 is written.</b>                                                                          |
| IRR9                  | Message overrun/overwrite interrupt flag | 0: No overrun/overwrite (initial value)<br>1: Discard received message/unread message overwrite<br><br>[Clearing condition]<br>All unread message status register (UMSR) bits are cleared or the mailbox interrupt mask registers (MBIMR) are set that correspond to all UMSR that were set | ORIF        | Receive overrun detect flag             | 0: Receive overrun not detected (initial value)<br>1: Receive overrun detected<br><br>[Clearing condition]<br><b>0 is written.</b><br><br><b>Note:</b><br><b>Becomes 1 only by an overrun. Will not become 1 in overwrite mode.</b> |
| IRR10                 | Start of new system matrix interrupt     | 0: A system matrix is not starting<br>1: Time reference message transmission/receive complete<br><br>[Clearing condition]<br>1 is written.                                                                                                                                                  | —           | —                                       | —                                                                                                                                                                                                                                   |
| IRR11                 | Timer compare match interrupt 2          | 0: TCMR2 timer compare match has not occurred<br>1: TCMR2 timer compare match has occurred (TCMR2 = CYCTR)<br><br>[Clearing condition]<br>1 is written.                                                                                                                                     | —           | —                                       | —                                                                                                                                                                                                                                   |

| H8SX/1720S (RCAN-TL1) |                                                                                 |                                                                                                                                                                                                                                          | RX65N (CAN) |          |          |
|-----------------------|---------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|----------|----------|
| Symbol                | Bit Name                                                                        | Function                                                                                                                                                                                                                                 | Symbol      | Bit Name | Function |
| IRR13                 | Timer overrun interrupt/Next_is_Gap reception interrupt/message error interrupt | 0: Nothing has occurred<br>1: Timer overrun has occurred in event trigger mode, a Next_is_Gap reference message was received in time trigger mode, or a message error occurred in test mode<br><br>[Clearing condition]<br>1 is written. | —           | —        | —        |
| IRR14                 | Timer compare match interrupt 0                                                 | 0: TCMR0 timer compare match has not occurred<br>1: TCMR0 timer compare match has occurred (TCMR0 = TCNTR)<br><br>[Clearing condition]<br>1 is written.                                                                                  | —           | —        | —        |
| IRR15                 | Timer compare match interrupt 1                                                 | 0: TCMR1 timer compare match has not occurred<br>1: TCMR1 timer compare match has occurred (TCMR1 = CYCTR)<br><br>[Clearing condition]<br>1 is written.                                                                                  | —           | —        | —        |
| IRR0                  | Reset/halt/sleep interrupt flag                                                 | 0: No mode transition<br>1: Transition to reset mode, transition to halt mode, or transition to sleep mode<br><br>[Clearing condition]<br>1 is written.                                                                                  | —           | —        | —        |

**2.7 Interrupt Source Request Enable/Disable Flag Details****Table 2.8 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Interrupt Source Request Enable/Disable Flags**

| H8SX/1720S (RCAN-TL1)         |                                                                                      |                                                                               | RX65N (CAN) |          |          |
|-------------------------------|--------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------|----------|----------|
| Symbol                        | Bit Name                                                                             | Function                                                                      | Symbol      | Bit Name | Function |
| Interrupt mask register (IMR) |                                                                                      |                                                                               | —           |          |          |
| IMR8                          | Mailbox empty interrupt mask                                                         | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR1                          | Data frame received interrupt mask                                                   | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR2                          | Remote frame receive interrupt mask                                                  | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR12                         | Bus activity while in sleep mode mask                                                | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR10                         | Start of new system matrix interrupt mask                                            | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR11                         | Timer compare match interrupt 2 mask                                                 | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR13                         | Timer overrun interrupt/Next_is_Gap reception interrupt/message error interrupt mask | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR14                         | Timer compare match interrupt 0 mask                                                 | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |
| IMR15                         | Timer compare match interrupt 1 mask                                                 | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —           | —        | —        |

| H8SX/1720S (RCAN-TL1)                                 |                                               |                                                                               | RX65N (CAN)                              |                                              |                                                                               |
|-------------------------------------------------------|-----------------------------------------------|-------------------------------------------------------------------------------|------------------------------------------|----------------------------------------------|-------------------------------------------------------------------------------|
| Symbol                                                | Bit Name                                      | Function                                                                      | Symbol                                   | Bit Name                                     | Function                                                                      |
| IMR0                                                  | Reset/halt/sleep interrupt mask               | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | —                                        | —                                            | —                                                                             |
| Interrupt mask register (IMR)                         |                                               |                                                                               | Error interrupt enable register (EIER)   |                                              |                                                                               |
| IMR3                                                  | Transmit error counter warning interrupt mask | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | EWIE                                     | Error-warning interrupt enable bit           | 0: Interrupt request disabled (initial value)<br>1: Interrupt request enabled |
| IMR4                                                  | Receive error counter warning interrupt mask  | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) |                                          |                                              |                                                                               |
| IMR5                                                  | Error passive interrupt mask                  | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | EPIE                                     | Error-passive interrupt enable bit           | 0: Interrupt request disabled (initial value)<br>1: Interrupt request enabled |
| IMR6                                                  | Bus off interrupt mask                        | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | BOEIE                                    | Bus-off entry interrupt enable bit           | 0: Interrupt request disabled (initial value)<br>1: Interrupt request enabled |
| IMR7                                                  | Overload frame mask                           | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | OLIE                                     | Overload frame transmit interrupt enable bit | 0: Interrupt request disabled (initial value)<br>1: Interrupt request enabled |
| IMR9                                                  | Message overrun/overwrite interrupt mask      | 0: Interrupt request enabled<br>1: Interrupt request disabled (initial value) | ORIE                                     | Overrun interrupt enable bit                 | 0: Interrupt request disabled (initial value)<br>1: Interrupt request enabled |
| Mailbox interrupt mask register 0, 1 (MBIMR0, MBIMR1) |                                               |                                                                               | Mailbox interrupt enable register (MIER) |                                              |                                                                               |
| MBIMR0 [15:0]<br>MBIMR1 [15:0]                        | Mailbox interrupt mask                        | 0: Interrupt enabled<br>1: Interrupt disabled (initial value)                 | MB [31:0]                                | Interrupt enable bits                        | 0: Interrupt disabled (initial value)<br>1: Interrupt enabled                 |

The interrupt controller specifications differ on the H8SX/1720S Group and RX65N Group. To control generation of interrupts on the RX65N Group it is necessary to make enable/disable settings for each interrupt in the interrupt controller. For details of the interrupt controller, refer to RX65N Group, RX651 Group User's Manual: Hardware (R01UH0590).

The CAN interrupts on the RX65N Group are listed below.

[Software configurable interrupt B]

CANi reception complete interrupt (mailboxes 0 to 31) [RXMi]

CANi transmission complete interrupt (mailboxes 0 to 31) [TXMi]

CANi receive FIFO interrupt [RXFi]

CANi transmit FIFO interrupt [TXFi]

[Group BE0 interrupts]

CANi error interrupts [ERSi] (error interrupt sources)

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock

**2.8 Details of Settings for Filtering Using Receive Message Identifier****Table 2.9 H8SX/1720S (RCAN-TL1) and RX65N (CAN) Settings for Filtering Using Receive Message Identifier**

| H8SX/1720S (RCAN-TL1)                           |                                                       |                                                                                                                        | RX65N (CAN)                         |                   |                                                                                                                                                                                         |
|-------------------------------------------------|-------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------------------------------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Symbol                                          | Bit Name                                              | Function                                                                                                               | Symbol                              | Bit Name          | Function                                                                                                                                                                                |
| Local acceptance filter masks (LAFML and LAFMH) |                                                       |                                                                                                                        | Mask register k (MKRk) (k = 0 to 7) |                   |                                                                                                                                                                                         |
| STDID_LAFM [10:0]                               | Filter mask bits for the CAN base identifier bits     | 0: Corresponding bits are compared<br>1: Corresponding bits are not compared<br>Note:<br>Initial values are undefined. | SID[10:0]                           | Standard ID bits  | 0: Corresponding bits are not compared<br>1: Corresponding bits are compared<br>Notes:<br>The bit functions are the opposite of those on the RCAN-TL1.<br>Initial values are undefined. |
| EXTID_LAFM [17:16]<br>EXTID_LAFM [15:0]         | Filter mask bits for the CAN Extended identifier bits | 0: Corresponding bits are compared<br>1: Corresponding bits are not compared<br>Note:<br>Initial values are undefined. | EID[17:0]                           | Extended ID bits  | 0: Corresponding bits are not compared<br>1: Corresponding bits are compared<br>Notes:<br>The bit functions are the opposite of those on the RCAN-TL1.<br>Initial values are undefined. |
| IDE_LAFM                                        | Filter mask bit for the CAN IDE bit                   | 0: Corresponding IDE bits are valid<br>1: Corresponding IDE bits are invalid<br>Note:<br>Initial values are undefined. | —                                   | —                 | —                                                                                                                                                                                       |
| —                                               | —                                                     | —                                                                                                                      | Mask invalid register (MKIVLR)      |                   |                                                                                                                                                                                         |
| —                                               | —                                                     | —                                                                                                                      | MB[31:0]                            | Mask invalid bits | 0: Mask valid for corresponding mailbox<br>1: Mask invalid for corresponding mailbox<br>Note:<br>Initial values are undefined.                                                          |

## 2.9 Timer Control/Time Trigger Details

Table 2.10 Details on H8SX/1720S (RCAN-TL1) and RX65N (CAN) Time Stamps and Time Triggers

| H8SX/1720S (RCAN-TL1)                  |                                  |                                                                                                                                                                                          | RX65N (CAN)             |                                  |                                                                                                                    |
|----------------------------------------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------|
| Symbol                                 | Bit Name                         | Function                                                                                                                                                                                 | Symbol                  | Bit Name                         | Function                                                                                                           |
| Time trigger control register0 (TTCR0) |                                  |                                                                                                                                                                                          | Control register (CTLR) |                                  |                                                                                                                    |
| TCR15                                  | Enable Timer                     | 0: Clear the counter (TCNTR) and cycle counter (CCR) and stop counting<br>1: Start counting                                                                                              | —                       | —                                | Note: Start counting will transition to normal operating mode.<br>Stop will transition to sleep mode or halt mode. |
|                                        |                                  |                                                                                                                                                                                          | TSRC                    | Time stamp counter reset command |                                                                                                                    |
| TCR14                                  | TimeStamp value                  | 0: Use CYCTR for time stamp<br>1: Use CCR+CYCTR for time stamp                                                                                                                           | —                       | —                                | —                                                                                                                  |
| TCR13                                  | Cancellation by TCMR2            | 0: Transmission cancellation by compare match is disabled<br>1: Transmission cancellation by compare match is enabled                                                                    | —                       | —                                | —                                                                                                                  |
| TCR12                                  | TCMR2 compare match enable       | 0: Compare match disabled<br>1: Compare match enabled                                                                                                                                    | —                       | —                                | —                                                                                                                  |
| TCR11                                  | TCMR1 compare match enable       | 0: Compare match disabled<br>1: Compare match enabled                                                                                                                                    | —                       | —                                | —                                                                                                                  |
| TCR10                                  | TCMR0 compare match enable       | 0: Compare match disabled<br>1: Compare match enabled                                                                                                                                    | —                       | —                                | —                                                                                                                  |
| TCR6                                   | Timer clear-set control by TCMR0 | 0: Counting is not cleared by compare match<br>1: Counting is cleared by compare match                                                                                                   | —                       | —                                | —                                                                                                                  |
| TPSC5 to TPSC0                         | Timer prescaler                  | Division ratio of $2 \times (\text{setting value } P + 1)$<br>Notes: The initial value is 0 (division by 1)<br>Notes: Valid in event trigger mode<br>Fixed to 1-bit timing in TTCAN mode | TSPS[1:0]               | Time stamp prescaler select bits | b1b0<br>0 0: Every bit time<br>0 1: Every 2-bit time<br>1 0: Every 4-bit time<br>1 1: Every 8-bit time             |

### 3. Differences between Mailboxes

Table 3.1 shows the Mailbox Structure of RX65N (CAN), and Table 3.2 to Table 3.7 show the mailbox structure of H8SX/1720S (RCAN-TL1). Items that only exist on one group are indicated in **red**.

**Table 3.1 Mailbox Structure of RX65N (CAN)**

| Register Name        | b7        | b6  | b5 | b4        | b3       | b2 | b1         | b0 | Access Size*1 | Field      |
|----------------------|-----------|-----|----|-----------|----------|----|------------|----|---------------|------------|
| MBj<br>(j = 0 to 31) | IDE*2     | RTR | —  | SID[10:6] |          |    |            |    | 8/16/32       | Control    |
|                      | SID[5:0]  |     |    |           |          |    | EID[17:16] |    |               |            |
|                      | EID[15:8] |     |    |           |          |    |            |    |               |            |
|                      | EID[7:0]  |     |    |           |          |    |            |    |               |            |
|                      | —         | —   | —  | —         | —        | —  | —          | —  | 8/16/32       | Data       |
|                      | —         | —   | —  | —         | DLC[3:0] |    |            |    |               |            |
|                      | DATA0     |     |    |           |          |    |            |    |               |            |
|                      | DATA1     |     |    |           |          |    |            |    |               |            |
|                      | DATA2     |     |    |           |          |    |            |    | 8/16/32       |            |
|                      | DATA3     |     |    |           |          |    |            |    |               |            |
|                      | DATA4     |     |    |           |          |    |            |    |               |            |
|                      | DATA5     |     |    |           |          |    |            |    |               |            |
|                      | DATA6     |     |    |           |          |    |            |    | 8/16/32       | Time stamp |
|                      | DATA7     |     |    |           |          |    |            |    |               |            |
|                      | TSH       |     |    |           |          |    |            |    |               |            |
|                      | TSL       |     |    |           |          |    |            |    |               |            |

Note: 1. When accessing mailbox register j (MBj) (j = 0 to 31), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

Note: 2. The IDE bit is enabled when the IDFM bit in CTLR register are mixed ID mode (10b). Write the IDE bits with 0 when the IDFM bits are not 10b. The value is 0 when it is read.

**Table 3.2 Mailbox Structure of H8SX/1720S (RCAN-TL1) (MB0 for Reception)**

| Register Name   | b7               | b6  | b5  | b4               | b3       | b2       | b1                | b0 | Access Size*1 | Field      |
|-----------------|------------------|-----|-----|------------------|----------|----------|-------------------|----|---------------|------------|
| MB0             | IDE              | RTR | 0   | STDID[10:6]      |          |          |                   |    | 16/32         | Control 0  |
|                 | STDID[5:0]       |     |     |                  |          |          | EXTID[17:16]      |    |               |            |
|                 | EXTID[15:8]      |     |     |                  |          |          |                   |    |               |            |
|                 | EXTID[7:0]       |     |     |                  |          |          |                   |    |               |            |
|                 | IDE_LAFM         | 0   | 0   | STDID_LAFM[10:6] |          |          |                   |    | 16/32         | LAFM       |
|                 | STDID_LAFM[5:0]  |     |     |                  |          |          | EXTID_LAFM[17:16] |    |               |            |
|                 | EXTID_LAFM[15:8] |     |     |                  |          |          |                   |    |               |            |
|                 | EXTID_LAFM[7:0]  |     |     |                  |          |          |                   |    |               |            |
|                 | MSG_DATA_0       |     |     |                  |          |          |                   |    | 8/16/32       | Data       |
|                 | MSG_DATA_1       |     |     |                  |          |          |                   |    |               |            |
|                 | MSG_DATA_2       |     |     |                  |          |          |                   |    |               |            |
|                 | MSG_DATA_3       |     |     |                  |          |          |                   |    |               |            |
|                 | MSG_DATA_4       |     |     |                  |          |          |                   |    | 8/16/32       |            |
|                 | MSG_DATA_5       |     |     |                  |          |          |                   |    |               |            |
|                 | MSG_DATA_6       |     |     |                  |          |          |                   |    |               |            |
|                 | MSG_DATA_7       |     |     |                  |          |          |                   |    |               |            |
|                 | 0                | 0   | NMC | 0                | 0        | MBC[2:0] |                   |    | 8/16          | Control 1  |
|                 | 0                | 0   | 0   | 0                | DLC[3:0] |          |                   |    |               |            |
|                 | Time Stamp[15:8] |     |     |                  |          |          |                   |    | 16            | Time stamp |
| Time Stamp[7:0] |                  |     |     |                  |          |          |                   |    |               |            |

Note: 1. When accessing mailbox (MB0), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

**Table 3.3 Mailbox Structure of H8SX/1720S (RCAN-TL1) (MB1 to MB15)**

| Register Name        | b7               | b6  | b5  | b4               | b3   | b2       | b1                | b0 | Access Size*1 | Field     |
|----------------------|------------------|-----|-----|------------------|------|----------|-------------------|----|---------------|-----------|
| MBi<br>(i = 1 to 15) | IDE              | RTR | 0   | STDID[10:6]      |      |          |                   |    | 16/32         | Control 0 |
|                      | STDID[5:0]       |     |     |                  |      |          | EXTID[17:16]      |    |               |           |
|                      | EXTID[15:8]      |     |     |                  |      |          |                   |    |               |           |
|                      | EXTID[7:0]       |     |     |                  |      |          |                   |    |               |           |
|                      | IDE_LAFM         | 0   | 0   | STDID_LAFM[10:6] |      |          |                   |    | 16/32         | LAFM      |
|                      | STDID_LAFM[5:0]  |     |     |                  |      |          | EXTID_LAFM[17:16] |    |               |           |
|                      | EXTID_LAFM[15:8] |     |     |                  |      |          |                   |    |               |           |
|                      | EXTID_LAFM[7:0]  |     |     |                  |      |          |                   |    |               |           |
|                      | MSG_DATA_0       |     |     |                  |      |          |                   |    | 8/16/32       | Data      |
|                      | MSG_DATA_1       |     |     |                  |      |          |                   |    |               |           |
|                      | MSG_DATA_2       |     |     |                  |      |          |                   |    |               |           |
|                      | MSG_DATA_3       |     |     |                  |      |          |                   |    |               |           |
|                      | MSG_DATA_4       |     |     |                  |      |          |                   |    | 8/16/32       |           |
|                      | MSG_DATA_5       |     |     |                  |      |          |                   |    |               |           |
|                      | MSG_DATA_6       |     |     |                  |      |          |                   |    |               |           |
|                      | MSG_DATA_7       |     |     |                  |      |          |                   |    |               |           |
|                      | 0                | 0   | NMC | ATX              | DART | MBC[2:0] |                   |    | 8/16          | Control 1 |
| 0                    | 0                | 0   | 0   | DLC[3:0]         |      |          |                   |    |               |           |
| Time Stamp[15:8]     |                  |     |     |                  |      |          |                   | 16 | Time stamp    |           |
| Time Stamp[7:0]      |                  |     |     |                  |      |          |                   |    |               |           |

Note: 1. When accessing mailbox (MBi) (i = 1 to 15), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

**Table 3.4 Mailbox Structure of H8SX/1720S (RCAN-TL1) (MB16 to MB23)**

| Register Name         | b7               | b6  | b5  | b4               | b3       | b2       | b1                | b0 | Access Size*1 | Field     |
|-----------------------|------------------|-----|-----|------------------|----------|----------|-------------------|----|---------------|-----------|
| MBi<br>(i = 16 to 23) | IDE              | RTR | 0   | STDID[10:6]      |          |          |                   |    | 16/32         | Control 0 |
|                       | STDID[5:0]       |     |     |                  |          |          | EXTID[17:16]      |    |               |           |
|                       | EXTID[15:8]      |     |     |                  |          |          |                   |    |               |           |
|                       | EXTID[7:0]       |     |     |                  |          |          |                   |    |               |           |
|                       | IDE_LAFM         | 0   | 0   | STDID_LAFM[10:6] |          |          |                   |    | 16/32         | LAFM      |
|                       | STDID_LAFM[5:0]  |     |     |                  |          |          | EXTID_LAFM[17:16] |    |               |           |
|                       | EXTID_LAFM[15:8] |     |     |                  |          |          |                   |    |               |           |
|                       | EXTID_LAFM[7:0]  |     |     |                  |          |          |                   |    |               |           |
|                       | MSG_DATA_0       |     |     |                  |          |          |                   |    | 8/16/32       | Data      |
|                       | MSG_DATA_1       |     |     |                  |          |          |                   |    |               |           |
|                       | MSG_DATA_2       |     |     |                  |          |          |                   |    |               |           |
|                       | MSG_DATA_3       |     |     |                  |          |          |                   |    |               |           |
|                       | MSG_DATA_4       |     |     |                  |          |          |                   |    | 8/16/32       |           |
|                       | MSG_DATA_5       |     |     |                  |          |          |                   |    |               |           |
|                       | MSG_DATA_6       |     |     |                  |          |          |                   |    |               |           |
|                       | MSG_DATA_7       |     |     |                  |          |          |                   |    |               |           |
|                       | 0                | 0   | NMC | ATX              | DART     | MBC[2:0] |                   |    | 8/16          | Control 1 |
|                       | 0                | 0   | 0   | 0                | DLC[3:0] |          |                   |    |               |           |

Note: 1. When accessing mailbox (MBi) (i = 16 to 23), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

Table 3.5 Mailbox Structure of H8SX/1720S (RCAN-TL1) (MB24 to MB29)

| Register Name         | b7                           | b6  | b5     | b4               | b3       | b2         | b1                | b0 | Access Size*1 | Field        |
|-----------------------|------------------------------|-----|--------|------------------|----------|------------|-------------------|----|---------------|--------------|
| MBi<br>(i = 24 to 29) | IDE                          | RTR | 0      | STDID[10:6]      |          |            |                   |    | 16/32         | Control 0    |
|                       | STDID[5:0]                   |     |        |                  |          |            | EXTID[17:16]      |    |               |              |
|                       | EXTID[15:8]                  |     |        |                  |          |            |                   |    |               |              |
|                       | EXTID[7:0]                   |     |        |                  |          |            |                   |    |               |              |
|                       | IDE_LAFM                     | 0   | 0      | STDID_LAFM[10:6] |          |            |                   |    | 16/32         | LAFM         |
|                       | STDID_LAFM[5:0]              |     |        |                  |          |            | EXTID_LAFM[17:16] |    |               |              |
|                       | EXTID_LAFM[15:8]             |     |        |                  |          |            |                   |    |               |              |
|                       | EXTID_LAFM[7:0]              |     |        |                  |          |            |                   |    |               |              |
|                       | MSG_DATA_0                   |     |        |                  |          |            |                   |    | 8/16/32       | Data         |
|                       | MSG_DATA_1                   |     |        |                  |          |            |                   |    |               |              |
|                       | MSG_DATA_2                   |     |        |                  |          |            |                   |    |               |              |
|                       | MSG_DATA_3                   |     |        |                  |          |            |                   |    |               |              |
|                       | MSG_DATA_4                   |     |        |                  |          |            |                   |    | 8/16/32       |              |
|                       | MSG_DATA_5                   |     |        |                  |          |            |                   |    |               |              |
|                       | MSG_DATA_6                   |     |        |                  |          |            |                   |    |               |              |
|                       | MSG_DATA_7                   |     |        |                  |          |            |                   |    |               |              |
|                       | 0                            | 0   | NMC    | ATX              | DART     | MBC[2:0]   |                   |    | 8/16          | Control 1    |
|                       | 0                            | 0   | 0      | 0                | DLC[3:0] |            |                   |    |               |              |
|                       | Reserved                     |     |        |                  |          |            |                   |    | —             | —            |
|                       | Reserved                     |     |        |                  |          |            |                   |    |               |              |
|                       | Tx-trigger time (TTT) [15:8] |     |        |                  |          |            |                   |    | 16            | Trigger time |
|                       | Tx-trigger time (TTT) [7:0]  |     |        |                  |          |            |                   |    |               |              |
|                       | TTW[1:0]                     |     | Offset |                  |          |            |                   |    | 16            | TT control   |
|                       | 0                            | 0   | 0      | 0                | 0        | Rep_Factor |                   |    |               |              |

Note: 1. When accessing mailbox (MBi) (i = 24 to 29), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

**Table 3.6 Mailbox Structure of H8SX/1720S (RCAN-TL1) (MB30)**

| Register Name | b7                                             | b6  | b5  | b4               | b3       | b2       | b1                | b0 | Access Size*1 | Field        |
|---------------|------------------------------------------------|-----|-----|------------------|----------|----------|-------------------|----|---------------|--------------|
| MB30          | IDE                                            | RTR | 0   | STDID[10:6]      |          |          |                   |    | 16/32         | Control 0    |
|               | STDID[5:0]                                     |     |     |                  |          |          | EXTID[17:16]      |    |               |              |
|               | EXTID[15:8]                                    |     |     |                  |          |          |                   |    |               |              |
|               | EXTID[7:0]                                     |     |     |                  |          |          |                   |    |               |              |
|               | IDE_LAFM                                       | 0   | 0   | STDID_LAFM[10:6] |          |          |                   |    | 16/32         | LAFM         |
|               | STDID_LAFM[5:0]                                |     |     |                  |          |          | EXTID_LAFM[17:16] |    |               |              |
|               | EXTID_LAFM[15:8]                               |     |     |                  |          |          |                   |    |               |              |
|               | EXTID_LAFM[7:0]                                |     |     |                  |          |          |                   |    |               |              |
|               | MSG_DATA_0                                     |     |     |                  |          |          |                   |    | 8/16/32       | Data         |
|               | MSG_DATA_1                                     |     |     |                  |          |          |                   |    |               |              |
|               | MSG_DATA_2                                     |     |     |                  |          |          |                   |    |               |              |
|               | MSG_DATA_3                                     |     |     |                  |          |          |                   |    |               |              |
|               | MSG_DATA_4                                     |     |     |                  |          |          |                   |    | 8/16/32       |              |
|               | MSG_DATA_5                                     |     |     |                  |          |          |                   |    |               |              |
|               | MSG_DATA_6                                     |     |     |                  |          |          |                   |    |               |              |
|               | MSG_DATA_7                                     |     |     |                  |          |          |                   |    |               |              |
|               | 0                                              | 0   | NMC | ATX              | DART     | MBC[2:0] |                   |    | 8/16          | Control 1    |
|               | 0                                              | 0   | 0   | 0                | DLC[3:0] |          |                   |    |               |              |
|               | Time Stamp [15:8] (TCNTR value at SOF)         |     |     |                  |          |          |                   |    | 16            | Time stamp   |
|               | Time Stamp [7:0] (TCNTR value at SOF)          |     |     |                  |          |          |                   |    |               |              |
|               | Tx-trigger time (TTT) as time reference [15:8] |     |     |                  |          |          |                   |    | 16            | Trigger time |
|               | Tx-trigger time (TTT) as time reference [7:0]  |     |     |                  |          |          |                   |    |               |              |

Note: 1. When accessing mailbox (MB30), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

**Table 3.7 Mailbox Structure of H8SX/1720S (RCAN-TL1) (MB31)**

| Register Name                          | b7               | b6  | b5  | b4               | b3   | b2       | b1                | b0 | Access Size*1 | Field     |
|----------------------------------------|------------------|-----|-----|------------------|------|----------|-------------------|----|---------------|-----------|
| MB31                                   | IDE              | RTR | 0   | STDID[10:6]      |      |          |                   |    | 16/32         | Control 0 |
|                                        | STDID[5:0]       |     |     |                  |      |          | EXTID[17:16]      |    |               |           |
|                                        | EXTID[15:8]      |     |     |                  |      |          |                   |    |               |           |
|                                        | EXTID[7:0]       |     |     |                  |      |          |                   |    |               |           |
|                                        | IDE_LAFM         | 0   | 0   | STDID_LAFM[10:6] |      |          |                   |    | 16/32         | LAFM      |
|                                        | STDID_LAFM[5:0]  |     |     |                  |      |          | EXTID_LAFM[17:16] |    |               |           |
|                                        | EXTID_LAFM[15:8] |     |     |                  |      |          |                   |    |               |           |
|                                        | EXTID_LAFM[7:0]  |     |     |                  |      |          |                   |    |               |           |
|                                        | MSG_DATA_0       |     |     |                  |      |          |                   |    | 8/16/32       | Data      |
|                                        | MSG_DATA_1       |     |     |                  |      |          |                   |    |               |           |
|                                        | MSG_DATA_2       |     |     |                  |      |          |                   |    |               |           |
|                                        | MSG_DATA_3       |     |     |                  |      |          |                   |    |               |           |
|                                        | MSG_DATA_4       |     |     |                  |      |          |                   |    | 8/16/32       |           |
|                                        | MSG_DATA_5       |     |     |                  |      |          |                   |    |               |           |
|                                        | MSG_DATA_6       |     |     |                  |      |          |                   |    |               |           |
|                                        | MSG_DATA_7       |     |     |                  |      |          |                   |    |               |           |
|                                        | 0                | 0   | NMC | ATX              | DART | MBC[2:0] |                   |    | 8/16          | Control 1 |
| 0                                      | 0                | 0   | 0   | DLC[3:0]         |      |          |                   |    |               |           |
| Time Stamp [15:8] (TCNTR value at SOF) |                  |     |     |                  |      |          |                   | 16 | Time stamp    |           |
| Time Stamp [7:0] (TCNTR value at SOF)  |                  |     |     |                  |      |          |                   |    |               |           |

Note: 1. When accessing mailbox (MB31), access even addresses for 16-bit access and access addresses ending in 0h, 4h, 8h, or Ch for 32-bit access.

## 4. Other Differences

### 4.1 Sleep Mode Setting Procedure

The procedures for entering and clearing sleep mode differ between the H8SX/1720S (RCAN-TL1) and RX65N (CAN). The sleep mode setting procedure on each device is shown below. For more information on detailed differences, refer to the User's Manual: Hardware of each device.

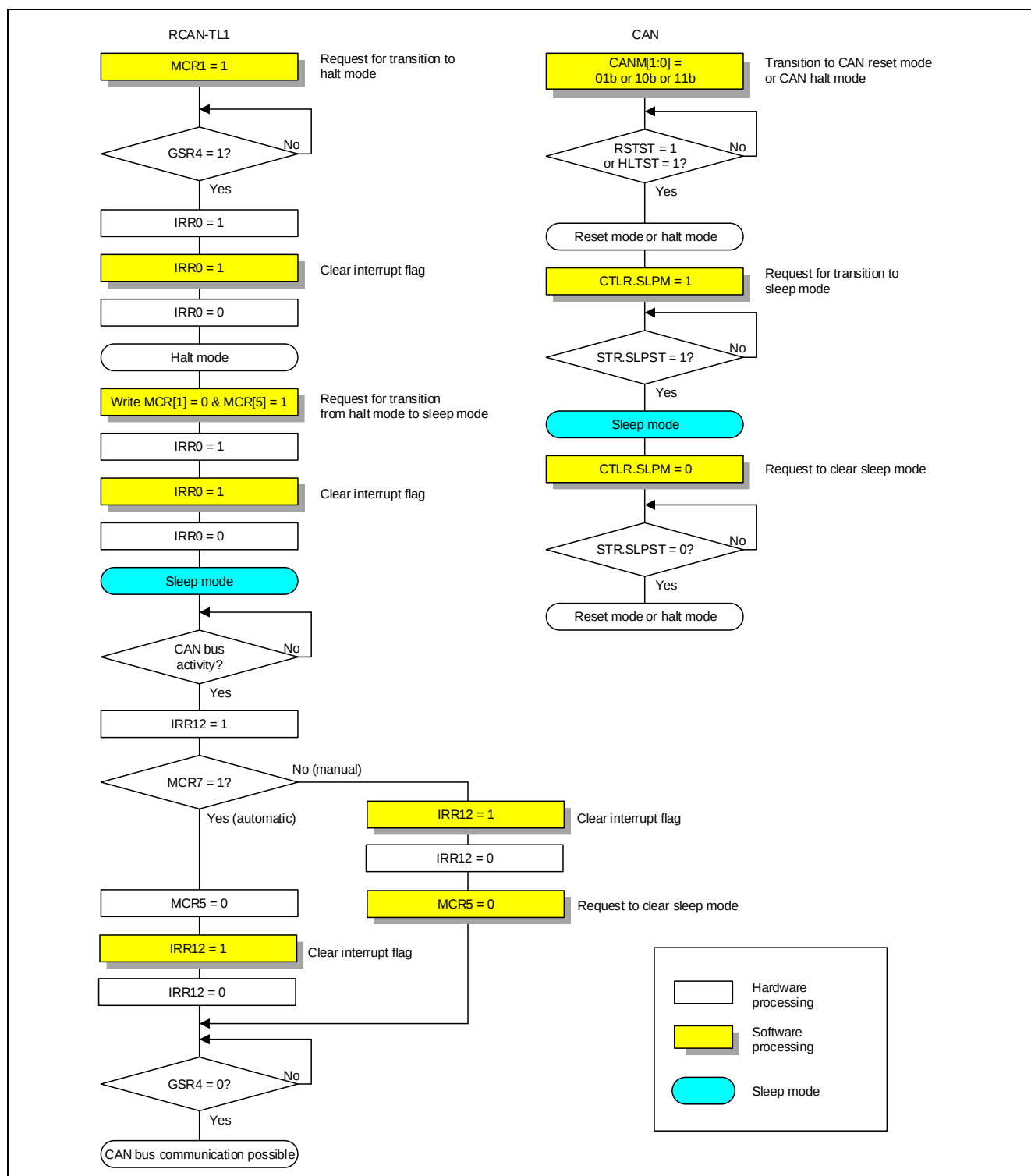


Figure 4.1 Sleep Mode Setting Procedure on H8SX/1720S (RCAN-TL1) and RX65N (CAN)

## 4.2 Initialization by CAN Reset

The register initialization operation and transition timing after a CAN software reset differ between the H8SX/1720S (RCAN-TL1) and RX65N (CAN). Table 4.1 lists the register initialization operation and transition timing differences between the two devices.

**Table 4.1 Register Initialization Operation and Transition Timing after CAN Software Reset**

| Item                    | H8SX/1720S (RCAN-TL1)                                                                   | RX65N (CAN)                                                                                                                                                                                                                                                               |
|-------------------------|-----------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Register initialization | All registers except MCR0 bit are initialized<br>(Except mailbox data allocated in RAM) | The following registers are initialized and the initialized state while in reset mode is retained:<br>MCTLj, STR (except SLPST and TFST flags), EIFR, RECR, TECR, TSR, MSSR, MSMR, RFCR, TFCR, TCR, and ECSR (except EDPM bit)                                            |
| Transition timing       | Transition to reset operation immediately after setting MCR0 bit to 1                   | After the CTLR.CANM[1:0] bits are set to 01b, transition occurs after message transmission finishes (without waiting for reception to complete).<br><br>[Forcible transition]<br>Transition to reset mode occurs immediately when the CTLR.CANM[1:0] bits are set to 11b. |

## 4.3 Endianness

The RX Family supports both littleendian and bigendian byte order. The H8SX Family supports bigendian byte order only.

For details of endian settings for the RX Family, refer to the User's Manual: Hardware of the specific RX Family device.

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## 5. Related Documents

Related documents are listed below. Consult them in conjunction with this application note.

### Application Notes

- RX Family Using the CAN (R01AN1448)
- RX65N/RX651 Group, RX230/RX231 Group Points of Difference Between RX65N Group and RX231 Group (R01AN3377)

### User's Manuals

- H8SX/1720S Group User's Manual: Hardware (R01UH0370)
- RX65N Group, RX651 Group User's Manual: Hardware (R01UH0590)

**Revision History**

| Rev. | Date      | Description |                      |
|------|-----------|-------------|----------------------|
|      |           | Page        | Summary              |
| 1.00 | Sep.30.19 | —           | First edition issued |
|      |           |             |                      |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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