RL78/I1D

Low Power Consuming Intermittent Operation Using DTC, ELC and SNOOZE Mode CC-RL

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Introduction

This application note describes the low power consuming intermittent operation achieved by using the DTC, ELC, and SNOOZE mode.

By using the DTC, ELC and transition to SNOOZE mode during STOP mode, the peripheral functions such as A/D converter are controlled without transition from STOP mode to normal operation.

Target Device

RL78/I1D

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application performs the following operations without returning from STOP mode to normal operation by using the DTC, ELC, and SNOOZE mode.

- Data processing:

  Illuminance or remaining battery level is checked using an A/D converter. The LED display data for illuminance or remaining battery level is generated using the obtained result of A/D conversion.

- LED display:

  LED display data is updated at fixed intervals using the 12-bit interval timer interrupt.

- Switch input:

  The target for A/D conversion and LED display is switched between remaining battery level and illuminance each time the switch is pressed.

1.1 Data Processing

Table 1.1 shows the peripheral functions used in data processing and their applications. Figure 1.1 shows an overview of the operations. Figure 1.2 illustrates the operation timing.

Table 1.1 Peripheral Functions and Applications (Data Processing)

Peripheral Function	Application
8-bit interval timer 00	· Counts the periods for starting data processing. · Generates an interrupt request to activate the DTC. · Period: 500 ms The period can be changed to the period longer than four cycles of the 12-bit interval timer (536 µs typ.).
8-bit interval timer 01	· Used as a hardware trigger signal of the A/D converter. · Generates an interrupt request to activate the ELC. · Counting: 134 µs typ. (the maximum speed of the 8-bit interval timer 01)
A/D converter	· Converts the analog signal input level on the P03/ANI17 pin (illuminance) or the P02/ANI16 pin (remaining battery level). · Generates the LED (LED1 to LED5) display data using the A/D conversion result. · Generates an interrupt to activate the DTC. · A/D conversion time: 11.375 µs Can be changed in the range from 11.375 µs to 77.875 µs.
DTC	· Executes the following operations triggered by an interrupt request from the 8-bit interval timer 00 (8bit-IT00). 1-a. Stores the LED display data in the display data output variable. 1-b. Sets the + side reference voltage of the A/D converter. 1-c. Specifies the analog input channel of the A/D converter. 1-d. Waits 10 µs for stabilization. (DTC dummy transfer) 1-e. Enables operation of the A/D voltage comparator of the A/D converter. 1-f. Sets “use the SNOOZE mode function”. 1-g. Starts the count operation of the 8-bit interval timer 01. · Executes the following operations triggered by an A/D conversion end interrupt request. 2-a. Stops operation of the A/D voltage comparator of the A/D converter. 2-b. Sets the + side reference voltage of the A/D converter to AVDD. 2-c. Sets “do not use the SNOOZE mode function”. 2-d. Reads the A/D conversion result, and uses it to generate the address value A for the area where the LED (LED1 to LED5) display data is stored. 2-e. Disables the 8bit-IT00 interrupt to activate the DTC transfer. 2-f. Sets the address value A described above as the transfer source address of DTC control data 14. 2-g. Enables the 8bit-IT00 interrupt to activate the DTC transfer. 2-h. Stores the LED (LED6) display data in the display data storage variable. 2-i. Stops operation of the 8-bit interval timer 01. 2-j. Initializes the 8-bit interval timer 01 compare value.
ELC	· Sets the interrupt request from the 8-bit interval timer 01 as a hardware trigger of the A/D converter.

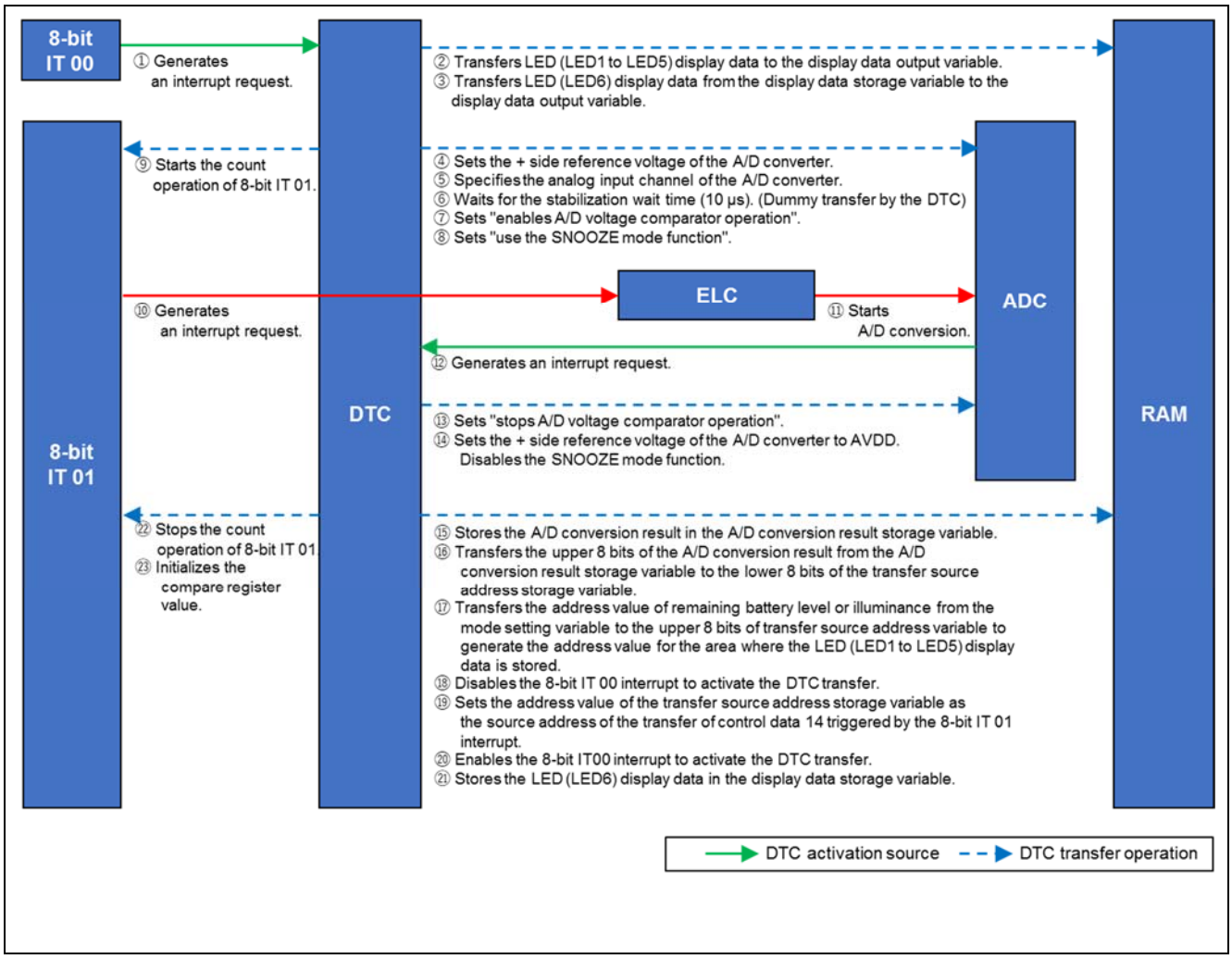


Figure 1.1 Overview of the Operation (Data Processing)

Note: 1. 12-bit IT and 8-bit IT in the above figure indicate the 12-bit and 8-bit interval timers, respectively.

2. A note of caution “Do not access the DTSARj register (DTC source address register j of the DTC) using a DTC transfer.” in RL78/I1D User’s Manual (Hardware) is provided to prevent an unintended DTC transfer. When it is necessary to access the DTSARj register using a DTC transfer, review the software and fully evaluate the system.

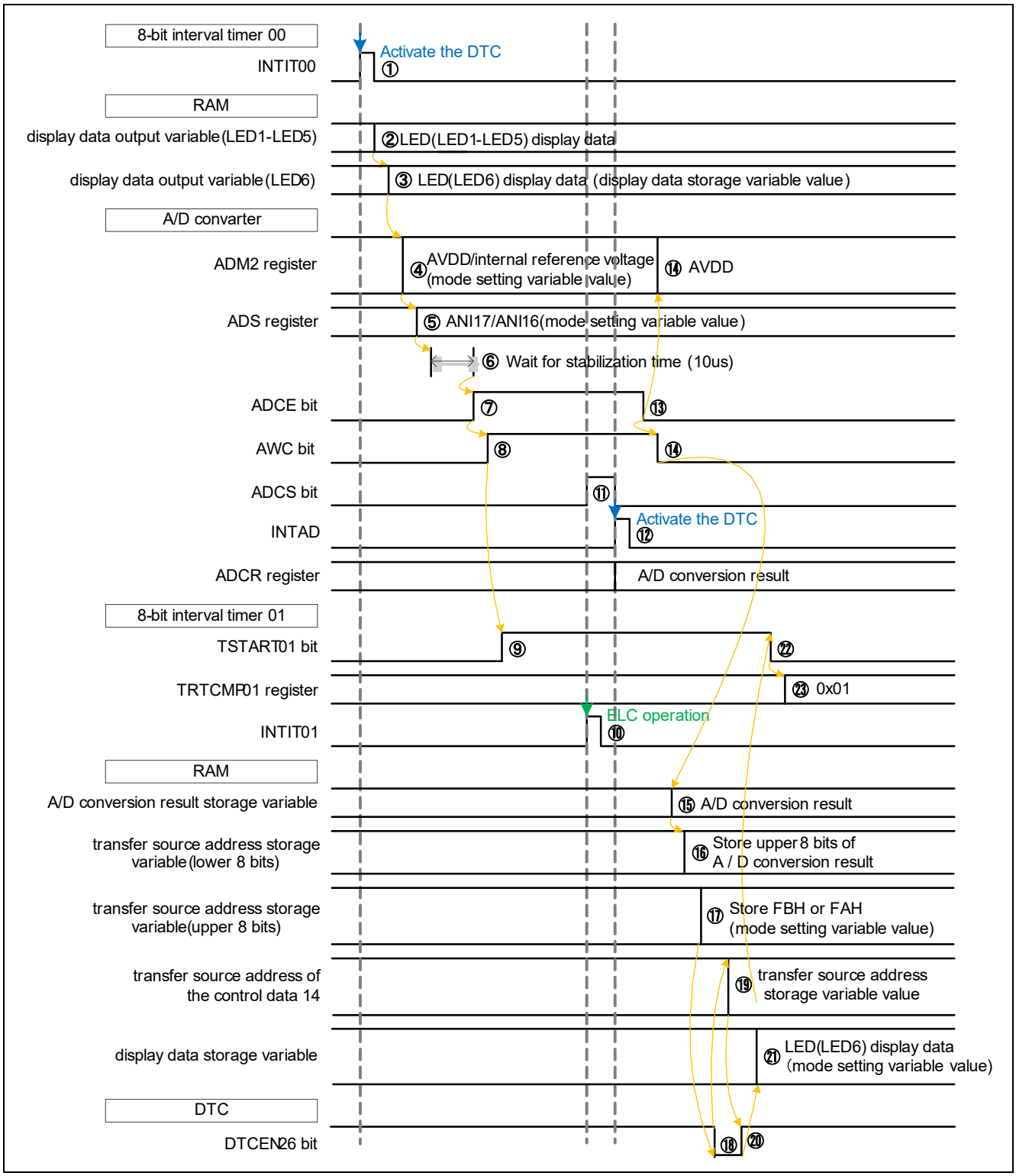


Figure 1.2 Operation Timing (Data Proessing)

Note: 1. The yellow arrows in the above figure indicate the chain transfer sequence of the DTC.

① The DTC is started by an interrupt request from the 8-bit interval timer 00.

② The LED (LED1 to LED5) display data is transferred using the DTC. The value stored in the address generated by the operations 16 and 17 below is transferred to the display data output variable.

③ By DTC chain transfer, the LED (LED6) display data in the display data storage variable is transferred and stored in the display data output variable.

④ By DTC chain transfer, the + side reference voltage of the A/D converter is set to AVDD (for measuring illuminance) or the internal reference voltage (for measuring remaining battery level) by transferring the value of the mode setting variable.

⑤ By DTC chain transfer, the analog input channel of the A/D converter is set to ANI17 (illuminance) or ANI16 (remaining battery level) by transferring the value of the mode setting variable.

⑥ Dummy transfer (from RAM area to RAM area) is performed several times by DTC chain transfer to provide the time (10 μs) for stabilization of the + side reference voltage of the A/D converter.

⑦ By DTC chain transfer, set "enables A/D voltage comparator operation".

⑧ By DTC chain transfer, set "use the SNOOZE mode function".

⑨ The count operation of the 8-bit interval timer 01 is started.

⑩ By DTC chain transfer, an interrupt request is generated from the 8-bit interval timer 01.

⑪ A/D conversion is started by the ELC setting (that sets an interrupt request from the 8-bit interval timer 01 as a hardware trigger for the A/D converter**)**.

⑫ The DTC is started by the A/D conversion end interrupt request.

⑬ By DTC chain transfer, set "stops A/D voltage comparator operation".

⑭ By DTC chain transfer, the + side reference voltage source of the A/D converter is set to AVDD and set "do not use the SNOOZE mode function".

⑮ By DTC chain transfer, the A/D conversion result is transferred to the A/D conversion result storage variable.

⑯ By DTC chain transfer, the upper 8 bits of the A/D conversion result is transferred from the A/D conversion result storage variable to the lower 8 bits of the transfer source address storage variable.

⑰ By DTC chain transfer, the address value (FBH or FAH) for illuminance or remaining battery level is transferred from the mode setting variable to the upper 8 bits of the transfer source address storage variable. This operation generates the value of the address where the LED (LED1 to LED5) display data is stored.

⑱ By DTC chain transfer, the 8-bit interval timer 00 is disabled to activate the DTC transfer.

⑲ By DTC chain transfer, the address value of the transfer source address storage variable is set as the transfer source address of the control data 14 triggered by the 8-bit interval timer 01.

⑳ By DTC chain transfer, the 8-bit interval timer 00 is enabled to activate the DTC transfer.

㉑ By DTC chain transfer, the LED (LED6) display data is stored in the LED display data storage variable by transferring the value of the mode setting variable.

㉒ By DTC chain transfer, the count operation of the 8-bit interval timer 01 is stopped.

㉓ By DTC chain transfer, the 8-bit interval timer 01 compare value is initialized.

1.2 LED Display

Table 1.2 shows the peripheral functions used for LED display and their applications. Figure 1.3 shows an overview of the operations. Figure 1.4 is the timing chart. Figure 1.5 shows the relationship between the switch and LED displays.

Table 1.2 Peripheral Functions and Applications (LED Display)

Peripheral Function	Application
P50-P53,57	· Outputs LED display data.
P60-P61	· Selects the LEDs to be displayed (LED1 to LED5 or LED6).
12-bit interval timer	· Counts the periods for LED lighting control. · Generates an interrupt request to activate the DTC. · Counting: 134 µs typ. (the maximum speed of the 12-bit interval timer when the low-speed on-chip oscillator clock is selected)
DTC	Executes the following operation in 12-bit interval timer interrupt processing. · Transfers the LED display data to the P5 and P6 registers.

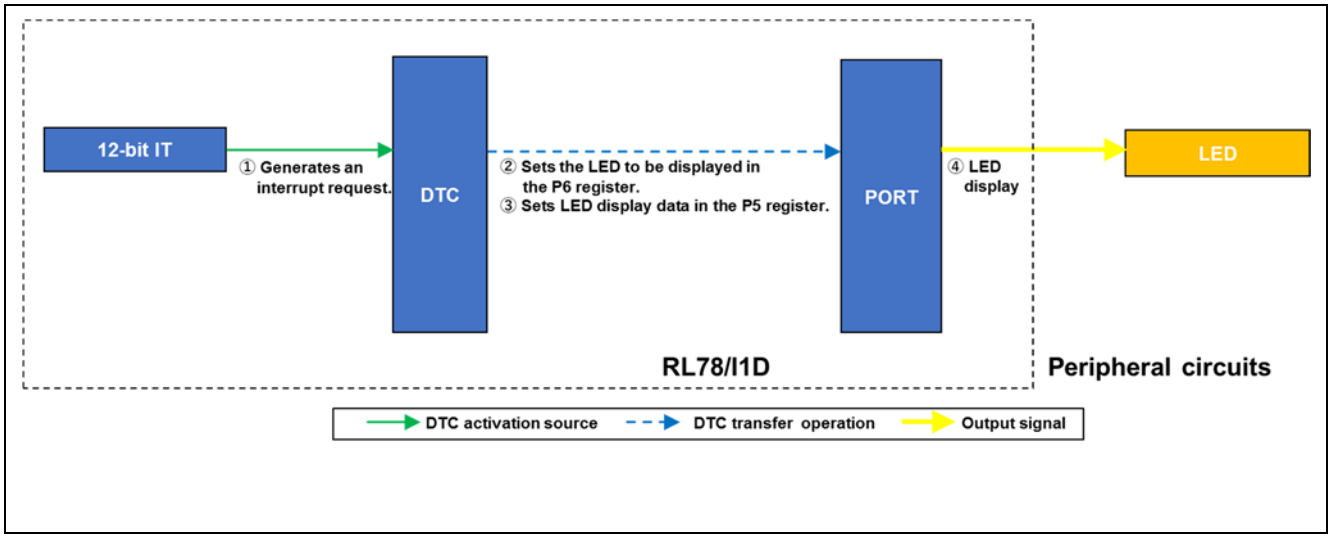


Figure 1.3 Overview Of The Operation (LED Display)

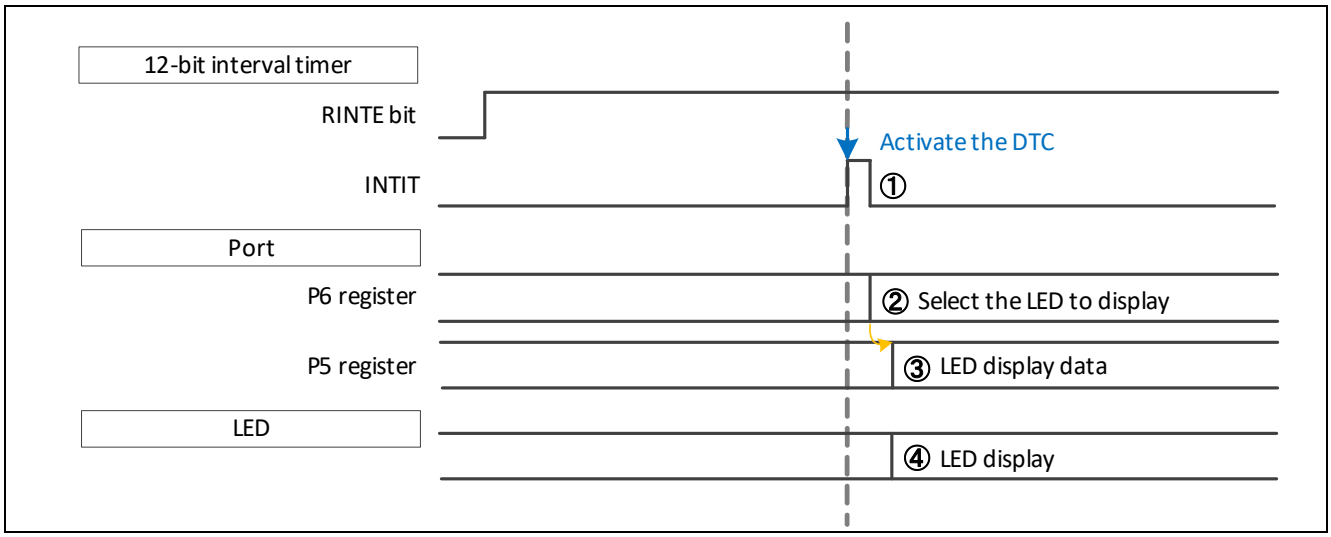


Figure 1.4 Operation Timing (LED Display)

Note: 1. The yellow arrows in the above figure indicate the chain transfer sequence of the DTC.

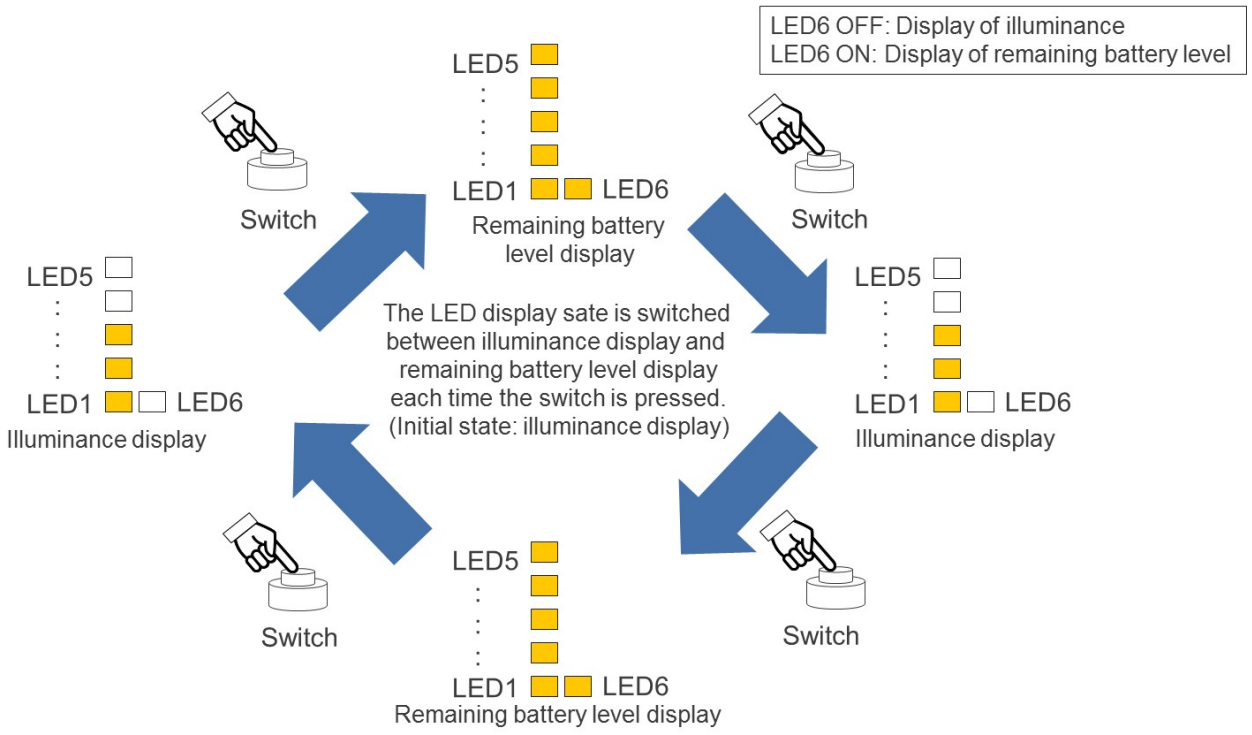
① The DTC is activated by an interrupt request from the 12-bit interval timer.

② The LED to be displayed is set in the P6 register by DTC transfer.

③ The LED display data is set in the P5 register by DTC chain transfer.

④ The LED is displayed.

LED display state is switched from “LED1 to LED5 ON” to “LED1 to LED6 OFF”, “LED6 ON”, and “LED1 to LED6 OFF” in this order each time an interrupt request is generated by the 12-bit interval timer.



Remaining battery level	LED1	LED2	LED3	LED4	LED5	LED6
86.3% or more	ON	ON	ON	ON	ON	ON
80.1% or more and less than 86.3%	ON	ON	ON	ON	OFF	ON
73.9% or more and less than 80.1%	ON	ON	ON	OFF	OFF	ON
67.8% or more and less than 73.9%	ON	ON	OFF	OFF	OFF	ON
61.5% or more and less than 67.8%	ON	OFF	OFF	OFF	OFF	ON
Less than 61.5%	OFF	OFF	OFF	OFF	OFF	ON

Illuminance	LED1	LED2	LED3	LED4	LED5	LED6
1000 lux or more	ON	ON	ON	ON	ON	OFF
670 lux or more and less than 1000 lux	ON	ON	ON	ON	OFF	OFF
550 lux or more and less than 670 lux	ON	ON	ON	OFF	OFF	OFF
300 lux or more and less than 550 lux	ON	ON	OFF	OFF	OFF	OFF
65 lux or more and less than 300 lux	ON	OFF	OFF	OFF	OFF	OFF
Less than 65 lux	OFF	OFF	OFF	OFF	OFF	OFF

Figure 1.5 Relationship between the Switch and LED Displays

1.3 Switch Input

The LED display state is switched between remaining battery level display and illuminance display each time the switch is pressed.

Table 1.3 shows the peripheral functions used for switch input and their applications. Figure 1.6 shows an overview of the operations. Figure 1.7 is the timing chart.

Table 1.3 Peripheral Functions and Applications (Switch Input)

Peripheral Function	Application
INTP0	· Stores the setting value for remaining battery level or illuminance in the mode setting variable when the switch is pressed. · Generates an interrupt request to activate the DTC.
DTC	Executes the following operation triggered by an interrupt request from INTP0. · Stores the setting value for remaining battery level or illuminance in the mode setting variable.

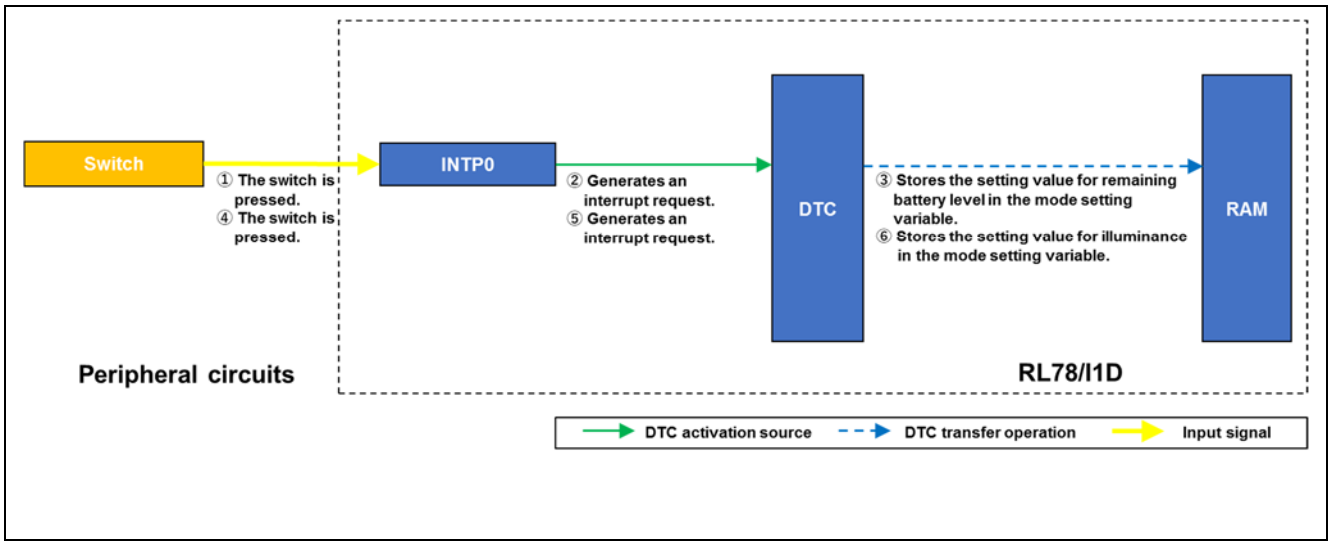


Figure 1.6 Overview of the Operation (Switch Input)

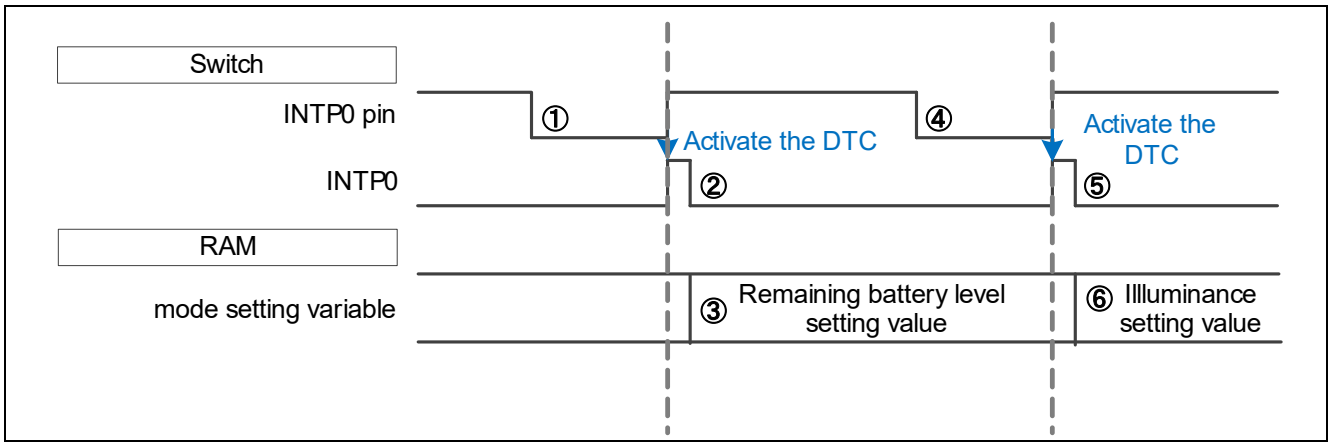


Figure 1.7 Operation Timing (Switch Input)

① The switch connected to the INTP0 pin is pressed.

② An interrupt request is generated by detection of a valid edge (rising edge) on the INTP0 pin.

③ The DTC is activated, and the setting values for remaining battery level (the A/D converter, the address where the LED (LED1 to LED5) display data is stored, and the LED (LED6) display data) are stored in the mode setting variable.

④ The switch connected to the INTP0 pin is pressed.

⑤ An interrupt request is generated by detection of a valid edge (rising edge) on the INTP0 pin.

⑥ The DTC is activated, and the setting value for illuminance (the A/D converter, the address where the LED (LED1 to LED5) display data is stored, and the LED (LED6) display data) is stored in the mode setting variable.

After the operation 6, remaining battery level display and illuminance display are alternately selected, each time the switch is pressed.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/I1D (R5F117GC)
Operating frequencies	● High-speed on-chip oscillator: 8MHz ● CPU/peripheral hardware clock: 8MHz ● Low-speed on-chip oscillator clock: 15kHz
Operating voltage	3.0V (operating range 1.9V to 5.5V) LVD operations (V_{LVD}): reset mode 1.88V (1.84V to 1.91V)
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.018 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.04.00 from Renesas Electronics Corp.
Board used	Renesas Electronics Corp. Evaluation Board

3. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

RL78/G13 Initialization CC-RL (R01AN2575E) Application Note

RL78/G13 A/D Converter (SNOOZE Mode) CC-RL (R01AN2804E) Application Note

RL78/G14 How to Use the DTC for the RL78/G14 CC-RL（R01AN0861E） Application Note

RL78/G14 Transferring A/D Conversion Result Using the DTC (R01AN0861E) Application Note

RL78/I1D Low Power Consuming Intermittent Operation of ADC Using DTC (R01AN2231E) Application Note

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used in this application note.

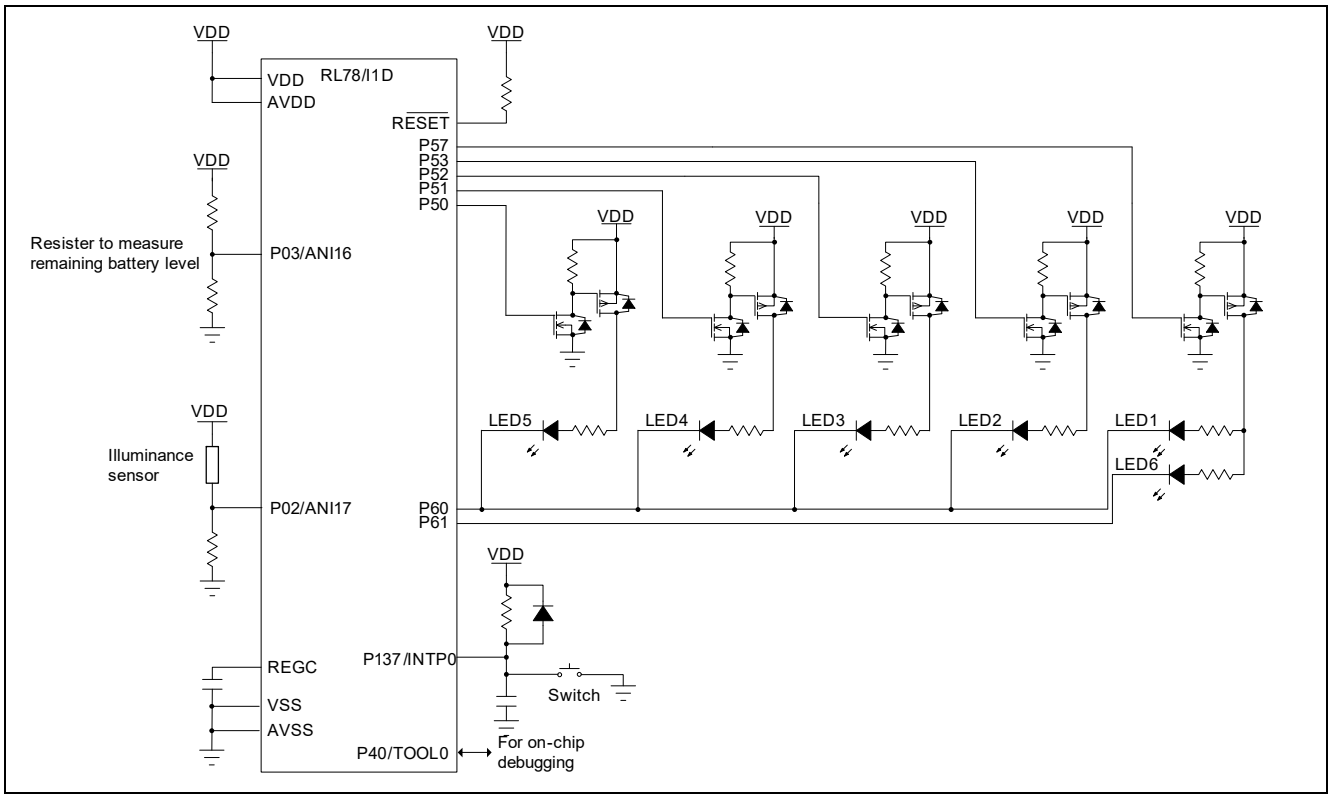


Figure 4.1 Hardware Configuration

Note: 1. This simplified circuit diagram was created to show an overview of connections only.
When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)
2. Make V_{DD} higher than the RESET release voltage (V_{LVD}) set in LVD.

4.2 Used Pin List

Table 4.1 provides List of Pins and Functions.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P50-P53, P57	Output	Outputs the LED display data.
P60-P61	Output	Selects the LEDs to be displayed (LED1 to LED5 or LED6).
P137	Input	Switch input (between the setting values for remaining battery level and illuminance)
P02/ANI16	Input	Analog input port (for measuring remaining battery level)
P03/ANI17	Input	Analog input port (for measuring illuminance sensor output)

5. Software Explanation

5.1 Operation Outline

In this application, A/D conversion and the LED display reflecting the A/D conversion result are performed without returning from STOP mode to normal operation by using the DTC, ELC, and SNOOZE mode. In addition, the target for A/D conversion and LED display is switched between remaining battery level and illuminance by pressing the switch.

The specific operations are described in ① to ⑳.

① Perform the initial setting of the ports. Turn off the LEDs (LED1 to LED6).

<Setting condition>

- Set P60 and P61 to high-level output.

② Perform the initial setting of the CPU. Select the high-speed on-chip oscillator clock (8 MHz) as the clock for SNOOZE mode operation. Select the low-speed on-chip oscillator clock as the operation clock of the 8-bit and 12-bit interval timers.

<Setting condition>

- Select the high-speed on-chip oscillator clock (8 MHz) as the main system clock.
- Select the low-speed on-chip oscillator clock as the subsystem clock.

③ Perform the initial setting of the 12-bit interval timer. Set the period for LED lighting control.

<Setting condition>

- Set the interval time to 134 μs.

④ Perform the initial setting of the 8-bit interval timer 00. Set the period for starting data processing.

< Setting condition >

- Set 8-bit count mode as the operation mode of the 8-bit interval timer 00.
- Set the interval time to 500 ms.

⑤ Perform the initial setting of the 8-bit interval timer 01. The interrupt request signal from the 8-bit interval timer 01 is used as a hardware trigger signal for the A/D converter.

< Setting condition >

- Set 8-bit count mode as the operation mode of the 8-bit interval timer 01.
- Set the interval time to 134 μs.

⑥ Perform the initial setting of the A/D converter for measuring illuminance.

< Setting condition >

- Set select mode for A/D conversion channel selection.
- Set one-shot conversion mode as the A/D conversion operation mode.
- Set hardware trigger wait mode as the A/D conversion start condition.
- Set the event signal selected by the ELC as a hardware trigger signal.
- Set the P03/ ANI17 pin as an analog input.
- Set the A/D conversion time to 11.375 μs.

⑦ DTC initialization.

<Setting condition >

Activation source: INTP0

Table 5.1 Activation Source: INTP0

Control data	Transfer mode	Data size	Transfer count	Block size	Transfer source address	Transfer destination address
0	Repeat mode	8 bits	2 times	5	&g_mode_sw_data. bat_adm2	&g_mode_data.adm2

- With control data 0, the setting value for remaining battery level stored in &g_mode_sw_data.bat_adm2 is transferred to the mode setting variable (&g_mode_data.adm2) in the first DTC transfer.
  In the second DTC transfer, the setting value for illuminance stored in &g_mode_sw_data.bat_adm2+5 is transferred to the mode setting variable (&g_mode_data.adm2).

  Since DTC transfer is performed in repeat mode, the data for the first and second DTC transfers are transferred alternately each time an interrupt request is generated.

Activation source: End of A/D conversion

Table 5.2 Activation Source: End of A/D conversion

Control data	Transfer mode	Data size	Transfer count	Block size	Transfer source address	Transfer destination address
1	Repeat mode	8 bits	once	1	&g_sfr.adm0_adce_clr	&ADM0
2	Normal mode	8 bits	once	1	&g_sfr.adm2_avdd	&ADM2
3	Normal mode	16 bits	once	1	&ADCR	&g_dtc_led.adcr_data
4	Normal mode	8 bits	once	1	&g_dtc_led.adcr_data + 1	&g_dtc_led.meter_address
5	Normal mode	8 bits	once	1	&g_mode_data.address	&g_dtc_led.meter_address + 1
6	Normal mode	8 bits	once	1	&g_sfr.dtcen2_it00_stop	&DTCEN2
7	Normal mode	8 bits	once	1	&g_dtc_led.meter_address	&dtc_controldata_14.dtsar
8	Normal mode	8 bits	once	1	&g_sfr.dtcen2_it00_start	&DTCEN2
9	Normal mode	8 bits	once	1	&g_mode_data.led	&g_dtc_led.mode_data
10	Normal mode	8 bits	once	1	&g_sfr.trtcr0_stop	&TRTCR0
11	Normal mode	8 bits	once	1	&g_sfr.trtcmp01_data	&TRTCMP01

- With control data 1, the setting value for stopping the A/D voltage comparator of the A/D converter is transferred from &g_sfr.adm0_adce_clr to the ADM0 register.
- With control data 2, the setting values for setting the + side reference voltage of the A/D converter to AVDD and for setting “do not use the SNOOZE mode function” are transferred from &g_sfr.adm2_avdd to the ADM2 register.
- With control data 3, the A/D conversion result stored in the ADCR register is transferred to the A/D conversion result storage variable (&g_dtc_led.adcr_data).
- With control data 4, the upper 8-bit value of the A/D conversion result stored in the A/D conversion result storage variable (&g_dtc_led.adcr_data + 1) is transferred to the lower 8 bits of the transfer source address storage variable (&g_dtc_led.meter_address).
- With control data 5, the address value stored in the mode setting variable (&g_mode_data.address) is transferred to the upper 8 bits of the transfer source address storage variable (&g_dtc_led.meter_address + 1). The address value reflecting the A/D conversion result is generated.
- With control data 6, the setting value for disabling the activation of the DTC for which the 8-bit interval timer 00 is used as an activation trigger is transferred from &g_sfr.dtcen2_it00_stop to the DTCEN2 register.
- With control data 7, the value of the address (at which the display data for illuminance is stored) stored in the transfer source address storage variable (&g_dtc_led_meter_address) is transferred to &dtc_controldata_14.dtsar. The transfer source address of the DTC for which the 8-bit interval timer 00 is used as an activation trigger is changed.
- With control data 8, the setting value for enabling the activation of the DTC for which the 8-bit interval timer 00 is used as an activation trigger is transferred from &g_sfr.dtcen2_it00_start to the DTCEN2 register.
- With control data 9, the LED6 display data stored in the mode setting variable (&g_mode_data.led) is transferred to the display data storage variable (&g_dtc_led_meter_data).
- With control data 10, the setting value to stop counting by the 8-bit interval timer 01 is transferred from &g_sfr.trtcr0_stop to the TRTCR0 register.
- With control data 11, the setting value for setting again the compare value of the 8-bit interval timer 01 is transferred from &g_sfr.trtcmp01_data to the TRTCMP01 register.

Activation source: 12-bit interval timer

Table 5.3 Activation Source: 12-bit interval timer

Control data	Transfer mode	Data size	Transfer count	Block size	Transfer source address	Transfer destination address
12	Repeat mode	8 bits	4 times	1	&g_dtc_led_P6	&P6
13	Repeat mode	8 bits	4 times	1	&g_dtc_led_P5	&P5

- With control data 12, the data stored in &g_dtc_led_P6 is transferred to the P6 register. The LEDs to be displayed are selected.
- With control data 13, the LED display data stored in the display data output variable (&g_dtc_led_P5) is transferred to the P5 register.
- The LED1 to LED5 display is turned on by the first DTC transfer.
  The LED1 to LED6 display is turned off by the second DTC transfer.
  The LED6 display is turned on by the third DTC transfer.
  The LED1 to LED6 display is turned off by the fourth DTC transfer.

Activation source: 8-bit interval timer 00

Table 5.4 Activation Source: 8-bit interval timer 00

Control data	Transfer mode	Data size	Transfer count	Block size	Transfer source address	Transfer destination address
14	Repeat mode	8 bits	once	1	0xFA00	&g_dtc_led_P5
15	Normal mode	8 bits	once	1	&g_dtc_led.mode_data	&g_dtc_led_P5 + 2
16	Normal mode	8 bits	once	1	&g_mode_data.adm2	&ADM2
17	Normal mode	8 bits	once	1	&g_mode_data.ads	&ADS
18	Normal mode	8 bits	once	40	0xF700	0xF701
19	Normal mode	8 bits	once	1	&g_sfr.adm0_adce_set	&ADM0
20	Normal mode	8 bits	once	1	&g_mode_data.awc_set	&ADM2
21	Normal mode	8 bits	once	1	&g_sfr.trtcr0_start	&TRTCR0

- With control data 14, the LED (LED1 to LED5) display data is transferred from the address of the transfer source address storage variable generated by reading the A/D conversion result to &g_dtc_led_P5.
- With control data 15, the LED (LED6) display data stored in the display data storage variable (&g_dtc_led.mode_data) is transferred to the display data output variable (&g_dtc_led_P5 + 2).
- With control data 16, the value for setting the + side reference voltage of the A/D converter is transferred from the mode setting variable (&g_mode_data.adm2) to the ADM2 register.
- With control data 17, the value for setting the analog input channel of the A/D converter is transferred from the mode setting variable (&g_mode_data.ads) to the ADS register.
- With control data 18, 40-byte transfer is performed to provide the time (10 μs) for stabilization of the + side reference voltage of the A/D converter.
- With control data 19, the setting value for enabling the A/D voltage comparator of the A/D converter is transferred from &g_sfr.adm0_adce_set to the ADM0 register.
- With control data 20, the setting value for setting "use the SNOOZE mode function" of the A/D converter is transferred from the mode setting variable (&g_mode_data.awc_set) to the ADM2 register.
- With control data 21, the setting value for starting count operation of the 8-bit interval timer 01 is transferred from &g_sfr.trtcr0_start to the TRTCR0 register.

⑧ ELC initialization.

<Setting condition >

- Set the A/D converter as a link destination peripheral function of ELSELR10 (8-bit interval timer 00).

⑨ Variables initialization.

< Setting condition >

Table 5.5 Variables Initialization (1/2)

Variable Name	Setting Value	Contents
g_dtc_led_P5[0]-[3]	0x00, 0x00, 0x00, 0x00	The setting value for the P5 register (for turning off the LED1 to LED5 display)
g_dtc_led_P6[0]-[3]	0x0E, 0x0F, 0x0D, 0x0F	The setting value for the P6 register 0x0E: Turns on the LED1 to LED5 display. 0x0D: Turns on the LED6 display. 0x0F: Turns off the LED1 to LED6 display.
g_dtc_led.adcr_data	0x00000000	Stores the value of the ADCR register.
g_dtc_led.meter_address	0x0000FA00	Sets the address in which the LED (LED1 to LED5) display data (illuminance) is stored.
g_dtc_led.mode_data	0x00	The setting value of the LED (LED6) display data
g_mode_sw_data.bat_adm2	0x80	The setting value for the ADM2 register (ADREFP1 bit = 1, ADREFP0 bit = 0)
g_mode_sw_data.bat_awc_set	0x84	The setting value for the ADM2 register (AWC bit = 1)
g_mode_sw_data.bat_ads	0x10	The setting value for the ADS register (analog input channel: ANI16)
g_mode_sw_data.bat_address	0xFB	Sets the upper 8 bits of the address in which the LED display data (remaining battery level) is stored.
g_mode_sw_data.bat_led	0x80	The setting value of the LED (LED6 to LED10) display data (remaining battery level)
g_mode_sw_data.ls_adm2	0x00	The setting value for the ADM2 register (ADREFP1 bit = 0, ADREFP0 bit = 0)
g_mode_sw_data.ls_awc_set	0x04	The setting value for the ADM2 register (AWC bit = 1)
g_mode_sw_data.ls_ads	0x11	The setting value for the ADS register (analog input channel: ANI17)
g_mode_sw_data.ls_address	0xFA	Sets the upper 8 bits of the address in which the LED display data (illuminance) is stored.
g_mode_sw_data.ls_led	0x00	The setting value of the LED (LED6 to LED10) display data (illuminance)
g_mode_data.adm2	0x 00	The setting value for the ADM2 register (ADREFP1 bit = 0, ADREFP0 bit = 0)
g_mode_data.awc_set	0x 04	The setting value for the ADM2 register (AWC bit = 1)
g_mode_data.ads	0x 11	The setting value for the ADS register (analog input channel: ANI17)
g_mode_data.address	0x FA	Sets the upper 8 bits of the address in which the LED display data (illuminance sensor) is stored.

Table 5.6 Variables Initialization (2/2)

Variable Name	Setting Value	Contents
g_mode_data.led	0x 00	The setting value of the LED (LED6 to LED10) display data (illuminance)
g_sfr.adm0_adce_clr	0x34	The setting value for the ADM0 register (ADCE bit = 0)
g_sfr.adm0_adce_set	0x35	The setting value for the ADM0 register (ADCE bit = 1)
g_sfr.adm2_avdd	0x00	The setting value for the ADM2 register (ADREFP1 bit = 0, ADREFP0 bit = 0)
g_sfr.dtcen2_it00_stop	0x80	The setting value for the DTCEN2 register (DTCEN26 bit = 0)
g_sfr.dtcen2_it00_start	0xC0	The setting value for the DTCEN2 register (DTCEN26 bit = 1)
g_sfr. trtcmp01_data	0x01	The setting value for the TRTCMP01 register
g_sfr. trtcr0_stop	0x11	The setting value for the TRTCR0 register (TSTART01 bit = 0)
g_sfr. trtcr0_start	0x15	The setting value for the TRTCR0 register (TSTART01 bit = 1)
g_wait_data[50]	0x00（all areas）	The area used for DTC transfer to wait for stabilization of the + side reference voltage of the A/D converter
g_level_data_ls[0]	LED_LEVEL_METER_0	The setting value for turning off the LED1 to LED5 display
g_level_data_ls[1]-[3]	LED_LEVEL_METER_1	The setting value for turning on the LED1 display
g_level_data_ls[4]-[6]	LED_LEVEL_METER_2	The setting value for turning on the LED1 and LED2 display
g_level_data_ls[7]-[9]	LED_LEVEL_METER_3	The setting value for turning on the LED1 to LED3 display
g_level_data_ls[10]-[12]	LED_LEVEL_METER_4	The setting value for turning on the LED1 to LED4 display
g_level_data_ls[13]-[15]	LED_LEVEL_METER_5	The setting value for turning on the LED1 to LED5 display
g_level_data_bat[0]-[8]	LED_LEVEL_METER_0	The setting value for turning off the LED1 to LED5 display
g_level_data_bat[9]-[10]	LED_LEVEL_METER_1	The setting value for turning on the LED1 display
g_level_data_bat[11]	LED_LEVEL_METER_2	The setting value for turning on the LED1 and LED2 display
g_level_data_bat[12]	LED_LEVEL_METER_3	The setting value for turning on the LED1 to LED3 display
g_level_data_bat[13]	LED_LEVEL_METER_4	The setting value for turning on the LED1 to LED4 display
g_level_data_bat[14]-[15]	LED_LEVEL_METER_5	The setting value for turning on the LED1 to LED5 display

⑩ Activate the DTC.

< Setting condition >

- Set the DTCEN06 bit in the DTCEN0 register to “1” (activation enabled).
- Set the DTCEN16 bit in the DTCEN1 register to “1” (activation enabled).
- Set the DTCEN26 bit in the DTCEN2 register to “1” (activation enabled).
- Set the DTCEN27 bit in the DTCEN2 register to “1” (activation enabled).

⑪ Start the count operation of the 8-bit interval timer 00.

<Setting condition>

- Set the TSTART00 bit in the TRTCR0 register to “1” (count operation started).

⑫ Start the count operation of the 12-bit interval timer.

<Setting condition>

- Set the RINTE bit in the ITMC register to “1” (count operation started).

⑬ Enable the SNOOZE mode function for the A/D converter.

<Setting condition>

- Set the AWC bit in the ADM2 register to “1” (use the SNOOZE mode function).

⑭ The operation mode is shifted to the STOP mode

⑮ An interrupt request is generated by compare match of the 8-bit interval timer 00 and DTC transfer is started.

<DTC transfer>

- Transfers the value stored in FFA00H (the address is updated according to the A/D conversion result in the second and subsequent DTC transfers) in the RAM area to the display data output variable (&g_dtc_led_P5[0]).
- Transfers the value stored in the display data storage variable (&g_dtc_led.mode_data) to the display data output variable (&g_dtc_led_P5[2]).
- Transfers the value stored in the mode setting variable (&g_mode_data.adm2) to the ADM2 register to set the + side reference voltage of the A/D converter.
- Transfers the value stored in the mode setting variable (&g_mode_data.ads) to the ADS register to set the analog input channel of the A/D converter.
- Transfers the value stored in FF700H to FF701H in the RAM area and repeats DTC transfer 40 times by incrementing the transfer source and destination addresses.
- Transfers the value stored in &g_sfr.adm0_adce_set to the ADM0 register to enable operation of the A/D voltage comparator of the A/D converter.
- Transfers the value stored in the mode setting storage variable (&g_mode_data.awc_set) to the ADM2 register to enable the SNOOZE mode function.
- Transfers the value stored in &g_sfr.trtcr0_start to the TRTCR0 register to start operation of the 8-bit interval timer 01.

⑯ An interrupt request is generated by compare match of the 8-bit interval timer 01. The ELC triggers A/D conversion.

⑰ An A/D conversion end interrupt request is generated to perform DTC transfer.

<DTC transfer>

- Transfers the value stored in &g_sfr.adm0_adce_clr to the ADM0 register to disable operation of the A/D voltage comparator of the A/D converter.
- Transfers the value stored in &g_sfr.adm2_avdd to the ADM2 register to set the + side reference voltage of the A/D converter to AVDD.
- Transfers the A/D conversion result stored in the ADCR register to the A/D conversion result storage variable (&g_dtc_led.adcr_data).
- Transfers the upper 8 bits of the A/D conversion result stored in the A/D conversion result storage variable (&g_dtc_led.adcr_data + 1) to the lower 8 bits of the transfer source address storage variable (&g_dtc_led.meter_address).
- Transfers the address value stored in the mode setting variable (&g_mode_data.address) to the upper 8 bits of the transfer source address storage variable (&g_dtc_led.meter_address+1) to store the address value of the LED (LED1 to LED5) display data to be read.
- Transfers the value stored in &g_sfr. dtcen2_it00_stop to the DTCEN2 register to disable the 8-bit interval timer 00 to activate the DTC.
- Transfers the address value of the LED (LED1 to LED5) display data stored in the transfer source address storage variable (&g_dtc_led.meter_address) to &dtc_controldata_14.dtsar to set the address value of the LED (LED1 to LED5) display data to be read to the transfer source address of control data 14.
- Transfers the value stored in &g_sfr. dtcen2_it00_start to the DTCEN2 register to enable the 8-bit interval timer 00 to activate the DTC.
- Transfers the value stored in the mode setting variable (&g_mode_data.led) to the display data storage variable (&g_dtc_led.mode_data) to store the LED (LED6) display data.
- Transfers the value stored in &g_sfr. trtcr0_stop to the TRTCR0 register to stop the count operation of the 8-bit interval timer 01.
- Transfers the value stored in &g_sfr. trtcmp01_data to the TRTCMP01 register to initialize the 8-bit interval timer 01 compare value.

⑱ 12-bit interval timer interval signal detection interrupt is generated to perform DTC transfer.

<DTC transfer>

- Transfers the value stored in &g_dtc_led_P6 to the P6 register to select the LEDs to be displayed.
- Transfers the value stored in the display data output variable (&g_dtc_led_P5) to the P5 register to perform LED display.

⑲ Pin input edge detection interrupt (INTP0) is generated to perform DTC transfer.

<DTC transfer>

- Transfers the value stored in &g_mode_sw_data.bat_adm2 to the mode setting variable (&g_mode_data.adm2) to transfer the setting values for remaining battery level and illuminance alternately each time an interrupt is generated.

⑳ The operations from ① to ⑰ are repeated.
The operation ⑱ is LED display and the operation ⑲ is switch input. They are operated at fixed intervals independently of the state of the operations ① to ⑰.

Note: Refer to the RL78/I1D User's Manual for usage notes concerning this device.

5.2 Option Byte Settings

Table 5.7 lists the option byte settings.

Table 5.7 OptionByte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD operation (V_{LVD}): reset mode Detection voltage: Rising edge 1.88 V/falling edge 1.84 V
000C2H/010C2H	10101010B	LS mode, High-speed on-chip oscillator clock: 8 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

5.3 Constants

Table 5.8 lists the constants that are used in this sample program.

Table 5.8 Constants for the Sample program

Constant Name	Setting Value	Contents
LED_LEVEL_METER_0	0x00	LED display setting value（LED1-LED5 OFF）
LED_LEVEL_METER_1	0x80	LED display setting value（LED1 ON）
LED_LEVEL_METER_2	0x88	LED display setting value（LED1-LED2 ON）
LED_LEVEL_METER_3	0x8C	LED display setting value（LED1-LED3 ON）
LED_LEVEL_METER_4	0x8E	LED display setting value（LED1-LED4 ON）
LED_LEVEL_METER_5	0x8F	LED display setting value（LED1-LED5 ON）

5.4 Variables

Table 5.9 and Table 5.10 lists the global variables that are used in the function R_DTC_Create.

The variable names used in Chapter 1 Specifications are also shown in the list.

Table 5.9 Variables (1/2)

Type	Variable Name		Contents
uint8_t	g_dtc_led_P5[4]	-	Stores the LED display data (to be set in the P5 register).
uint8_t	g_dtc_led_P6[4]	-	Stores the LED display data (to be set in the P6 register).
uint8_t	g_level_data_ls[16]	-	Stores the LED (LED1 to LED5) display data (illuminance).
uint8_t	g_level_data_bat[16]	-	Stores the LED (LED1 to LED5) display data (remaining battery level).
uint8_t	g_sfr.adm0_adce_clr	-	The setting value of the ADM0 register (for clearing the ADCE bit)
uint8_t	g_sfr.adm0_adce_set	-	The setting value of the ADM0 register (for setting the ADCE bit)
uint8_t	g_mode_sw_data.bat_adm2	-	The setting value of the ADM2 register (remaining battery level)
uint8_t	g_mode_sw_data.bat_awc_set	-	The setting value of the ADM2 register (for clearing the AWC bit) (remaining battery level)
uint8_t	g_mode_sw_data.bat_ads	-	The setting value of the ADS register (remaining battery level)
uint8_t	g_mode_sw_data.bat_address	-	Stores the upper 8 bits of the value of the address in which the LED (LED1 to LED5) display data is stored (remaining battery level).
uint8_t	g_mode_sw_data.bat_led	-	Stores the setting value of the LED (LED6) display data (remaining battery level).
uint8_t	g_mode_sw_data.ls_adm2	-	The setting value of the ADM2 register (illuminance)
uint8_t	g_mode_sw_data.ls_awc_set	-	The setting value of the ADM2 register (for clearing the AWC bit) (illuminance)
uint8_t	g_mode_sw_data.ls_ads	-	The setting value of the ADS register (illuminance)
uint8_t	g_mode_sw_data.ls_address	-	Stores the upper 8 bits of the value of the address in which the LED (LED1 to LED5) display data is stored (illuminance).
uint8_t	g_mode_sw_data.ls_led	-	Stores the setting value of the LED (LED6) display data (illuminance).
uint32_t	g_dtc_led.adcr_data	A/D conversion result storage variable	Stores the A/D conversion result.
uint32_t	g_dtc_led.meter_address	transfer source address storage variable	Stores the address value for reading the LED (LED1 to LED5) display data.
uint8_t	g_dtc_led.mode_data	display data storage variable	Stores the setting value of the LED (LED6) display data.
uint8_t	g_mode_data.adm2	mode setting variable	The setting value of the ADM2 register
uint8_t	g_mode_data.awc_set	mode setting variable	The setting value of the ADM2 register (for clearing the AWC bit)
uint8_t	g_mode_data.ads	mode setting variable	The setting value of the ADS register

Table 5.10 Variables (2/2)

uint8_t	g_mode_data.address	mode setting variable	Stores the upper 8 bits of the value of the address in which the LED (LED1 to LED5) display data is stored.
uint8_t	g_mode_data.led	mode setting variable	Stores the setting value for displaying mode.
uint8_t	g_wait_data[50]	-	Secures the RAM area for DTC transfer to provide the wait time.
uint8_t	g_sfr.dtcen2_it00_stop	-	The setting value of the DTCEN2 register (DTC activation disabled by the DTCEN26 bit)
uint8_t	g_sfr.dtcen2_it00_start	-	The setting value of the DTCEN2 register (DTC activation enabled by the DTCEN26 bit)
uint8_t	g_sfr.trtcr0_stop	-	The setting value of the TRTCR0 register (for stopping count operation)
uint8_t	g_sfr.trtcr0_start	-	The setting value of the TRTCR0 register (for starting count operation)
uint8_t	g_sfr.trtcmp01_data	-	The setting value of the TRTCMP01 register
uint8_t	g_sfr.adm2_avdd	-	The setting value of the ADM2 register (for selecting AVDD)

5.5 Functions

Table 5.11 lists the functions.

Table 5.11 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of the peripheral functions
R_PORT_Create	Initial setting of the ports
R_CGC_Create	Initial setting of the CPU
R_IT_Create	Initial setting of the 12-bit interval timer
R_IT8Bit0_Channel0_Create	Initial setting of the 8-bit interval timer 00
R_IT8Bit0_Channel1_Create	Initial setting of the 8-bit interval timer 01
R_ADC_Create	Initial setting of the A/D converter
R_DTC_Create	Initial setting of the DTC
R_ELC_Create	Initial setting of the ELC
R_INTC_Create	Initial setting of the external interrupt
main	Main processing
R_MAIN_UserInit	Main initial setting
r_dtc_raminit	Variables initialization processing
R_IT8Bit0_Channel0_Start	8-bit interval timer00 count start
R_IT_Start	12-bit interval timer count start

5.6 Function Specifications

This part describes function specifications of the sample code.

[Function name] hdwinit

Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	This function is used for initial setting of peripheral functions.
Arguments	None
Return value	None
Remarks	None

[Function name] R_Systeminit

Outline	Initial setting of the peripheral functions
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_cgc.h, r_cg_port.h, r_cg_it.h, r_cg_it8bit.h, r_cg_adc.h, r_cg_dtc.h, r_cg_elc.h, r_cg_intp.h
Declaration	void R_Systeminit(void)
Description	This function is used for initial setting of peripheral functions used in this application note.
Arguments	None
Return value	None
Remarks	None

[Function name] R_PORT_Create

Outline	Initial setting of the ports
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_port.h
Declaration	void R_PORT_Create(void)
Description	This function is used for initial setting of ports.
Arguments	None
Return value	None
Remarks	None

[Function name] R_CGC_Create

Outline	Initial setting of the CPU
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	This function is used for initial setting of the CPU.
Arguments	None
Return value	None
Remarks	None

[Function name] R_IT_Create

Outline	Initial setting of the 12-bit interval timer
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_it.h
Declaration	void R_IT_Create(void)
Description	This function is used for initial setting of the 12-bit interval timer.
Arguments	None
Return value	None
Remarks	None

[Function name] R_IT8Bit0_Channel0_Create

Outline	Initial setting of the 8-bit interval timer00
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_it8bit.h
Declaration	void R_IT8Bit0_Channel0_Create(void)
Description	This function is initial setting for use in 8-bit count mode.
Arguments	None
Return value	None
Remarks	None

[Function name] R_IT8Bit0_Channel1_Create

Outline	Initial setting of the 8-bit interval timer01
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_it8bit.h
Declaration	void R_IT8Bit0_Channel1_Create(void)
Description	This function is initial setting for use in 8-bit count mode.
Arguments	None
Return value	None
Remarks	None

[Function name] R_ADC_Create

Outline	Initial setting of the A/D converter
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_adc.h
Declaration	void R_ADC_Create(void)
Description	This function is used for initial setting to use the A/D converter in the hardware trigger wait mode (select mode, one-shot conversion mode).
Arguments	None
Return value	None
Remarks	None

[Function name] R_DTC_Create

Outline	Initial setting of the DTC
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_dtc.h
Declaration	void R_DTC_Create(void)
Description	This function is used for initial setting of the DTC.
Arguments	None
Return value	None
Remarks	None

[Function name] R_ELC_Create

Outline	Initial setting of the ELC
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_elc.h
Declaration	void R_ELC_Create(void)
Description	This function is used for initial setting of the ELC.
Arguments	None
Return value	None
Remarks	None

[Function name] R_INTC_Create

Outline	Initial setting of the external interrupt
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_intp.h
Declaration	void R_INTC_Create(void)
Description	This function is used for initial setting of external interrupt.
Arguments	None
Return value	None
Remarks	None

[Function name] main

Outline	Main processing
Header	r_cg_macrodriver.h, r_cg_userdefine.h
Declaration	void main(void)
Description	This function is used for main processing.
Arguments	None
Return value	None
Remarks	None

[Function name] R_MAIN_UserInit

Outline	Main initial setting
Header	r_cg_macrodriver.h, r_cg_it.h, r_cg_it8bit.h, r_cg_dtc.h
Declaration	void R_MAIN_UserInit(void)
Description	This function is used for main initial setting.
Arguments	None
Return value	None
Remarks	None

[Function name] r_dtc_raminit

Outline	Variables initialization processing
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_dtc.h
Declaration	void r_dtc_raminit(void)
Description	This function is used for initial setting of variables.
Arguments	None
Return value	None
Remarks	None

[Function name] R_IT8Bit0_Channel0_Start

Outline	8-bit interval timer00 count start
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_it8bit.h
Declaration	void R_IT8Bit0_Channel0_Start(void)
Description	This function is used for setting to enable activation of the 8-bit interval timer 00.
Arguments	None
Return value	None
Remarks	None

[Function name] R_IT _Start

Outline	12-bit interval timer count start
Header	r_cg_macrodriver.h, r_cg_userdefine.h, racist's
Declaration	void R_IT _Start(void)
Description	This function is used for setting to enable activation of the 12-bit interval timer.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows an overall flow of the sample code.

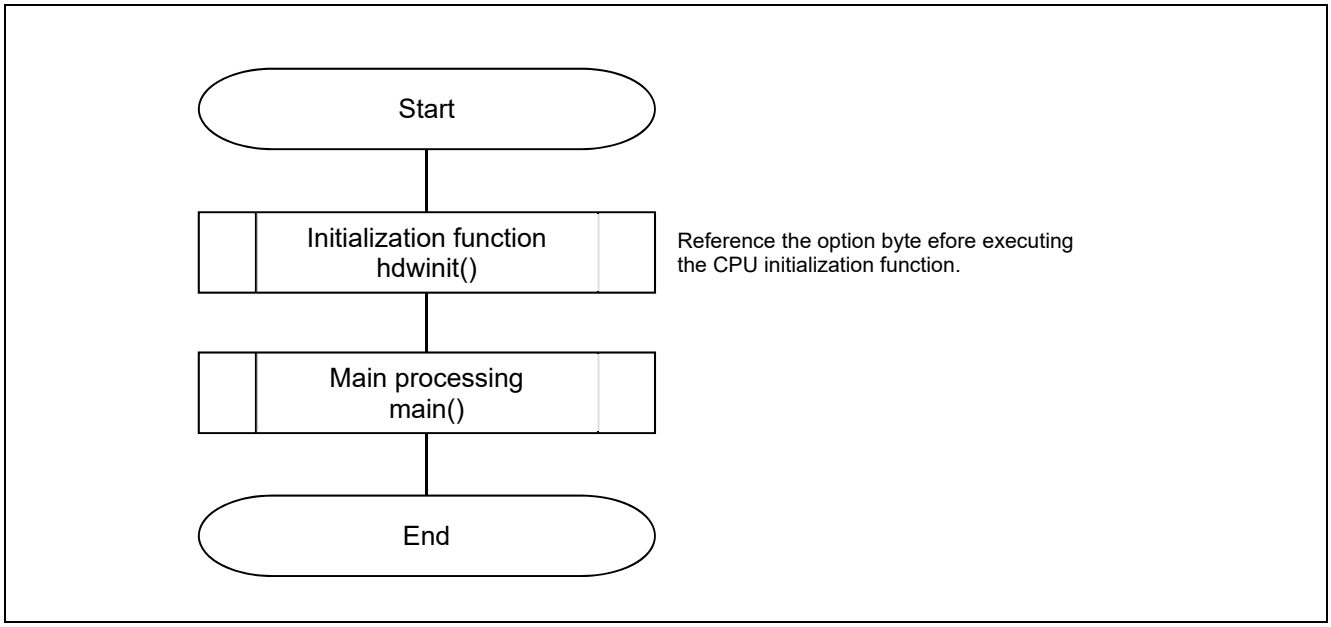


Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

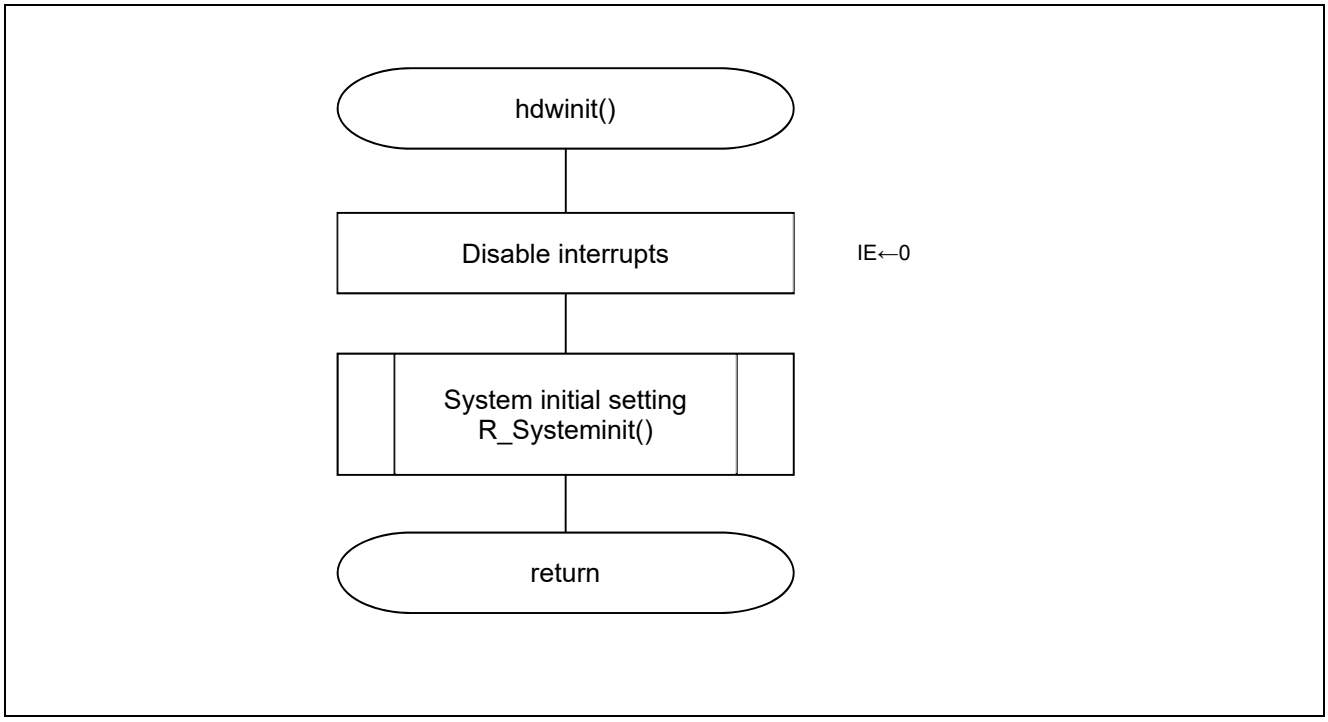


Figure 5.2 Initialization Function

5.7.2 System Initial Setting

Figure 5.3 and Figure 5.4 shows the flowchart for the system initial setting.

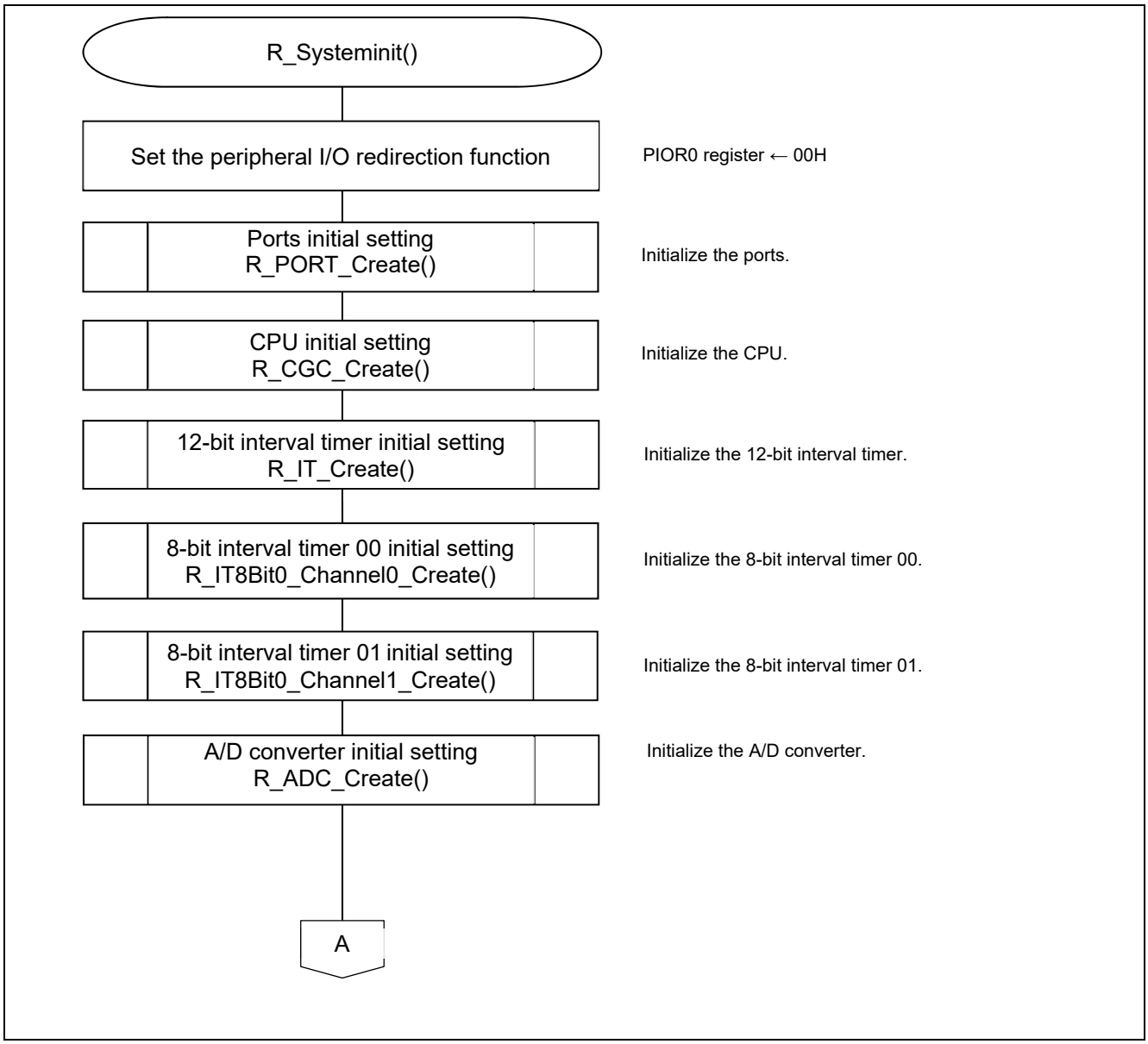


Figure 5.3 System Initial Setting (1/2)

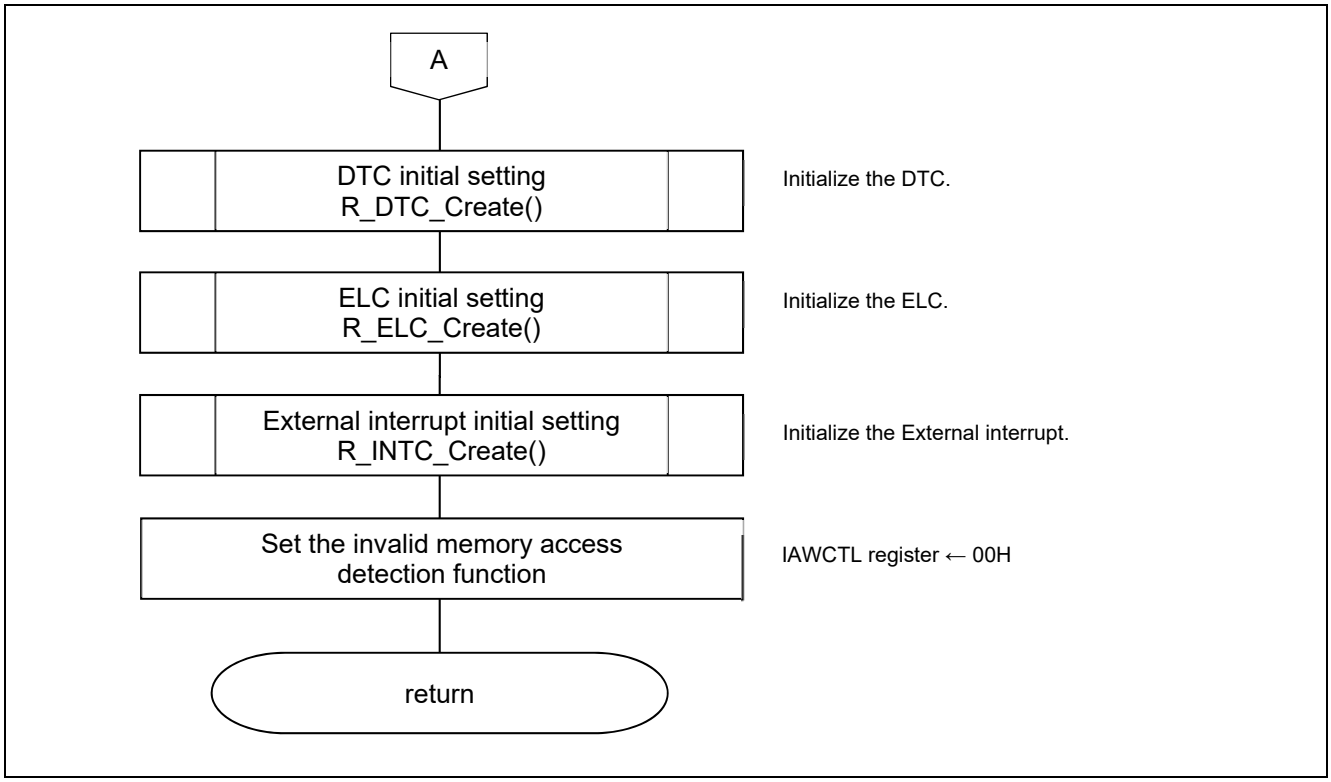


Figure 5.4 System Initial Setting (2/2)

5.7.3 Ports Initial Setting

Figure 5.5 shows the flowchart for the ports initial setting.

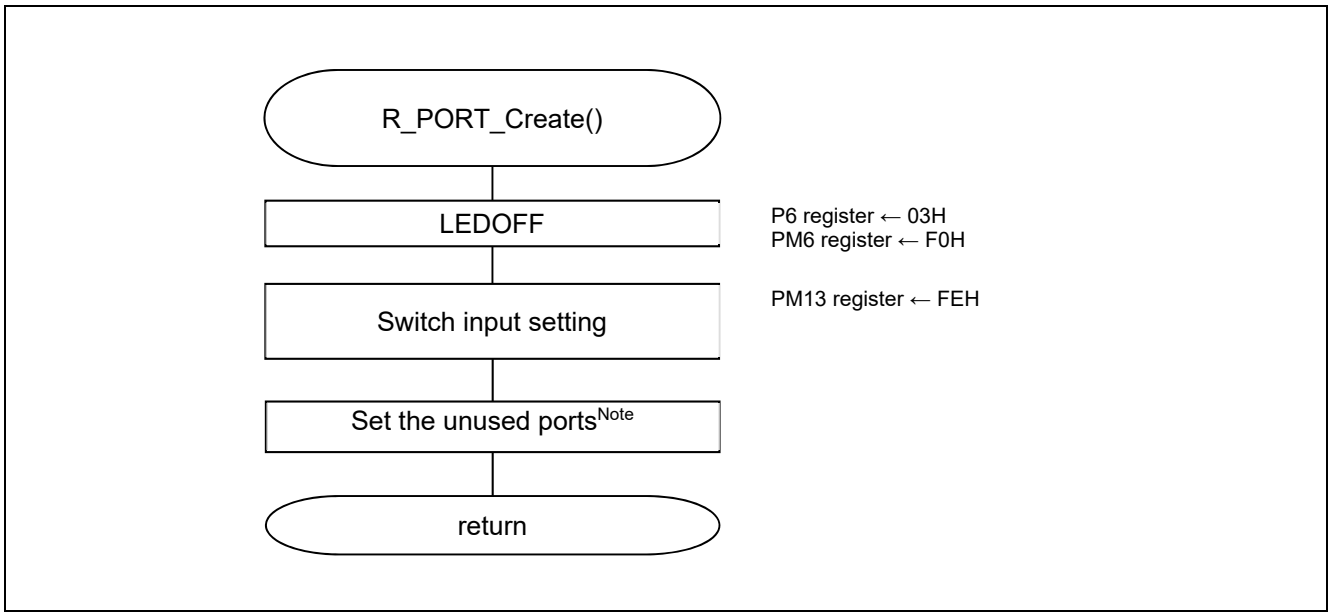


Figure 5.5 Port Initial Setting

Note: Refer to the initialization flowchart in the RL78/G13 Initialization CC-RL (R01AN2575E) Application Note for details on how to set unused ports.

Caution: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

5.7.4 CPU Initial Setting

Figure 5.6 shows the flowchart for the CPU initial setting.

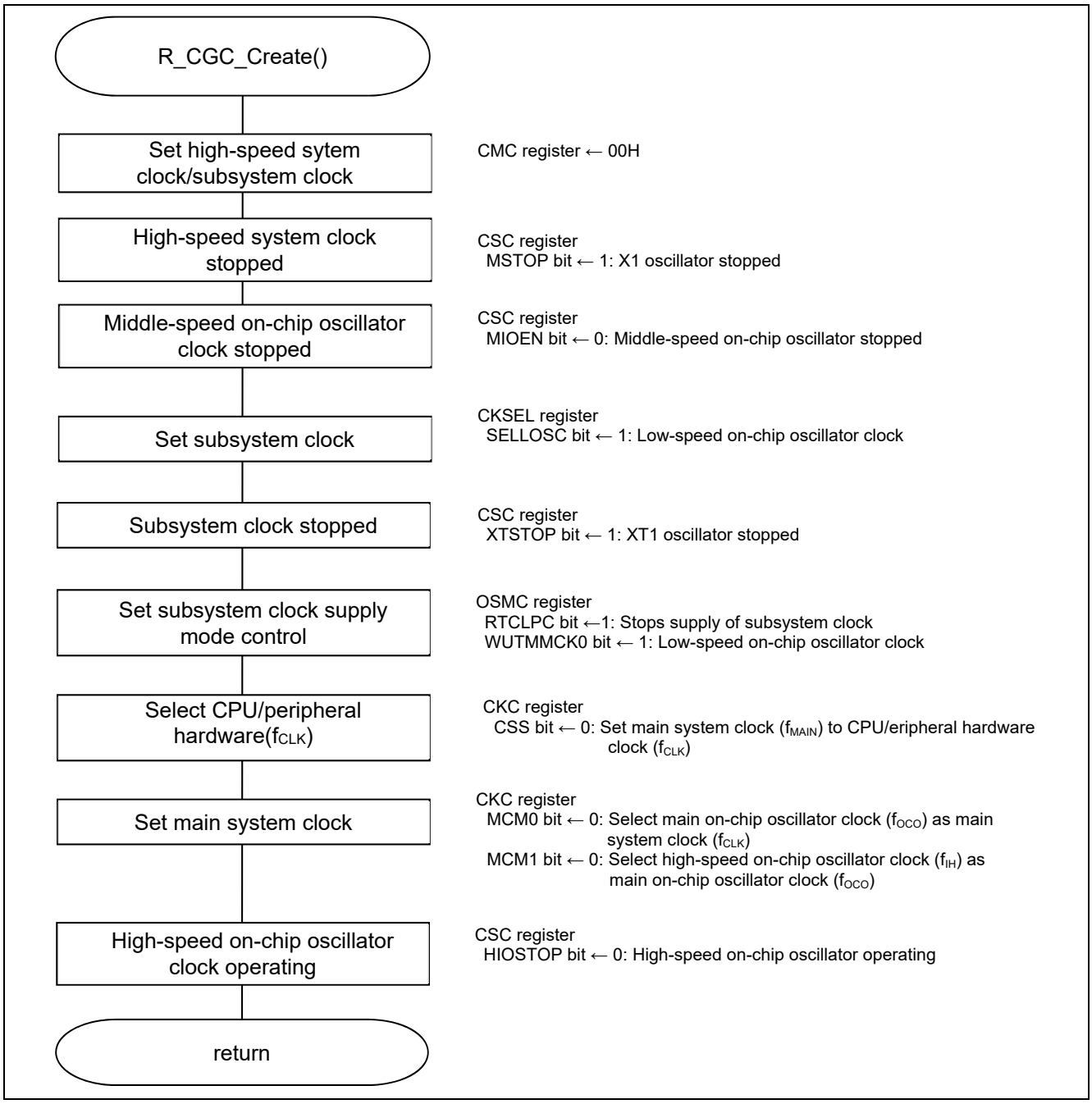


Figure 5.6 CPU Initial Setting

Clock operation mode setting

- Clock operation mode control register (CMC)

Set the high-speed system clock pin operation mode to input mode.
Set the subsystem clock pin operation mode to input mode.

Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH
0	**0**	**0**	**0**	0	**0**	**0**	**0**

Bits 7-6

EXCLK	OSCSEL	High-seed oscillation clock pin operation mode	X1/P121 Port	X2/EXCLK/P122 Port
0	**0**	**Input port mode**	**Input port**	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bits 5-4

EXCLKS	OSCSELS	Subsystem clock pin operation mode	XT1/P123 Pin	XT2/EXCLKS/P124 Pin
0	**0**	**Input port mode**	**Input port**	
0	1	XT1 oscillation mode	Crystal resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bits 2-1

AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection
0	**0**	**Low-power consumption oscillation (default)**
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	Setting prohibited

Bit 0

AMPH	Control of X1 clock oscillation frequency
0	**1MHz ≤ f_X ≤ 10MHz**
1	10MHz < f_X ≤ 20MHz

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

Operation control of clocks

- Clock operation status control register (CSC)

High-speed system clock operation control: X1 oscillator stopped
Subsystem clock operation control: XT1 oscillator stopped
Middle-speed on-chip oscillator clock operation control: Middle-speed on-chip oscillator stopped
High-speed on-chip oscillator clock operation control: High-speed on-chip oscillator operating

Symbol: CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP	0	0	0	0	MIOEN	HIOSTOP
1	**1**	x	x	x	x	**0**	**0**

Bit 7

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	**Input port**
1	**X1 oscillator stopped**	External clock from EXCLK pin is invalid	

Bit 6

XTSTOP	Subsystem clock operation control		
	XT1 oscillation mode	External clock input mode	Input port mode
0	XT1 oscillator operating	External clock from EXCLKS pin is valid	**Input port**
1	**XT1 oscillator stopped**	External clock from EXCLKS pin is invalid	

Bit 1

MIOEN	Middle-speed on-chip oscillator clock operation control
0	**Middle-speed on-chip oscillator stopped**
1	Middle-speed on-chip oscillator operating

Bit 0

HIOSTOP	High-speed on-chip oscillator clock operation control
0	**High-speed on-chip oscillator operating**
1	High-speed on-chip oscillator stopped

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

Subsystem clock setting

- Subsystem clock select register (CKSEL)

Select low-speed on-chip oscillator clock as subsystem clock.

Symbol: CKSEL

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SELLOSC
0	0	0	0	0	0	0	**1**

Bit 0

SELLOSC	Selection of sub clock/low-speed on-chip oscillator clock
0	Sub clock
1	**Low-speed on-chip oscillator clock**

Subsystem clock supply mode control

- Subsystem clock supply mode control register (OSMC)

Setting in STOP mode or in HALT mode while subsystem clock is selected as CPU clock

: Stops supply of subsystem clock to peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and clock output/buzzer output controller.

Selection of count clock for real-time clock and 12-bit interval timer: low-speed on-chip oscillator clock

Symbol: OSMC

7	6	5	4	3	2	1	0
RTCLPC	0	0	WUTMMCK0	0	0	0	0
1	0	0	**1**	0	0	0	0

Bit 7

RTCLPC	Setting in STOP mode or in HALT mode while subsystem clock is selected as CPU clock
0	Enables supply of subsystem clock to peripheral functions
1	**Stops supply of subsystem clock to peripheral functions other than the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and clock output/buzzer output controller.**

Bit 4

WUTMMCK0	Selection of operation clock for real-time clock 2, frequency measurement circuit, 12-bit interval timer, 8-bit interval timer, and clock output/buzzer output controller
0	Subsystem clock (f_{SUB})
1	**Low-speed internal oscillator clock**

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

System clock control setting

- System clock control register (CKC)

Select the high-speed on-chip oscillator clock as a CPU/peripheral hardware clock.

Symbol: CKC

7	6	5	4	3	2	1	0
CLS	CSS	MCS	MCM0	0	0	MCS1	MCM1
x	**0**	x	**0**	0	0	x	**0**

Bit 6

CSS	Selection of CPU/peripheral hardware clock (f_{CLK})
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Bit 4

MCM0	Main system clock (fMAIN) operation control
0	**Selects the main on-chip oscillator clock (f_{OCO}) as the main system clock (f_{MAIN})**
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

Bit 0

MCM1	Main on-chip oscillator clock (f_{oco}) operation control
0	**High-speed on-chip oscillator clock (f_{IH})**
1	Middle-speed on-chip oscillator clock (f_{IM})

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

5.7.5 12-bit Interval Timer Initial Setting

Figure 5.7 shows the flowchart for the 12-bit interval timer initial setting.

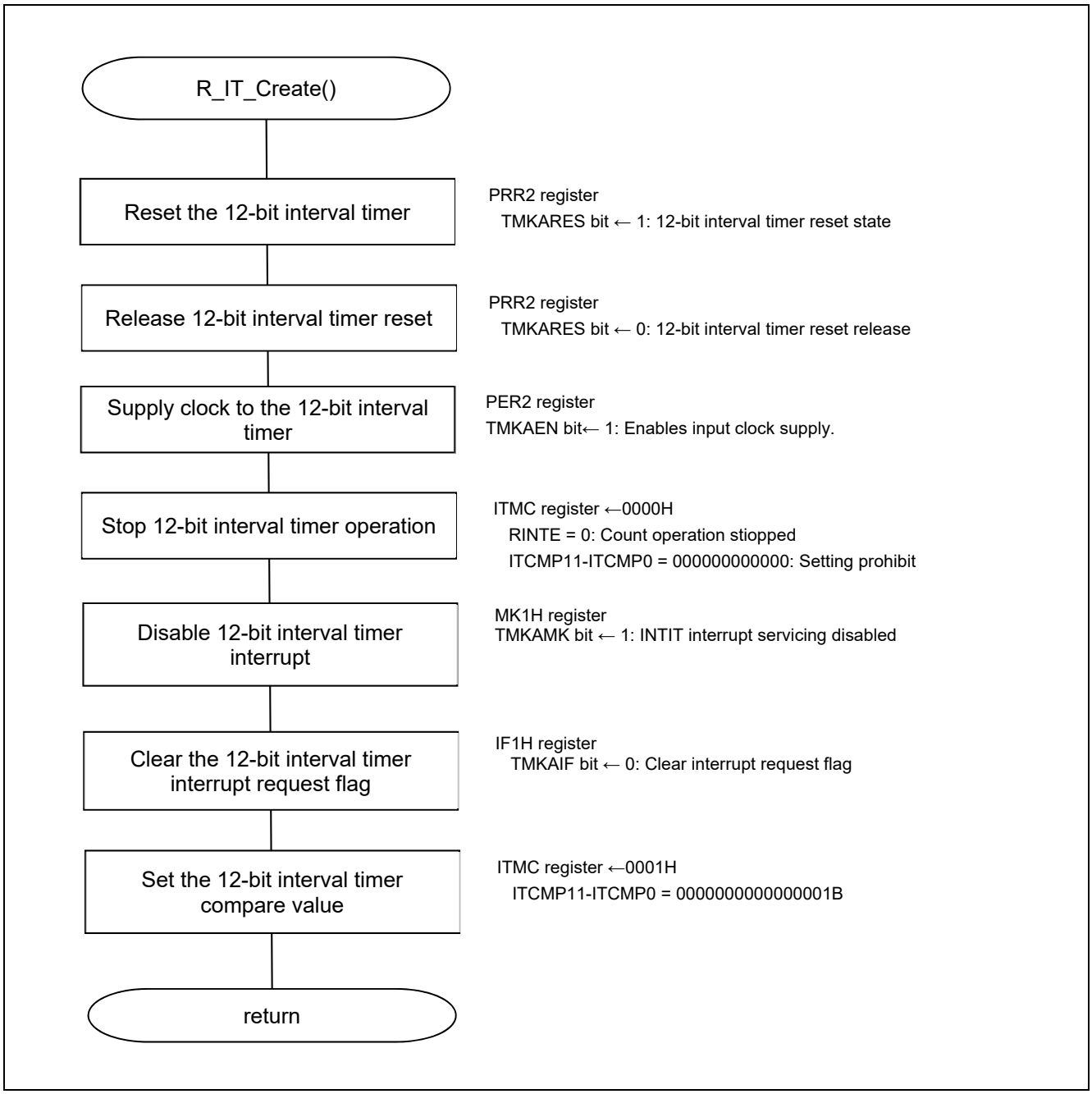


Figure 5.7 12-bit Interval Timer Initial Setting

Reset of 12-bit interval timer

- Peripheral reset control register2 (PRR2)

Reset of the 12-bit interval timer.

Symbol: PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	0
1	0	x	0	0	0	0	0

Bit 7

TMKARES	Reset control of 12-bit interval timer
0	12-bit interval timer reset release
1	**12-bit interval timer reset state**

12-bit interval timer clock supply setting

- Peripheral enable register 2 (PER2)

Enable clock supply to the 12-bit interval timer.

Symbol: PER2

7	6	5	4	3	2	1	0
TMKAEN	FMCEN	DOCEN	0	0	0	0	0
1	x	x	0	0	0	0	0

Bit 7

	Control of 12-bit interval timer input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

12-bit interval timer interval signal detection interrupt setting

- Interrupt request flag register (IF1H)

Clear TMKAIF interrupt source flag.

- Interrupt mask flag register (MK1H)

Set TMKAMK interrupt mask.

Symbol: IF1H

7	6	5	4	3	2	1	0
0	DOCIF	CMPIF1	CMPIF0	KRIF	TMKAIF	RTCIF	ADIF
0	x	x	x	x	**0**	x	x

Bit 2

TMKAIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

略号：MK1H

7	6	5	4	3	2	1	0
0	DOCMK	CMPMK1	CMPMK0	KRMK	TMKAMK	RTCMK	ADMK
0	x	x	x	x	**1**	x	x

Bit 2

TMKAMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

12 bit interval timre operation ad to specify the timer compare value setting

- 12-bit interval timer control register (ITMC)

Stop 12-bit interval timer count operation.

Set the 12-bit interval timer compare value.

Symbol: ITMC

15	14	13	12	11 - 0
RINTE	0	0	0	ITCMP 11 - ITCMP 0
0	0	0	0	**000000000001**

Bit 15

RINTE	12-bit interval timer operation control
0	**Count operation stopped (count clear)**
1	Count operation started

Bit 11-0

ITCMP11 - ITCMP0	Specification of 12-bit interval timer compare value
001H	**These bits generate an interrupt at the fixed cycle (count clock cycles x (ITCMP setting value + 1)).**
・・・	
FFFH	
000H	Setting prohibited

5.7.6 8-bit Interval Timer 00 Initial Setting

Figure 5.8 shows the flowchart for the 8-bit interval timer 00 initial setting.

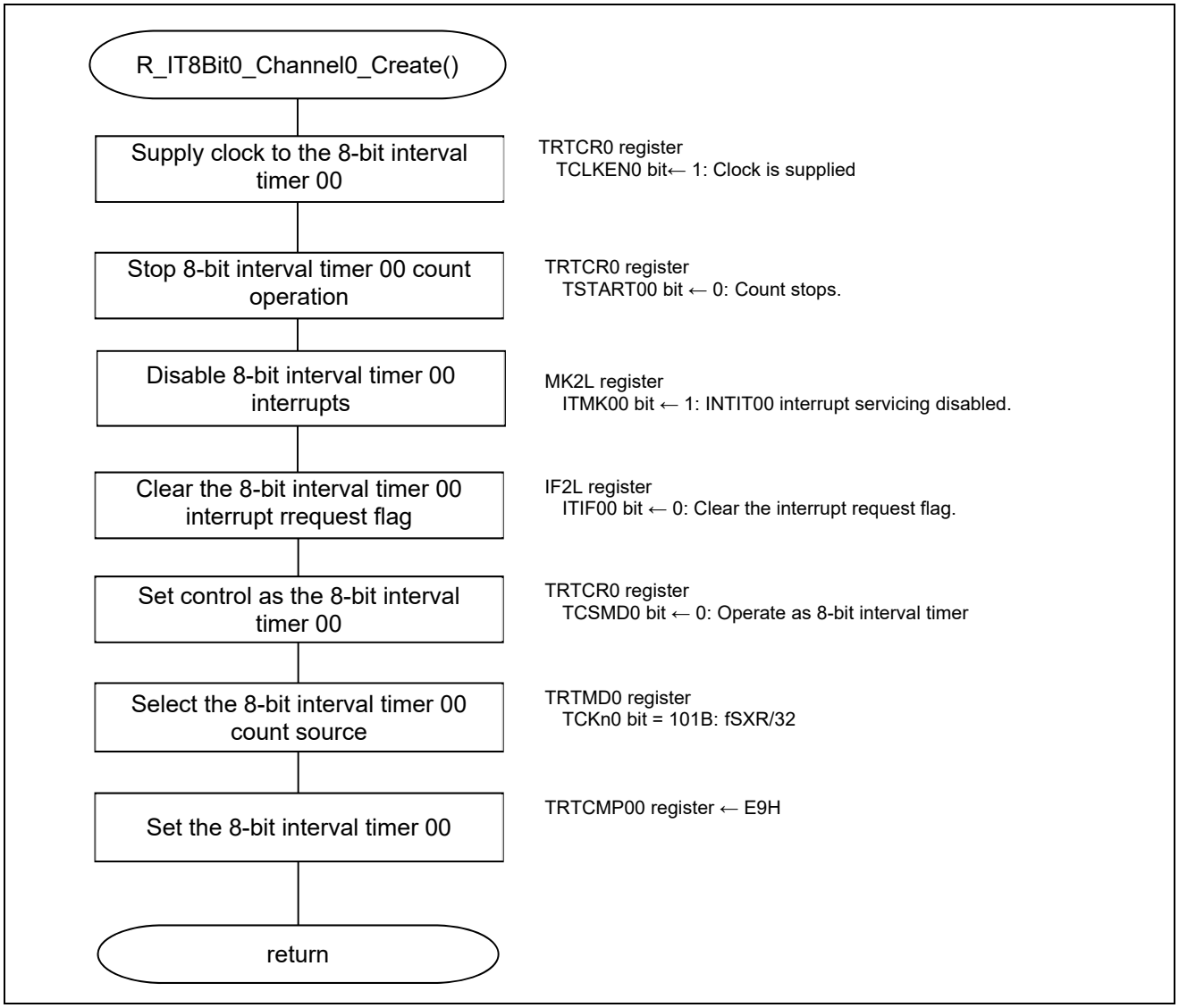


Figure 5.8 8-bit interval timer 00 initial setting

8-bit interval timer 00 control setting

- 8-bit interval timer control register 0 (TRTCR0)

Start clock supply as the 8-bit counter.

Symbol: TRTCR0

7	6	5	4	3	2	1	0
TCSMD0	0	0	TCLKEN0	0	TSTART01	0	TSTART00
0	0	0	**1**	0	x	0	**0**

Bit 7

TCSMD0	Mode selection
0	**Operates as 8-bit counter**
1	Operates as 16-bit counter (channel 0 and channel 1 are connected)

Bit 4

TCLKEN0	8-bit interval timer clock enable
0	Clock is stopped
1	**Clock is supplied**

Bit 0

TSTART00	8-bit interval timer 0 count start
0	**Count stops**
1	Count starts

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

8-bit interval timer 00 interrupt setting

- Interrupt mask flag register (MK2L)
Disable interrupt servicing.
- Interrupt request flag register (IF2L)
Clear the interrupt request flag.

Symbol: MK2L

7	6	5	4	3	2	1	0
FLMK	0	0	0	ITMK11	ITMK10	ITMK01	ITMK00
x	0	0	0	x	x	x	**1**

Bit 0

ITMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: IF2L

7	6	5	4	3	2	1	0
FLIF	0	0	0	ITIF11	ITIF10	ITIF01	ITIF00
x	0	0	0	x	x	x	**0**

Bit 0

ITIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

8-bit interval timer 00 count source setting

- 8-bit interval timer division register 0 (TRTMD0)
Set the division of 8-bit interval timer 0.

Symbol: TRTMD0

7	6	5	4	3	2	1	0
0	TCK01			0	TCK00		
0	x	x	x	0	**101**		

Bits 2-0

TCK00			8-bit interval timer 0 division selection
Bit 2	Bit 1	Bit 0	
0	0	0	fSXR or fIL
0	0	1	fSXR/2 or fIL/2
0	1	0	fSXR/4 or fIL/4
0	1	1	fSXR/8 or fIL/8
1	0	0	fSXR/16 or fIL/16
1	**0**	**1**	**fSXR/32 or fIL/32**
1	1	0	fSXR/64 or fIL/64
1	1	1	fSXR/128 or fIL/128

8-bit interval timer 00 count value setting

- 8-bit interval timer compare register 00 (TRTCMP00)
Set a count value.

Symbol: RTCMP00

7	6	5	4	3	2	1	0
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**

Bits 7-0

Function
8-bit counter

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

5.7.7 8-bit Interval Timer 01 Initial Setting

Figure 5.9 shows the flowchart for the 8-bit interval timer 01 initial setting.

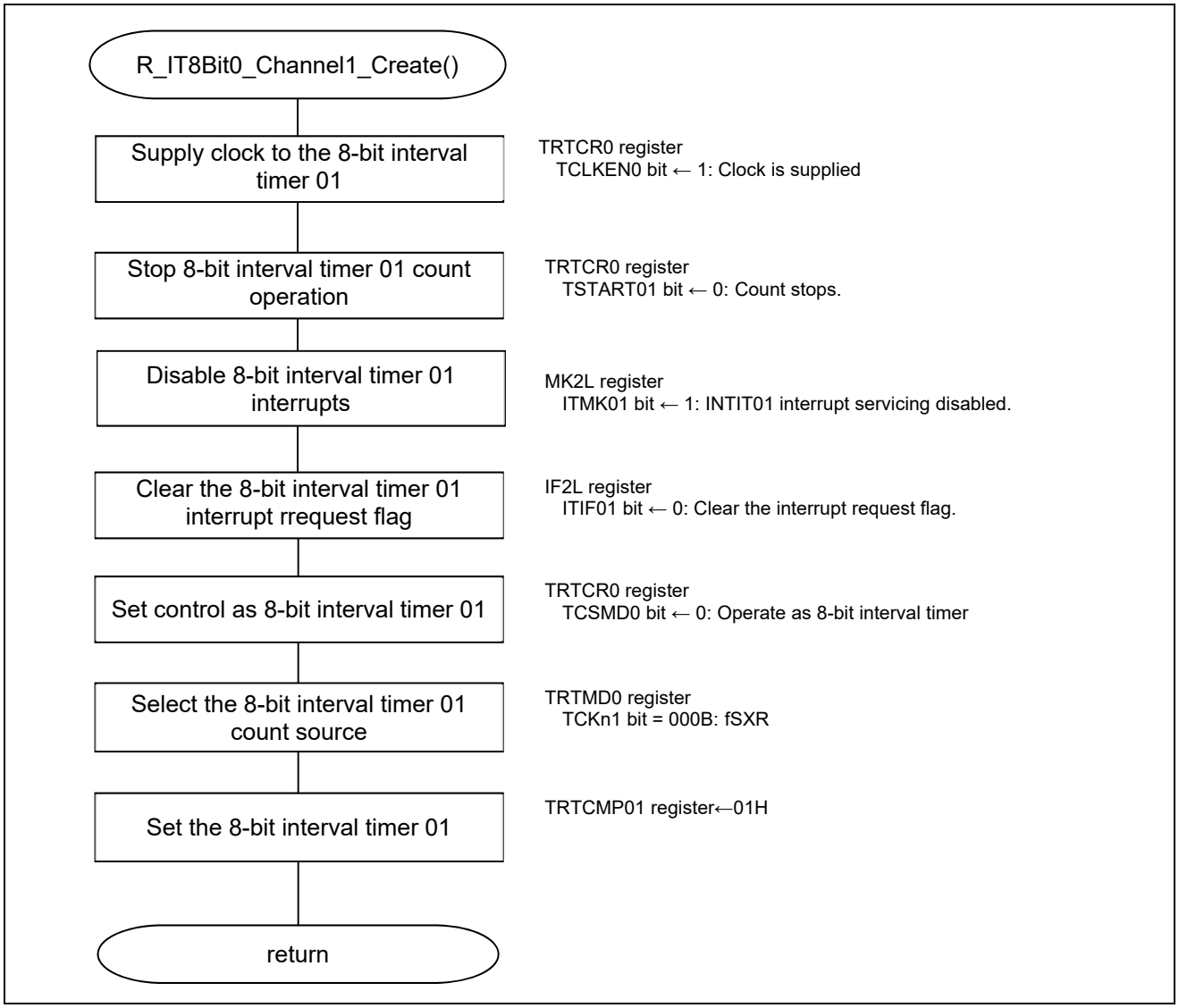


Figure 5.9 8-bit Interval Timer 01 Initial Setting

5.7.8 A/D Converter Initial Setting

Figure 5.10 and Figure 5.11 shows the flowchart for the A/D converter initial setting.

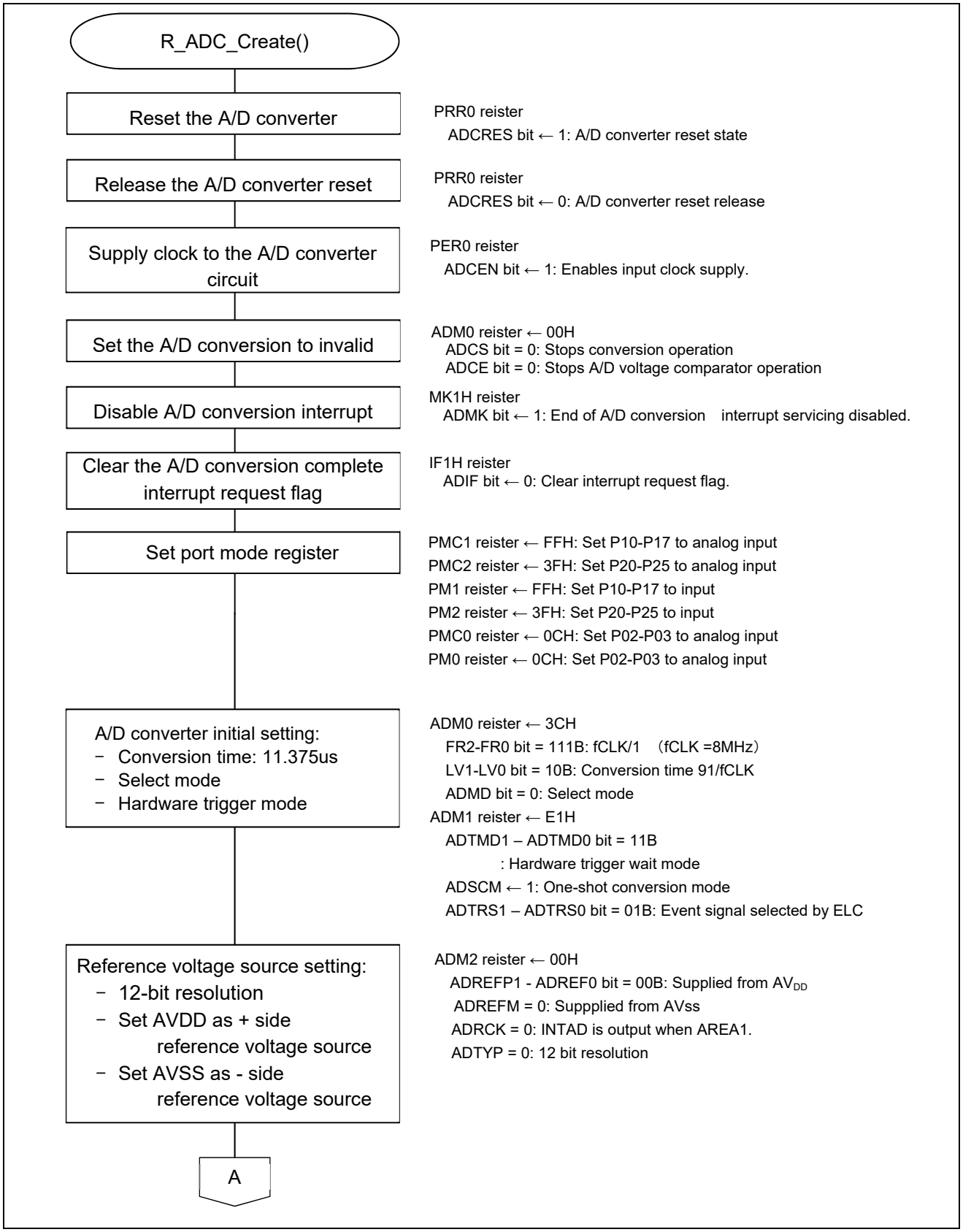


Figure 5.10 A/D Converter Initial Setting (1/2)

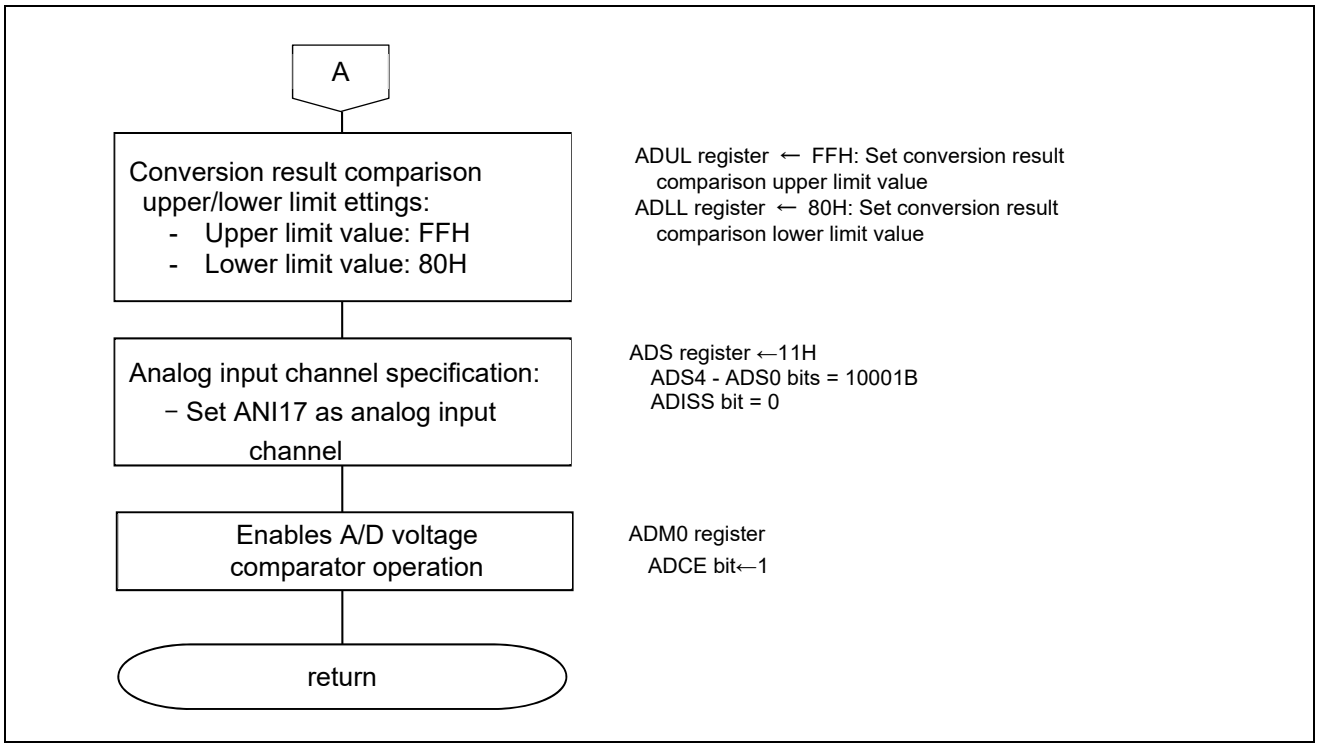


Figure 5.11 A/D Converter Initial Setting (2/2)

Reset of A/D converter

- Peripheral reset control register 0 (PRR0)

Reset of the A/D converter.

Symbol: PRR0

7	6	5	4	3	2	1	0
0	0	ADCRES	0	0	SAU0RES	0	TAU0RES
0	0	**1**	0	0	x	0	x

Bit 5

ADCRES	Reset control of A/D converter
0	A/D converter reset release
1	**A/D converter reset state**

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

A/D converter clock supply setting

- Peripheral enable register 0 (PER0)

Enable clock supply to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	0	ADCEN	0	0	SAU0EN	0	TAU0EN
x	0	**1**	0	0	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply
1	**Enables input clock supply.**

End of A/D conversion interrupt setting

- Interrupt mask flag register (MK1H)

Set the interrupt mask.

- Interrupt request flag register (IF1H)

Clear the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
0	DOCMK	CMPMK1	CMPMK0	KRMK	TMKAMK	RTCMK	ADMK
0	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: IF1H

7	6	5	4	3	2	1	0
0	DOCIF	CMPIF1	CMPIF0	KRIF	TMKIF	RTCIF	ADIF
0	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

A/D conversion time and operation mode settings

- A/D converter mode register 0 (ADM0)

Control the A/D conversion operation.

Specify the A/D conversion channel selection mode

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
0	**0**	**1**	**1**	**0**	**1**	**0**	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation**
1	Enables conversion operation

Bit 6

ADMD	Specification of A/D channel selection mode
0	**Select mode**
1	Scan mode

Bits 5-1

ADM0					Mode	Conversion Time					Conversion clock (f_{AD})
FR2	FR1	FR0	LV1	LV2		f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	f_{CLK}= 24MHz	
0	0	0	**1**	**0**	**Low-voltage 1**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	101.958µs	f_{CLK}/32
0	0	1							76.9375µs	51.292µs	**f_{CLK}/16**
0	1	0						77.875µs	38.9375µs	25.958µs	f_{CLK}/8
0	1	1						58.875µs	29.4375µs	19.625µs	f_{CLK}/6
1	0	0						49.375µs	24.6875µs	16.458µs	f_{CLK}/5
1	0	1					79.75µs	39.875µs	19.9375µs	13.292µs	f_{CLK}/4
1	1	0					41.75µs	20.875µs	10.4375µs	6.958µs	f_{CLK}/2
1	**1**	**1**				91µs	22.75µs	**11.375µs**	5.6875µs	Setting prohibited	**f_{CLK}/1**

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D enables comparator operation**
1	Enables A/D voltage comparator operation

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

A/D conversion trigger mode setting

- A/D converter mode register 1 (ADM1)

Select the A/D conversion trigger mode.
Specify the A/D conversion operation mode.
Select hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
1	**1**	**1**	0	0	0	**0**	**1**

Bits 7-6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	x	Software trigger mode
1	0	Hardware trigger no-wait mode
1	**1**	**Hardware trigger wait mode**

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bits 1-0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 01 count or capture interrupt signal (INTTM01)
0	**1**	**Event signal selected by ELC**
1	0	Setting prohibited
1	1	12-bit interval timer interrupt signal (INTIT)

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

Reference voltage source setting

- A/D converter mode register 2 (ADM2)

Selection of the + side reference voltage source of the A/D converter.
Selection of the - side reference voltage source of the A/D converter
Checking the upper and lower limit conversion result values.
Specification of the SNOOZE mode
Selection of the A/D conversion resolution

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
0	**0**	**0**	0	**0**	**0**	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from AV_{DD}**
0	1	Supplied from$P20/AV_{REFP}$/ANI0
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the - side reference voltage source of the A/D converter
0	**Supplied from AV_{SS}**
1	Supplied from $P21/AV_{REFM}$/ANI1

Bit 3

ADRCK	Checking the upper and lower limit conversion result values
0	**The A/D conversion end interrupt request signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register (AREA1).**
1	The A/D conversion end interrupt request signal (INTAD) is output when the ADCR register < the ADLL register (AREA2) or the ADUL register < the ADCR register (AREA3).

Bit 2

AWC	Specification of the SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**12-bit resolution**
1	8-bit resolution

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

Conversion result comparison upper/lower limit settings

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set conversion result comparison upper/lower limit values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

略号：ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

Input channel specification

- Analog input channel specification register (ADS)

Specify the input channel of the analog voltage to be A/D converted.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**1**	**0**	**0**	**0**	**1**

Bits 7, 4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P10/ANI0/AVREFP pin
0	0	0	0	0	1	ANI1	P11/ANI1/AVREFM pin
0	0	0	0	1	0	ANI2	P12/ANI2 pin
0	0	0	0	1	1	ANI3	P13/ANI3 pin
0	0	0	1	0	0	ANI4	P14/ANI4 pin
0	0	0	1	0	1	ANI5	P15/ANI5 pin
0	0	0	1	1	0	ANI6	P16/ANI6 pin
0	0	0	1	1	1	ANI7	P17/ANI7 pin
0	0	1	0	0	0	ANI8	P25/ANI8 pin
0	0	1	0	0	1	ANI9	P24/ANI9 pin
0	0	1	0	1	0	ANI10	P23/ANI10 pin
0	0	1	0	1	1	ANI11	P22/ANI11 pin
0	0	1	1	0	0	ANI12	P21/ANI12 pin
0	0	1	1	0	1	ANI13	P20/ANI13 pin
0	1	0	0	0	0	ANI16	P02/ANI16 pin
0	**1**	**0**	**0**	**0**	**1**	**ANI17**	**P03/ANI17 pin**
0	1	0	1	1	0	ANI18	P04/ANI18 pin
1	0	0	0	0	0	—	Temperature sensor 0 output
1	0	0	0	0	1	—	Internal reference voltage output (1.45 V)
Other than the above						Setting prohibited	

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

5.7.9 DTC Initial Setting

Figure 5.12 to Figure 5.19 show the flowchart for the DTC initial setting.

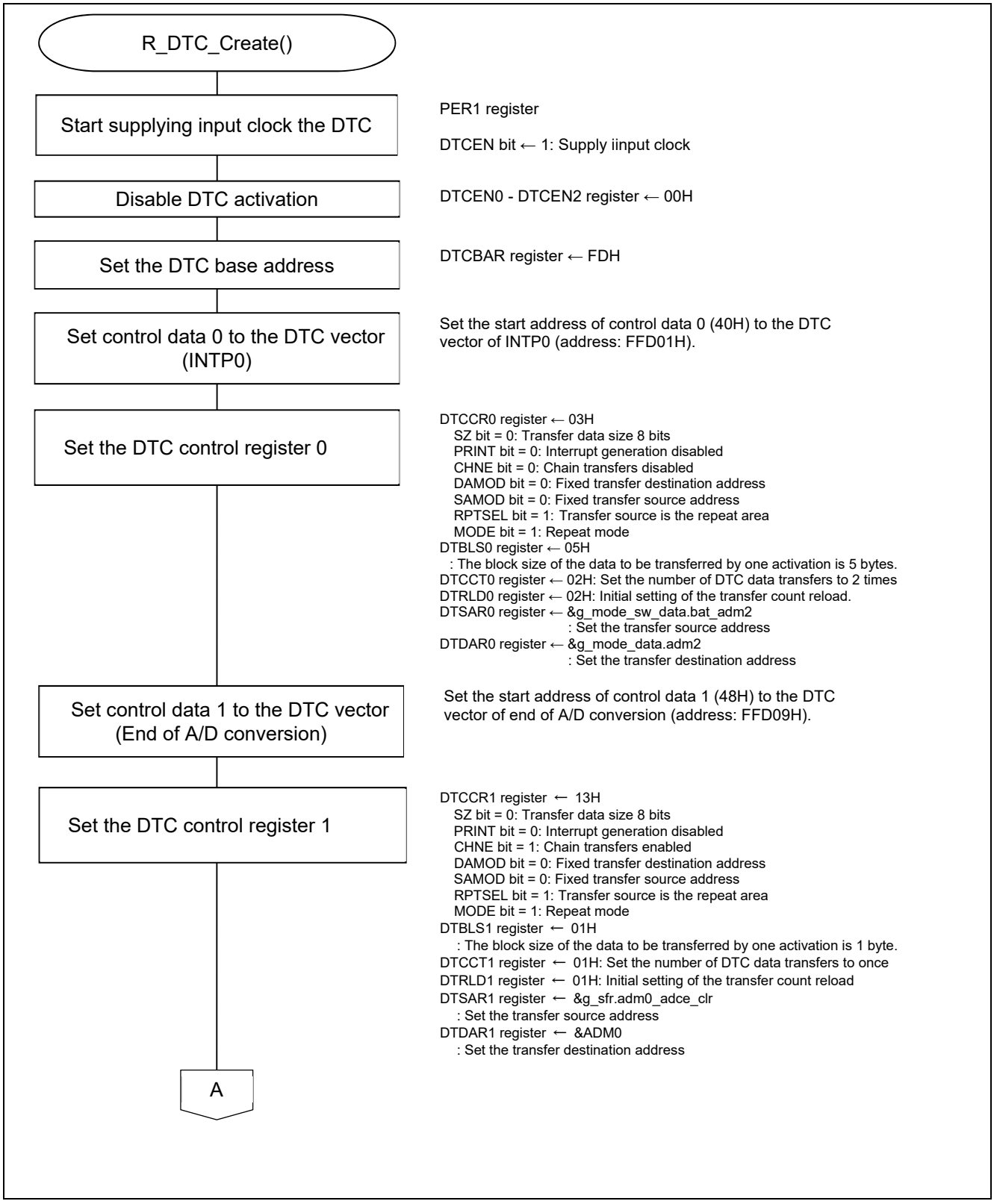


Figure 5.12 DTC Initial Setting (1/8)

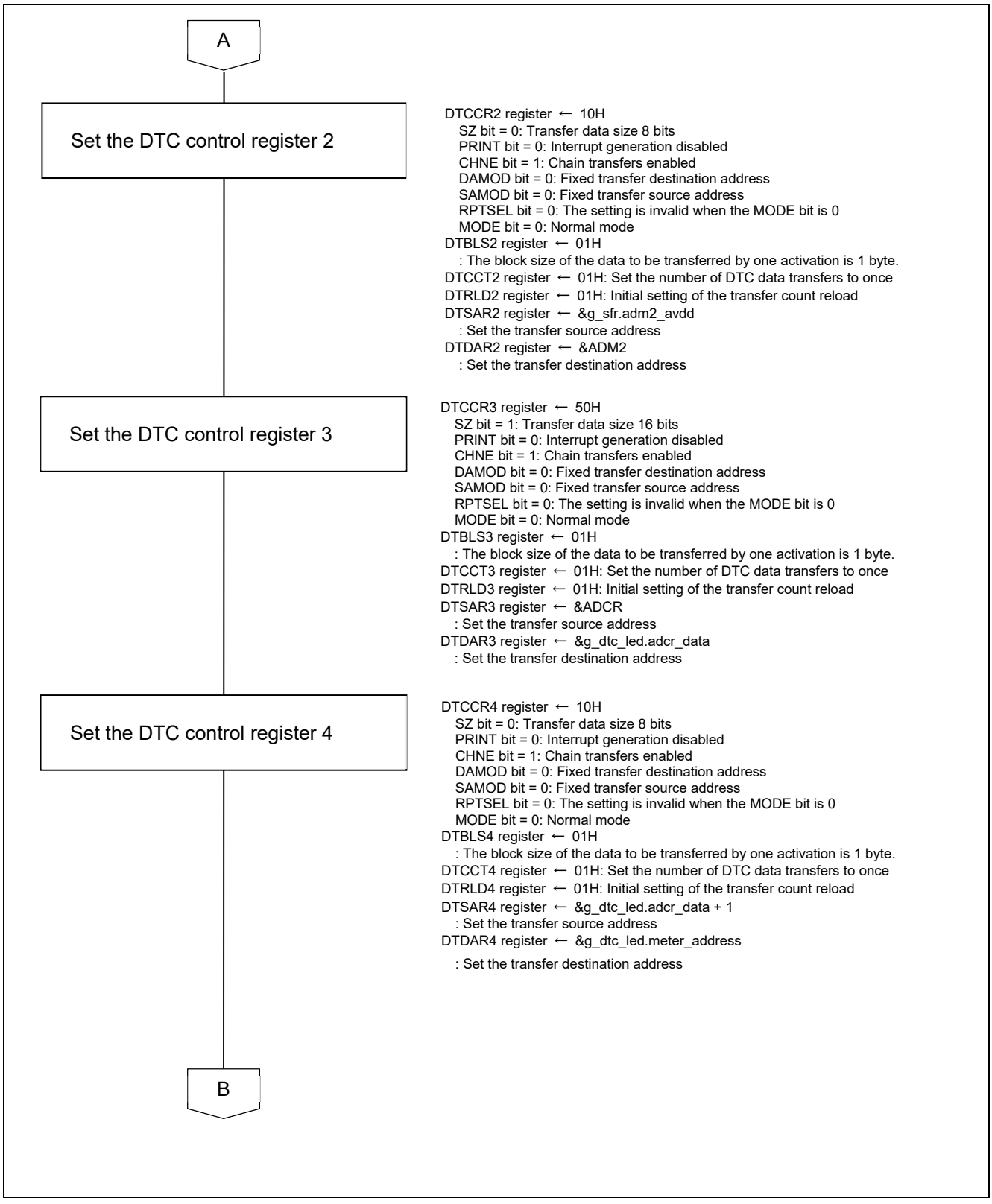


Figure 5.13 DTC Initial Setting (2/8)

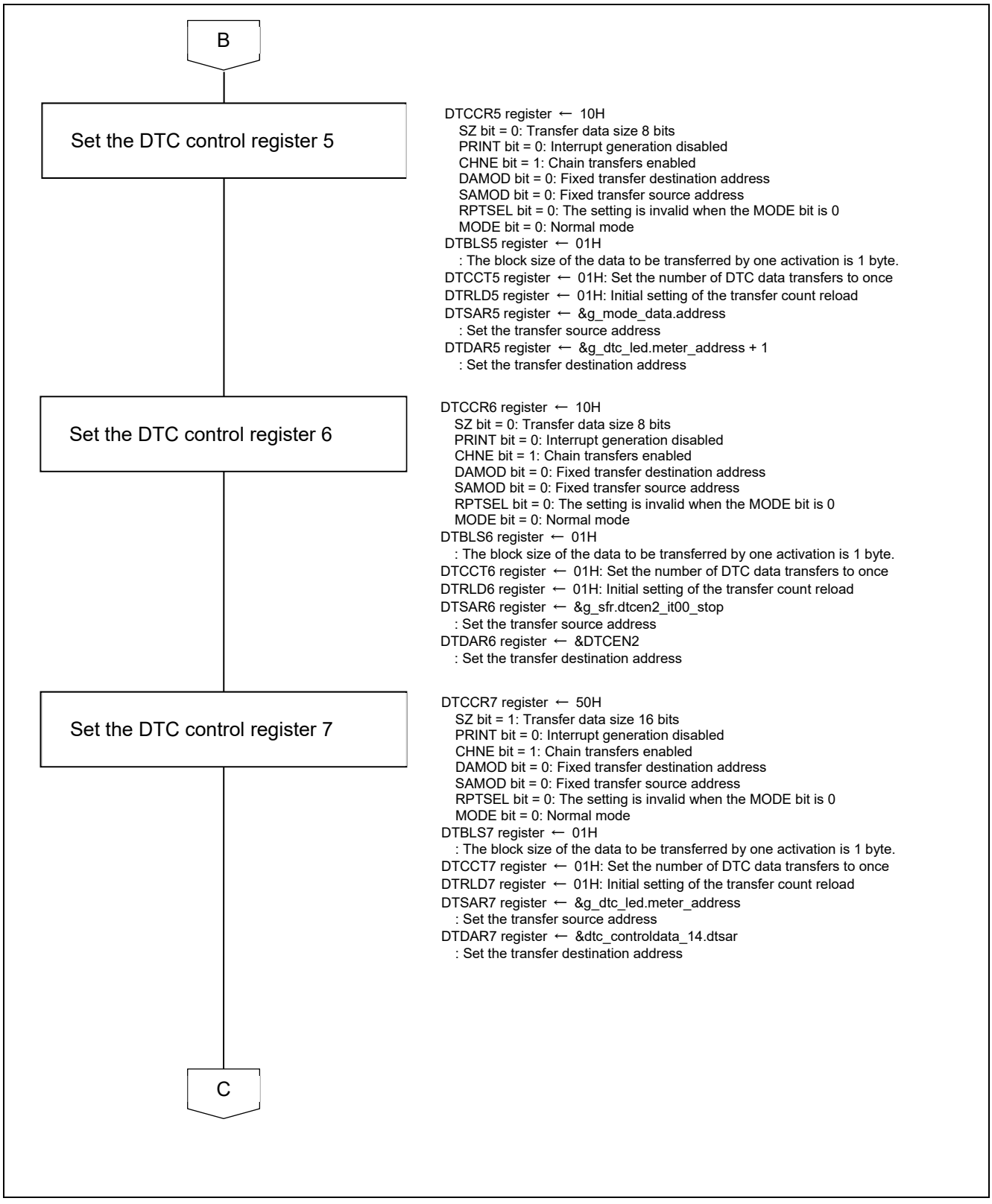


Figure 5.14 DTC Initial Setting (3/8)

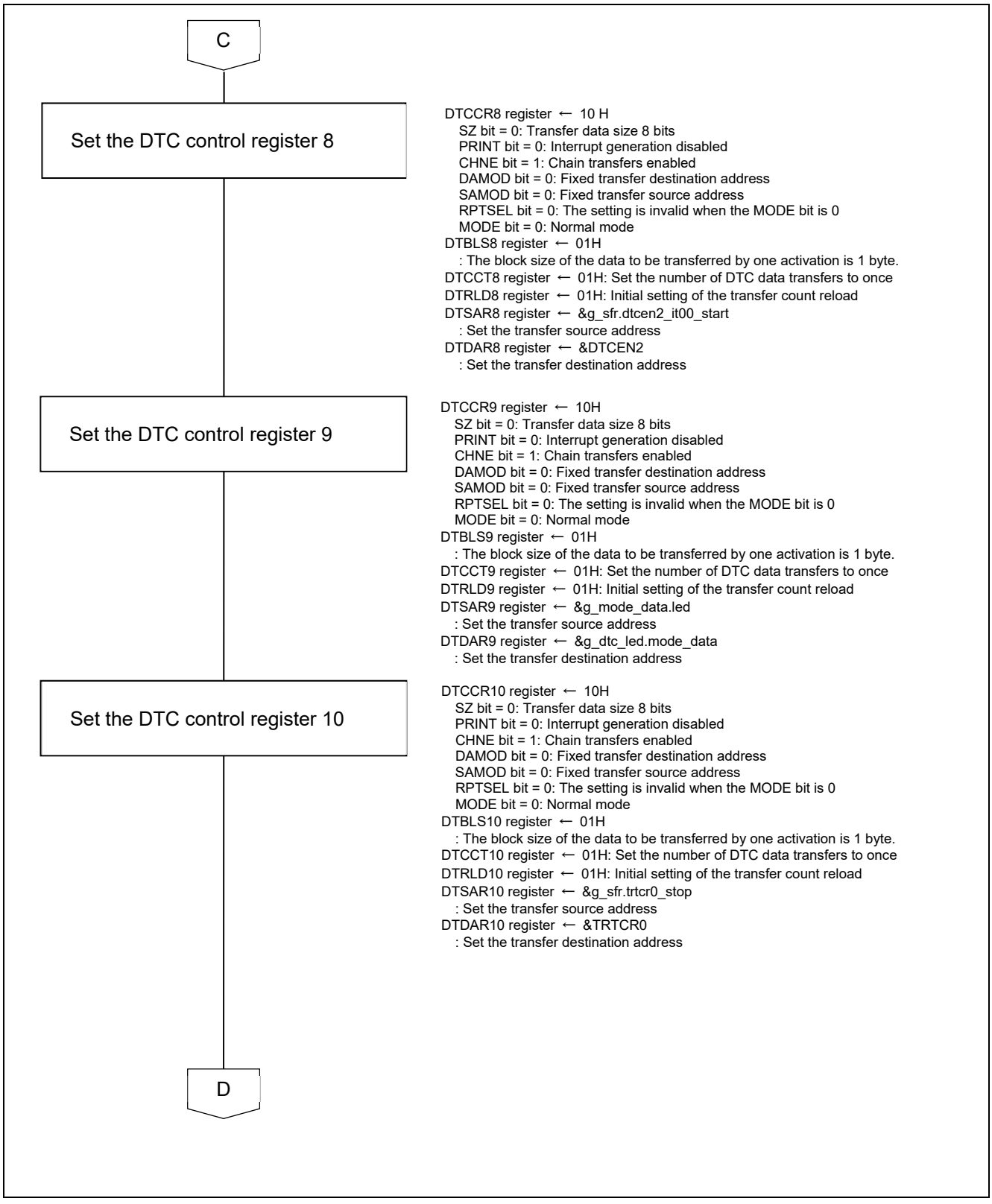


Figure 5.15 DTC Initial Setting (4/8)

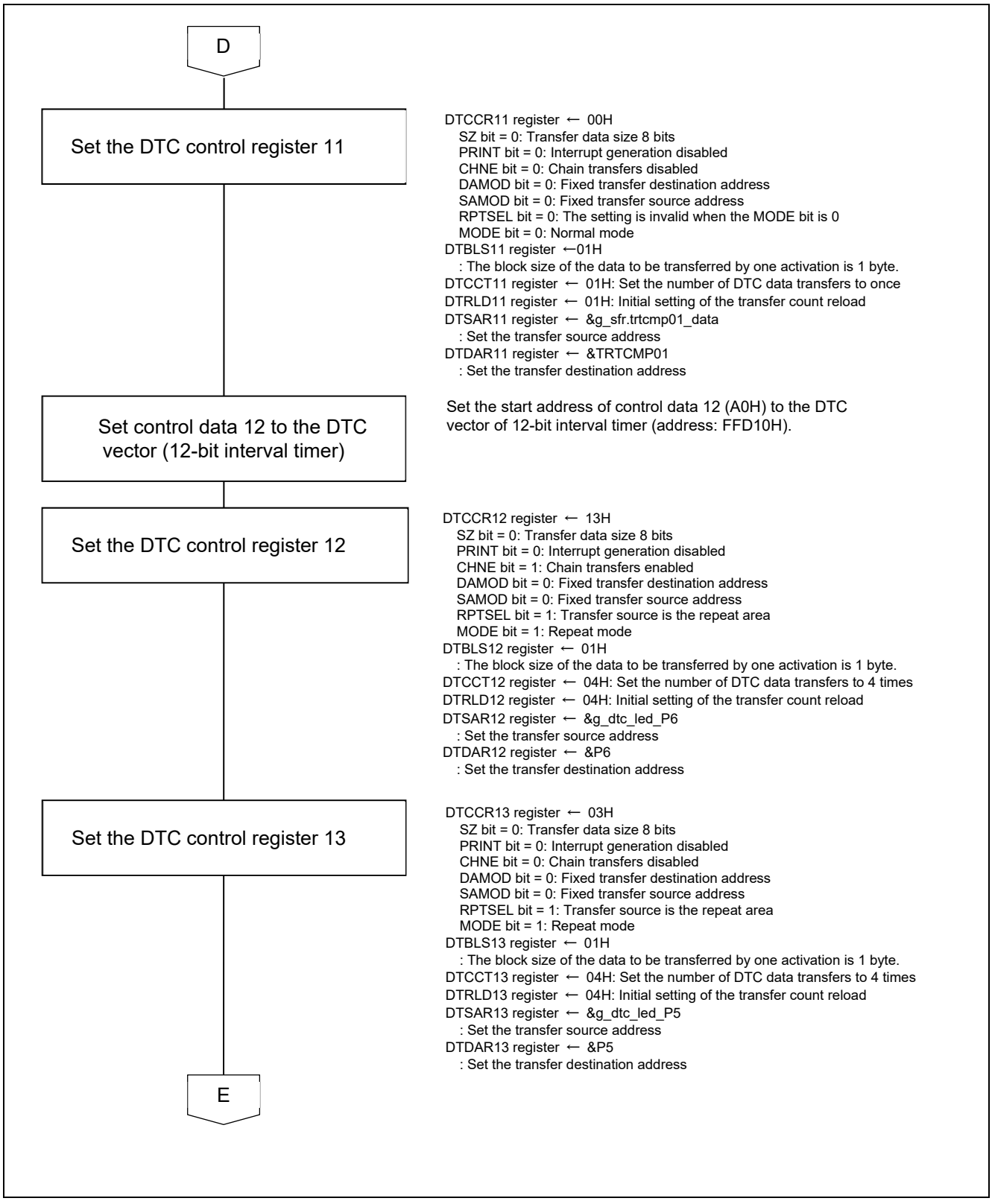


Figure 5.16 DTC Initial Setting (5/8)

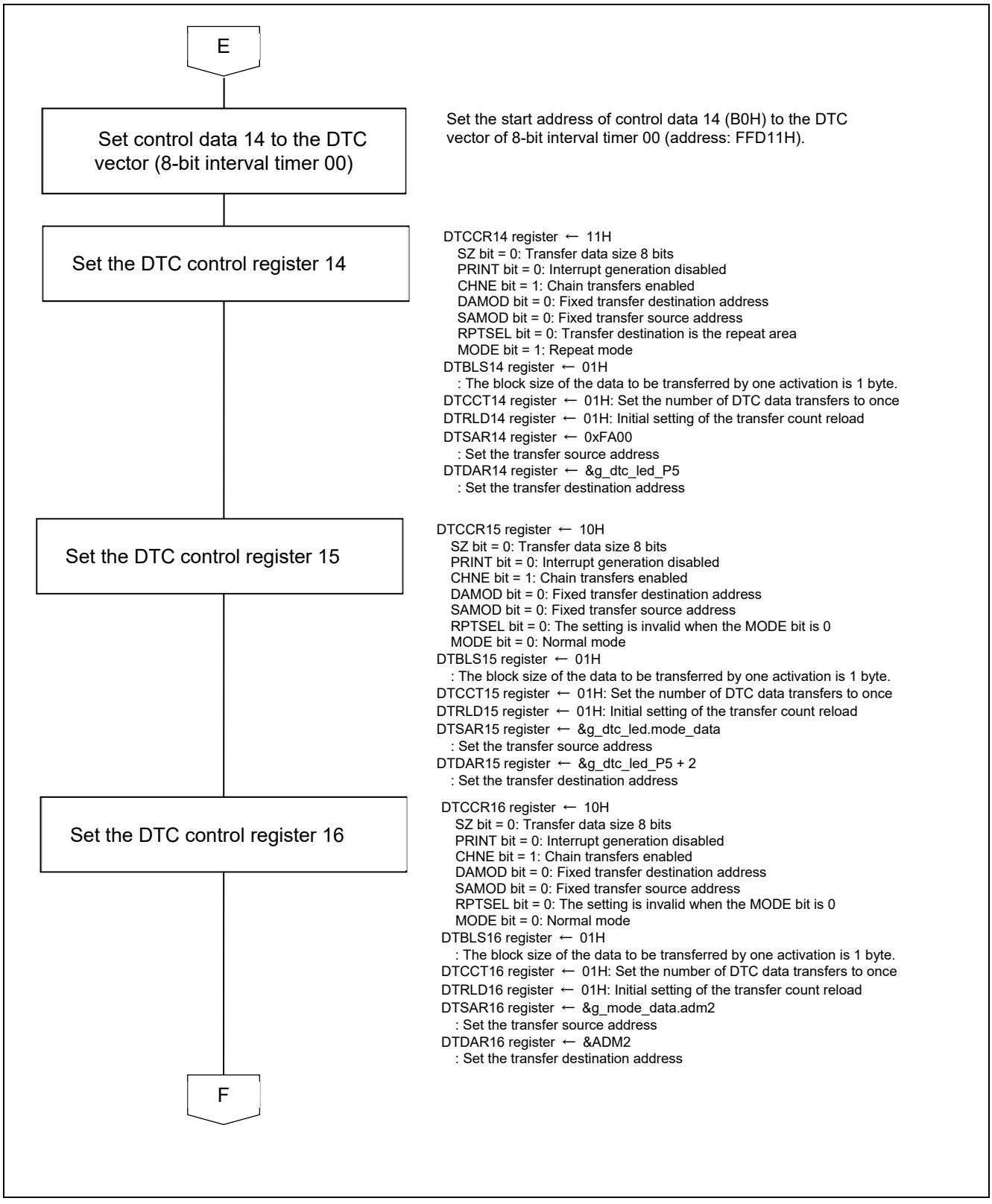


Figure 5.17 DTC Initial Setting (6/8)

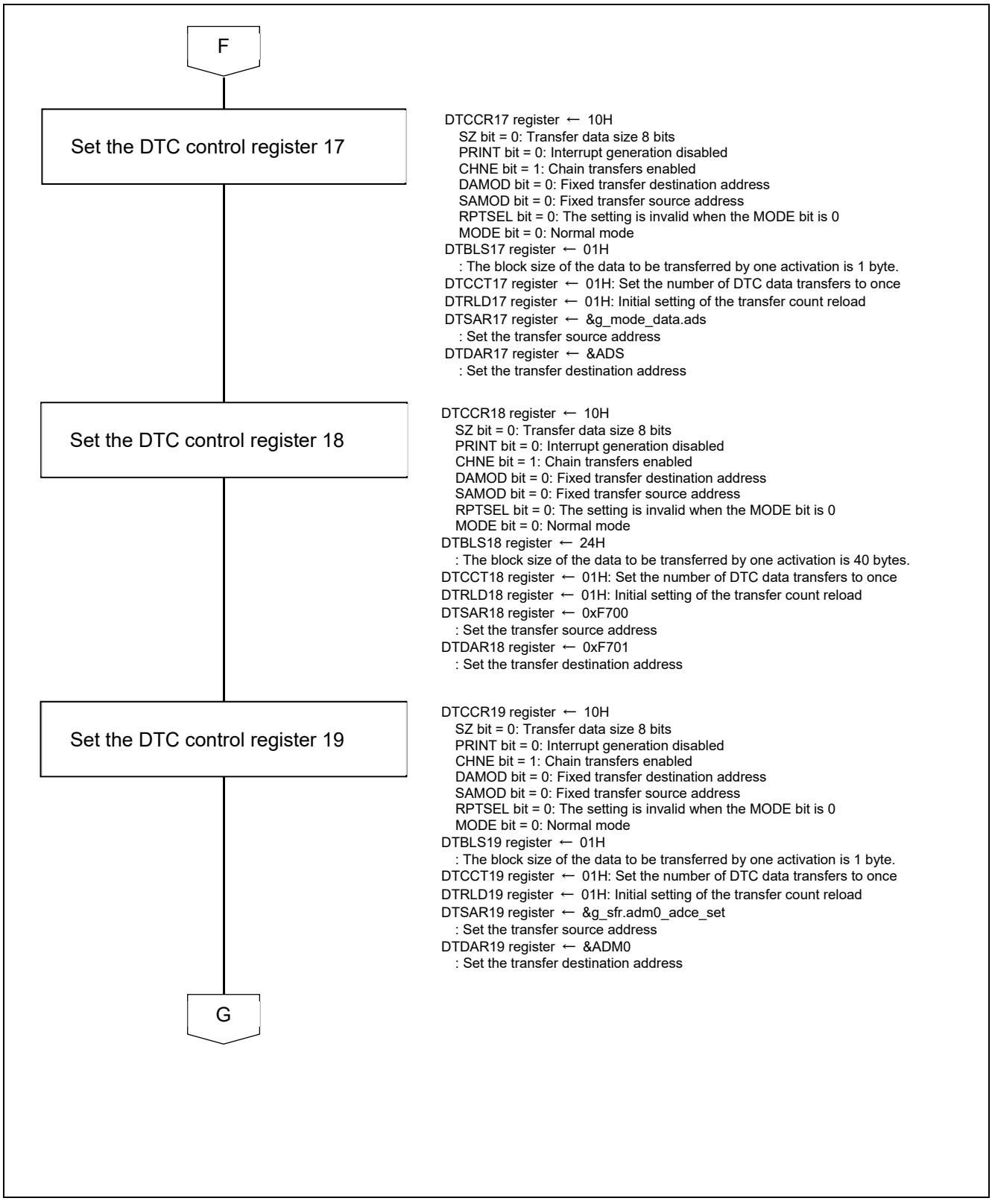


Figure 5.18 DTC Initial Setting (7/8)

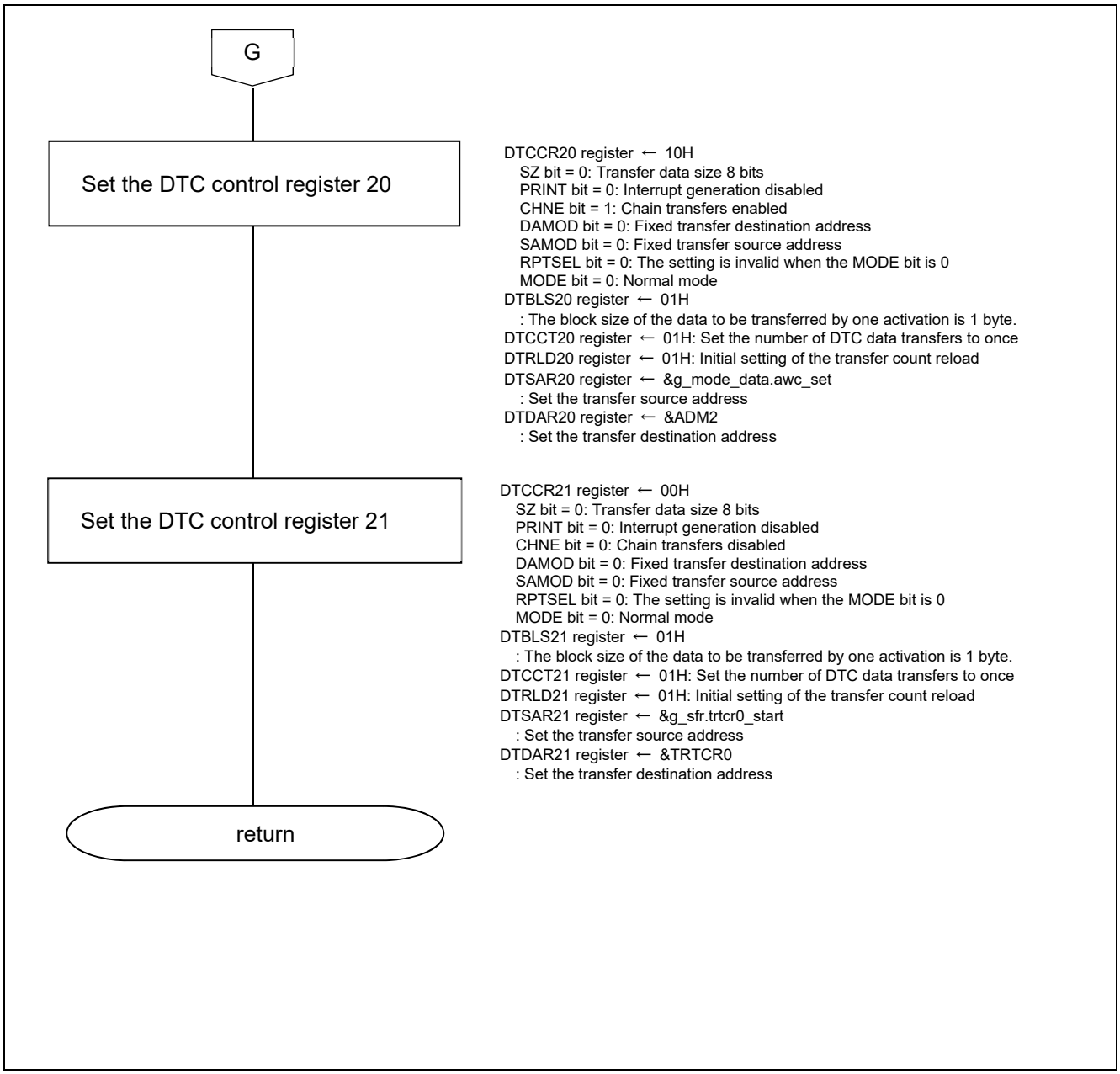


Figure 5.19 DTC Initial Setting (8/8)

DTC clock supply start

- Peripheral enable register 1 (PER1)

Start clock supply to the DTC.

Symbol: PER1

7	6	5	4	3	2	1	0
0	0	CMPEN	0	DTCEN	0	0	0
0	0	x	0	**1**	0	0	0

Bit 3

DTCEN	Control of DTC input clock
0	Stops input clock supply.
1	**Supplies input clock.**

DTC activation disabling

- DTC activation enable register i (DTCENi) (i = 0 to 2)

Disable DTC activation.

Symbol: DTCENi

7	6	5	4	3	2	1	0
DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7-0 (The below table shows the format of the bit 7 as an example. (The formats of the bits 7 to 0 are same.))

DTCENi7	DTC activation enable i7
0	**Activation disabled**
1	Activation enabled

DTC base address

- DTC base address register (DTCBAR)

Set the DTC base address to “FDH”.

Symbol: DTCBAR

7	6	5	4	3	2	1	0
DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0
1	**1**	**1**	**1**	**1**	**1**	**0**	**1**

Note: Refer to the RL78/I1D User’s Manual (Hardware version) for details on how to set registers.

DTC control register 0 setting

- DTC control register 0 (DTCCR0)

Set to 8 bits (data size), repeat mode (transfer mode).

Symbol: DTCCR0

7	6	5	4	3	2	1	0
0	SZ	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Bit 6

SZ	Data size selection
0	**8 bits**
1	16 bits

Bit 5

RPTINT	Enabling/disabling repeat mode interrupts
0	**Interrupt generation disabled**
1	Interrupt generation enabled
The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).	

Bit 4

CHNE	Enabling/disabling chain transfers
0	**Chain transfers disabled**
1	Chain transfers enabled
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).	

Bit 3

DAMOD	Transfer destination address control
0	**Fixed**
1	Incremented
The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).	

Bit 2

SAMOD	Transfer source address control
0	Fixed
1	Incremented
The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).	

Bit 1

RPTSEL	Repeat area selection
0	Transfer destination is the repeat area.
1	**Transfer source is the repeat area.**

Bit 0

MODE	Transfer mode selection
0	Normal mode
1	**Repeat mode**

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

DTC block size register 0 setting

- DTC blobk size register 0 (DTBLS0)

Set the block size to 5 bytes.

Symbol: DTBLS0

7	6	5	4	3	2	1	0
DTBLS07	DTBLS06	DTBLS05	DTBLS04	DTBLS03	DTBLS02	DTBLS01	DTBLS00
0	**0**	**0**	**0**	**0**	**1**	**0**	**1**

DTBLS0	Transfer block size	
	8-bit transfer	16-bit transfer
00H	256 bytes	512 bytes
01H	1 byte	2 bytes
02H	2 bytes	4 bytes
03H	3 bytes	6 bytes
.	.	.
05H	**5 bytes**	.
.	.	.
FDH	253 bytes	506 bytes
FEH	254 bytes	508 bytes
FFH	255 bytes	510 bytes

DTC transfer count register 0 setting

- DTC transfer count register 0 (DTCCT0)

Set the number of DTC data transfer to 2 times.

Symbol: DTCCT0

7	6	5	4	3	2	1	0
DTCCT07	DTCCT06	DTCCT05	DTCCT04	DTCCT03	DTCCT02	DTCCT01	DTCCT00
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**

DTCCT0	Number of transfers
00H	256 times
01H	Once
02H	**2 times**
03H	3 times
.	.
.	.
.	.
FDH	253 times
FEH	254 times
FFH	255 times

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

DTC transfer count reload register 0 setting

- DTC transfer count reload register 0 (DTRLD0)

Set the transfer reload count to 2 times.

Symbol: DTRLD0

7	6	5	4	3	2	1	0
DTRLD07	DTRLD06	DTRLD05	DTRLD04	DTRLD03	DTRLD02	DTRLD01	DTRLD00
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**

DTC source address register 0 setting

- DTC source address register 0 (DTSAR0)

Set the transfer destination address to “F800H”.

Symbol: DTSAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTSAR0 15	DTSAR0 14	DTSAR0 13	DTSAR0 12	DTSAR0 11	DTSAR0 10	DTSAR0 9	DTSAR0 8	DTSAR0 7	DTSAR0 6	DTSAR0 5	DTSAR0 4	DTSAR0 3	DTSAR0 2	DTSAR0 1	DTSAR0 0
1	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

DTC destination address register 0 setting

- DTC destination address register 0 (DTDAR0)

Set the transfer source address to “F30AH”.

Symbol: DTDAR0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTDAR0 15	DTDAR0 14	DTDAR0 13	DTDAR0 12	DTDAR0 11	DTDAR0 10	DTDAR0 9	DTDAR0 8	DTDAR0 7	DTDAR0 6	DTDAR0 5	DTDAR0 4	DTDAR0 3	DTDAR0 2	DTDAR0 1	DTDAR0 0
1	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

Note: Refer to the RL78/I1D User’s Manual (Hardware version) for details on how to set registers.

5.7.10 ELC Initial Setting

Figure 5.20 shows the flowchart of the ELC initial setting.

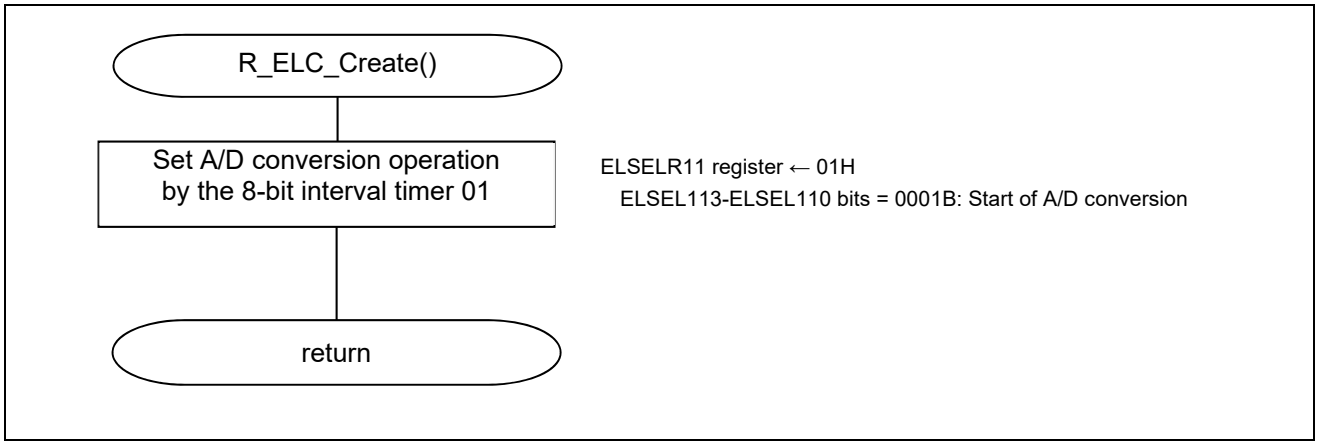


Figure 5.20 ELC Initial Setting

A/D conversion setting by 8-bit interval timer 01

- Event output destination select register 11 (ELSELR11)

Set operation start of the A/D conversion by compare match of the 8-bit interval timer 01.

略号：ELSELR11

7	6	5	4	3	2	1	0
0	0	0	0	ELSEL113	ELSEL112	ELSEL111	ELSEL110
0	0	0	0	**0**	**0**	**0**	**1**

Bits 3-0

Bit 3	Bit 2	Bit 1	Bit 0	Event link selection of 8-bit interval timer 01 selection
0	0	0	0	Event link disabled
0	**0**	**0**	**1**	**Peripheral function to link: A/D converter Operation at event acceptance: Start of A/D conversion**
0	0	1	0	Select operation of peripheral function 2 to link
0	0	1	1	Select operation of peripheral function 3 to link
0	1	0	0	Select operation of peripheral function 4 to link
0	1	0	1	Select operation of peripheral function 5 to link
0	1	1	0	Select operation of peripheral function 6 to link
0	1	1	1	Select operation of peripheral function 7 to link
Other than above				Setting prohibited

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

5.7.11 External Interrupt Initial Setting

Figure 5.21 shows the flowchart of the external interrupt initial setting.

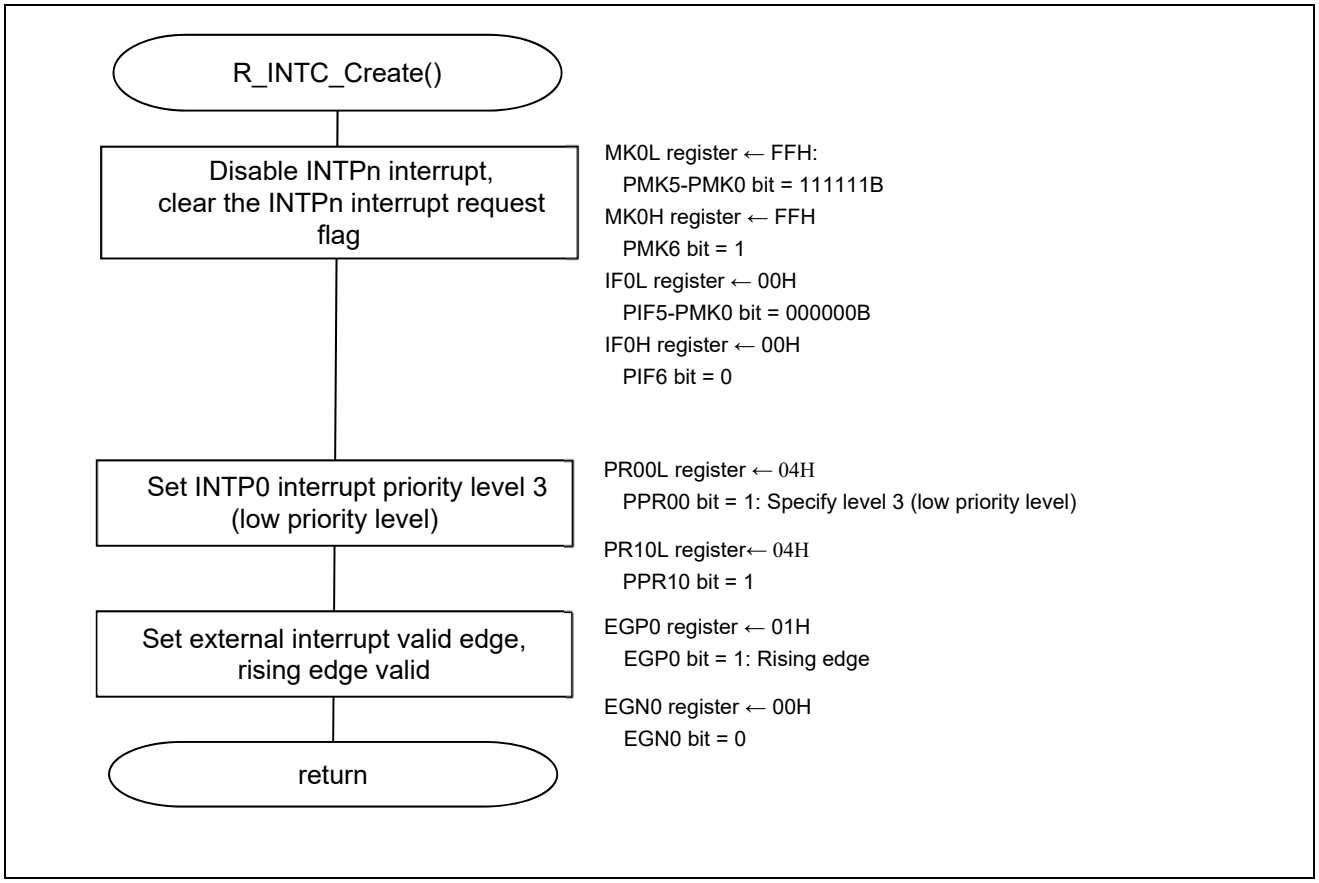


Figure 5.21 External Interrupt Initial Setting

Control of external interrupt valid edge

- External interrupt rising edge enable register (EGP0)

Select valid edge for INTP0 pin: falling edge

Symbol: EGP0

7	6	5	4	3	2	1	0
0	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
0	x	x	x	x	x	x	**1**

Symbol: EGN0

7	6	5	4	3	2	1	0
0	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
0	x	x	x	x	x	x	**0**

Bit 0

EGP1	EGN1	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	**0**	**Rising edge**
1	1	Both rising and falling edges

Note: Refer to the RL78/I1D User's Manual (Hardware version) for details on how to set registers.

5.7.12 Main processing

Figure 5.22 shows the flowchart of the main processing.

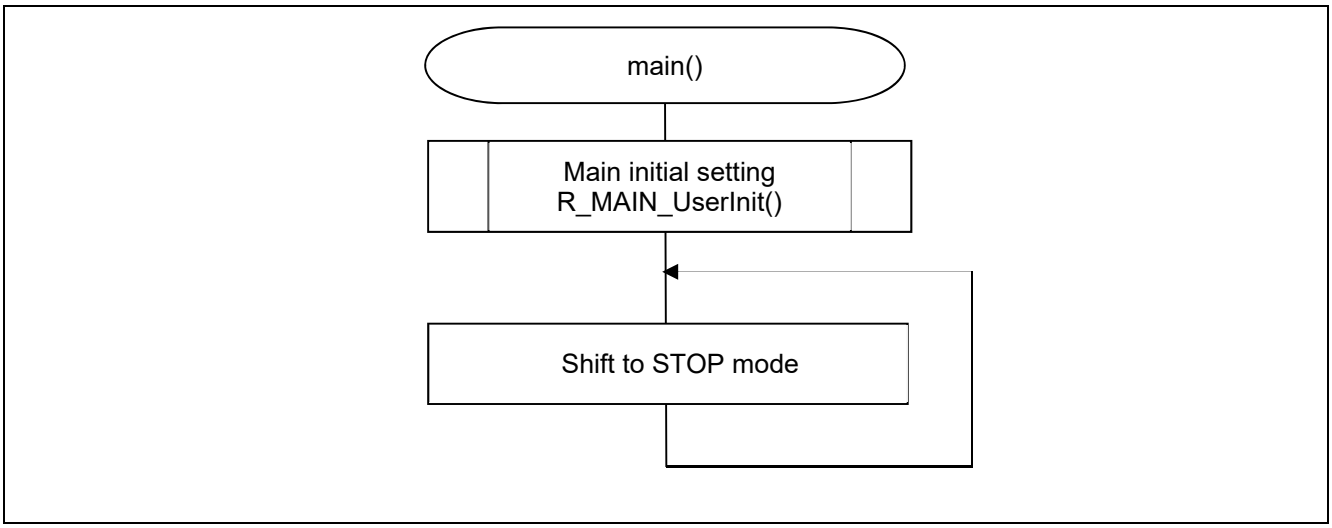


Figure 5.22 Main Processing

5.7.13 Main Initial Setting

Figure 5.23 shows the flowchart for main initial setting.

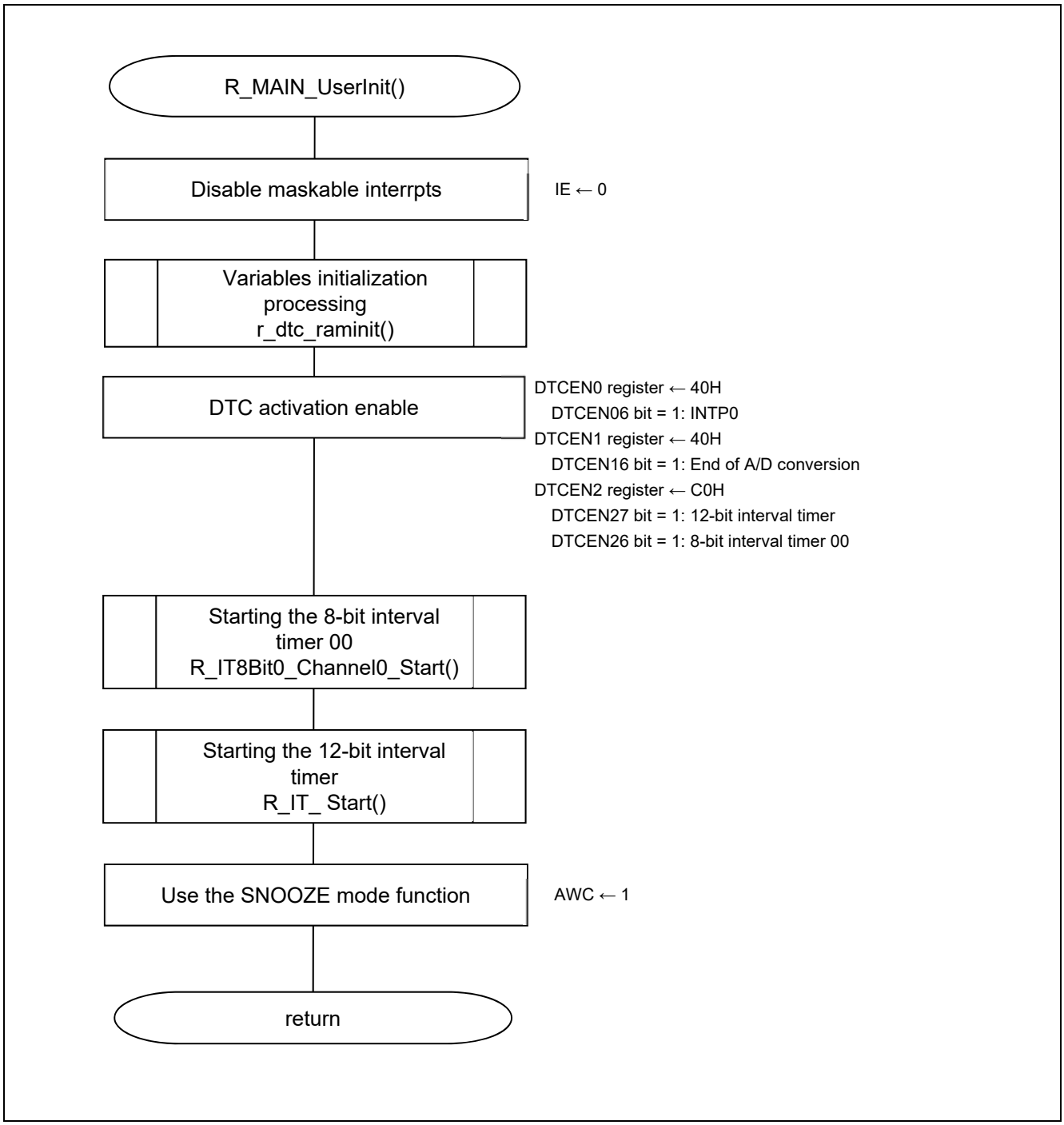


Figure 5.23 Main Initial Setting

5.7.14 Variables Initialization Processing

Figure 5.24 and Figure 5.25 shows the flowchart of the variables initialization processing.

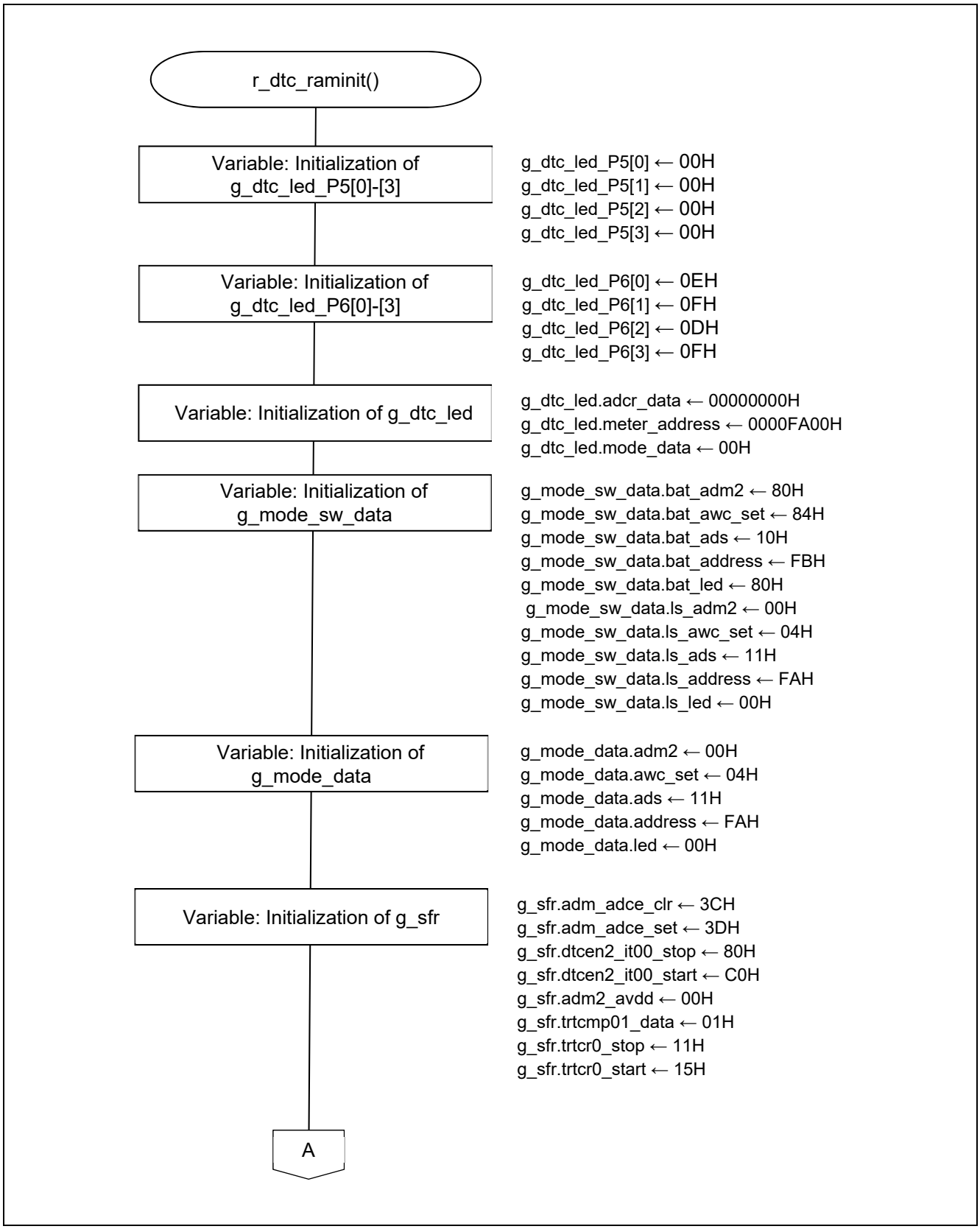


Figure 5.24 Variables Initialization Processing (1/2)

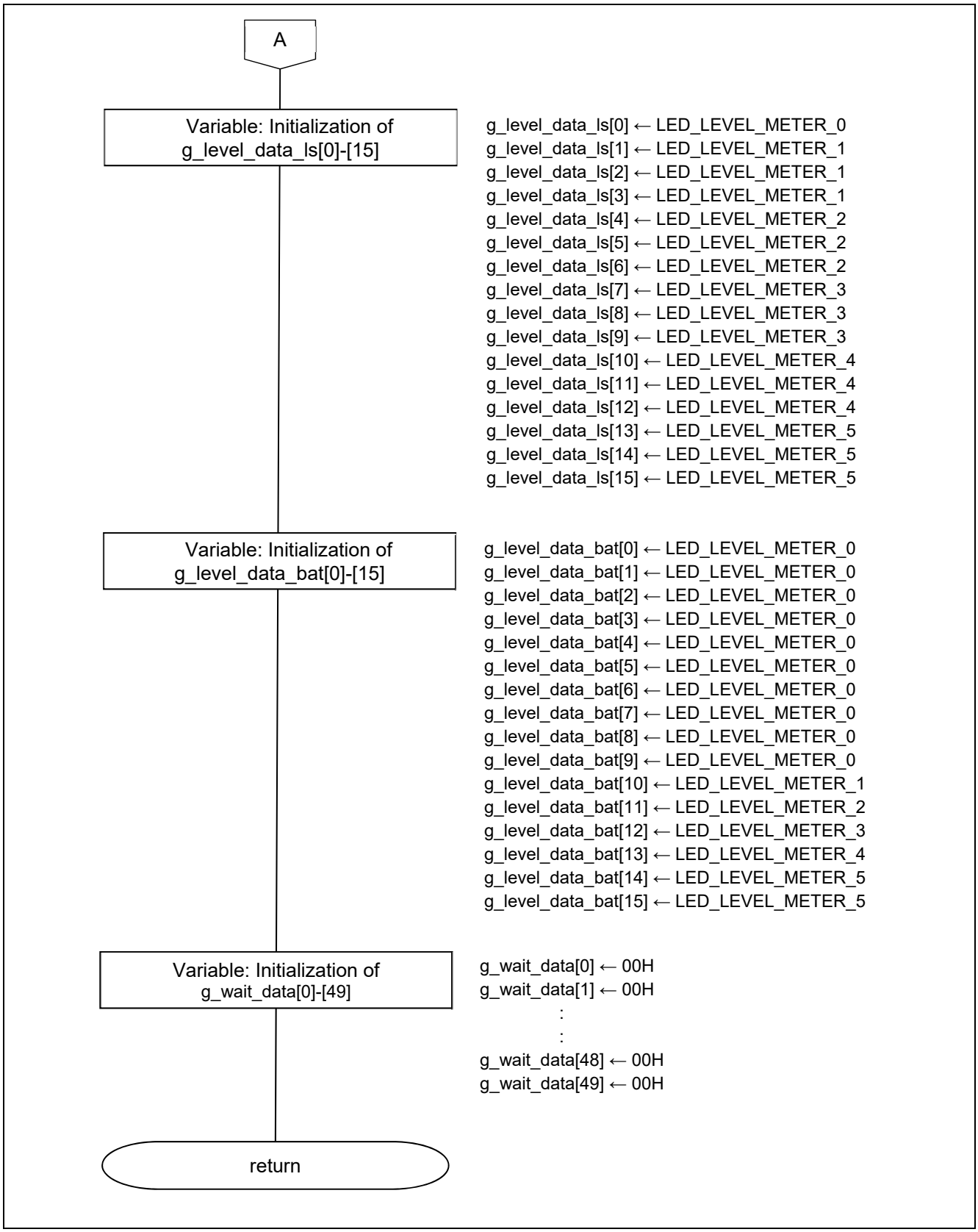


Figure 5.25 Variables Initialization Processing (2/2)

5.7.15 8-bit Interval Timer 00 Count Start

Figure 5.26 shows the flowchart of the 8-bit interval timer 00 count start.

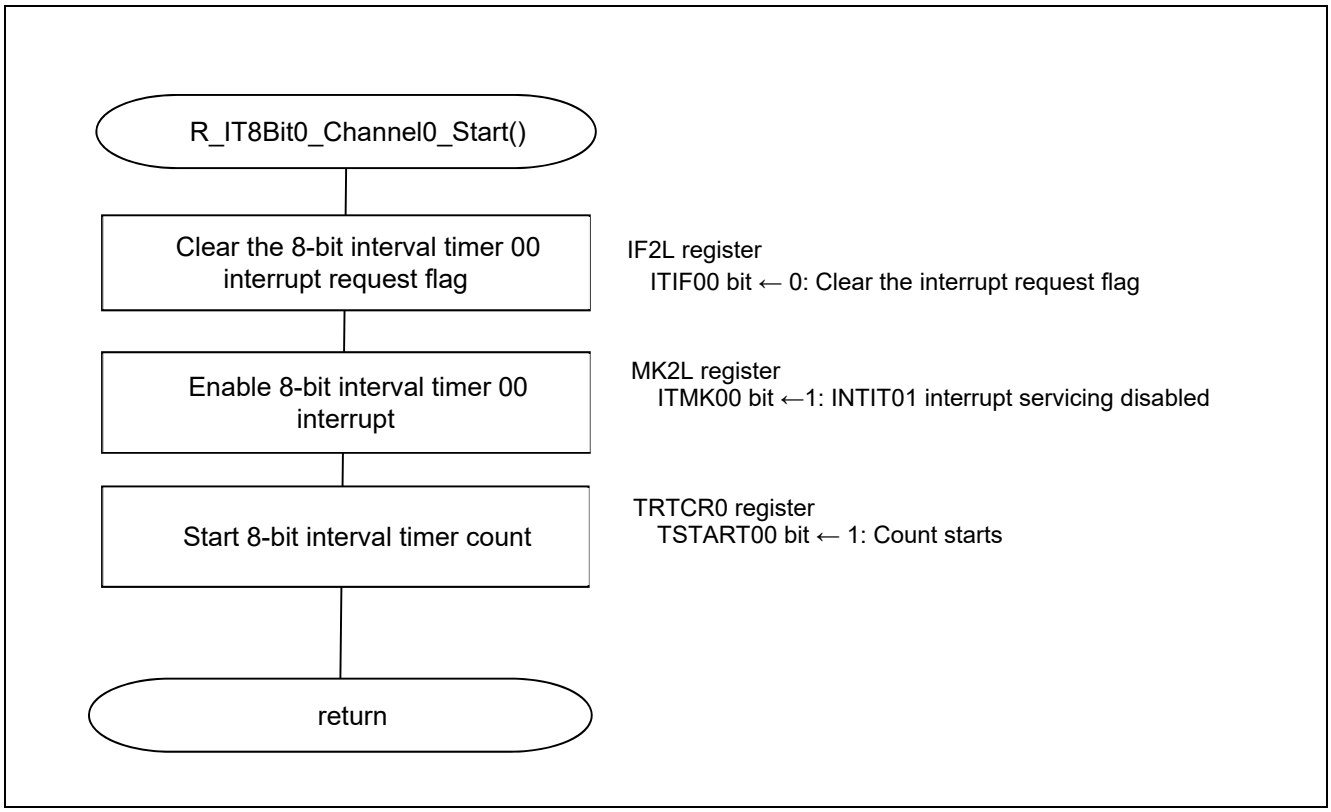


Figure 5.26 8-bit Interval Timer 00 Count Start

5.7.16 12-bit Interval Timer Count Start

Figure 5.27 shows the flowchart of the 12-bit interval timer count start.

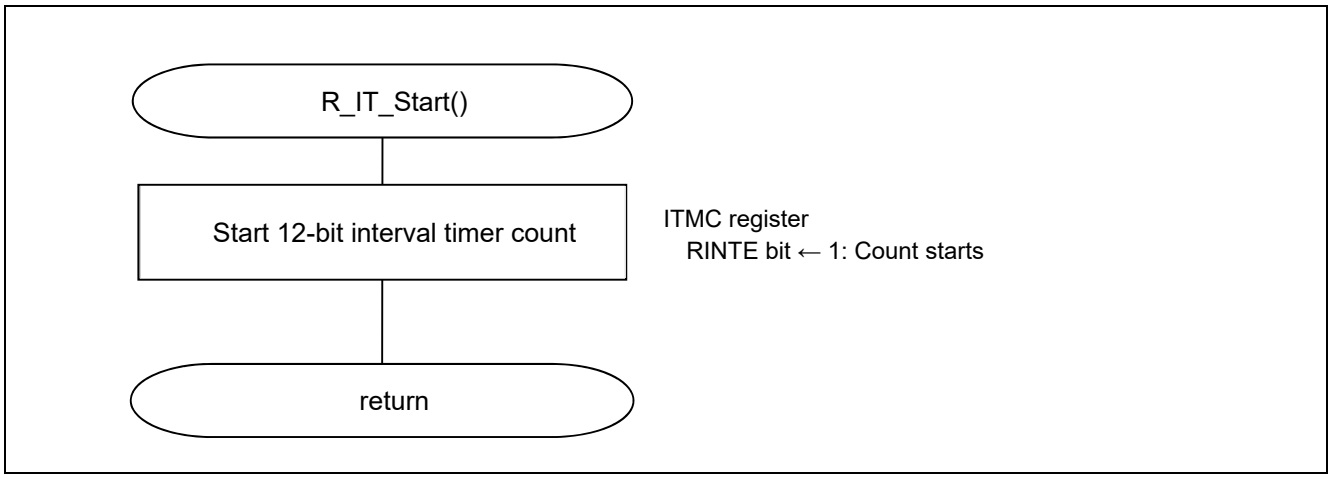


Figure 5.27 12-bit Interval Timer Count Start

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/I1D User's Manual: Hardware (R01UH0474E)

RL78 Family User's Manual: Software (R01US0015E)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Oct. 20, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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California Eastern Laboratories, Inc.
4590 Patrick Henry Drive, Santa Clara, California 95054-1817, U.S.A.
Tel: +1-408-919-2500, Fax: +1-408-988-0279

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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