RL78/G23

40mA Port Output

Introduction

This application note shows an example of using 40mA port output setting function to drive the DC motor directly from the pin by changing the allowable low-level output current.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Specification Outline

In this application note, 40mA port output control register (PTDC) setting changes the allowable low-level output current of P17 from 20mA to 40mA.

Table 1.1 shows the peripheral function to be used and its use, Table 1.2 shows the operation of the DC motor according to the SW status.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
P17	DC Motor control
P137	Switch Input

Table 1.2 DC Motor operation Status

Status	P137 (SW status)	DC Motor
1	High-level input (Not pushed)	Stop
2	Low-level input (pushed)	Work

1.2 Operation Outline

The operation outline of this application note is shown.

(1) Initial setting of Port.
<Setting Conditions>

- Set SW input P137 pin to input.
- Set DC Motor drive P17 pin to output high (Stop DC motor).

(2) Main processing

- Change the allowable low-level output current of the motor drive control pin P17 from 20mA to 40mA.
- According to SW input P137 pin status, set P17 pin High-level output (DC motor stop) or low-level output (DC motor work).

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2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

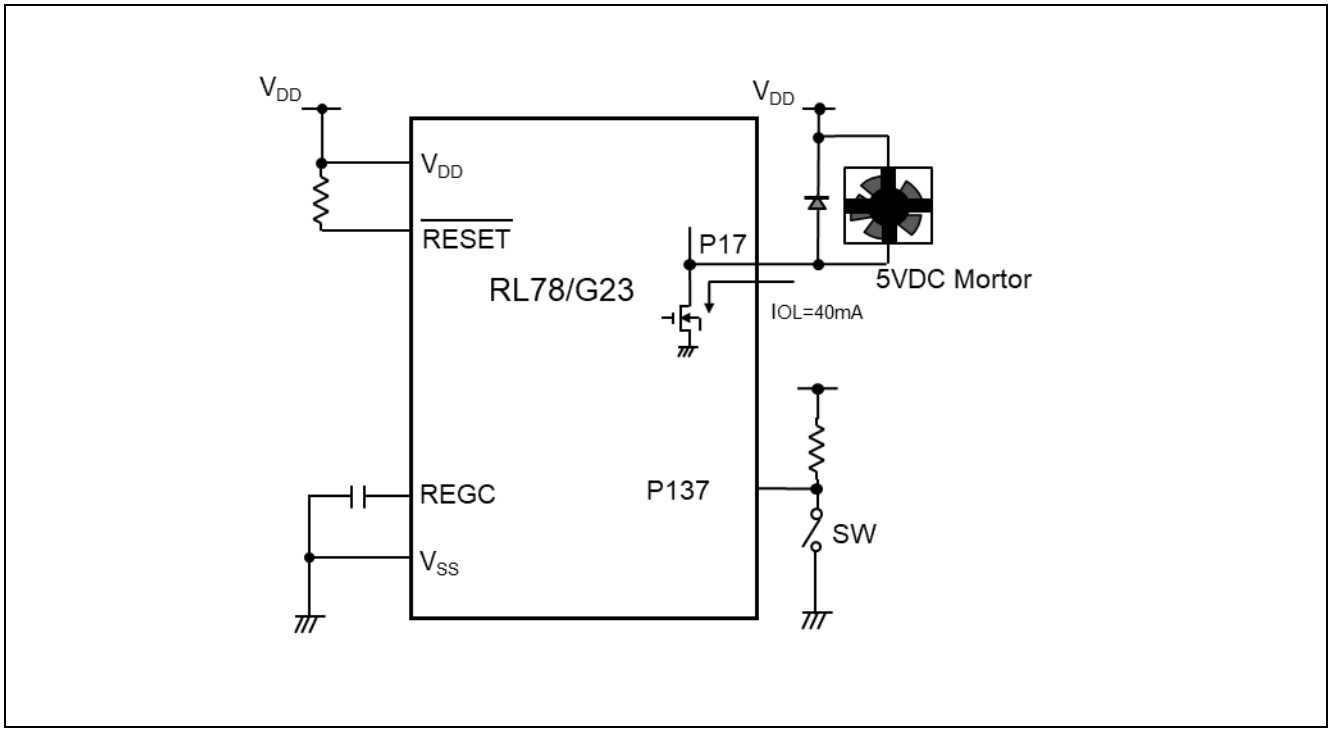
Item	Description
Microcontroller used	RL78/G23 (R7F100GBG3CFP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V LVD operation (V_{LVD}): Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	Renesas Electronics CS+ for CC V8.06.00
C compiler (CS+)	Renesas Electronics CC-RL V1.10.00
Integrated development environment (e^2 studio)	Renesas Electronics e2 studio V2021-10
C compiler (e^2 studio)	Renesas Electronics CC-RL V1.10.00
Integrated development environment (IAR)	IAR Systems IAR Embedded Workbench for Renesas RL78 V4.21.2
C compiler (IAR)	
Smart Configurator	V.1.1.0

3. Hardware

3.1 Hardware Configuration Example

Figure 3.1 shows an example of hardware configuration that is used for this application note.

Figure 3.1 Hardware Configuration



Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

3.2 List of Pins to be Used

Figure 3.2 lists the pins to be used and their function.

Figure 3.2 Pins to be Used and their Functions

Pin Name	I/O	Description
P17/EO17/CCD01/TI02/TO02/(TxD0)	Output	DC Motor control pin
P137/EI137/INTP0	Input	SW input pin

Caution: In this application note, only the used pin is properly connected. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met.

4. Software

4.1 List of Option Byte Settings

Table 4.1summarizes the settings of the option bytes.

Table 4.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	11111110B	LVD operation: Reset mode. At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H/010C2H	11101000B	HS mode, High-speed on-chip oscillator (HOCO) clock: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

4.2 List of Constants and Variables

No constants are variables are used.

4.3 List of Functions

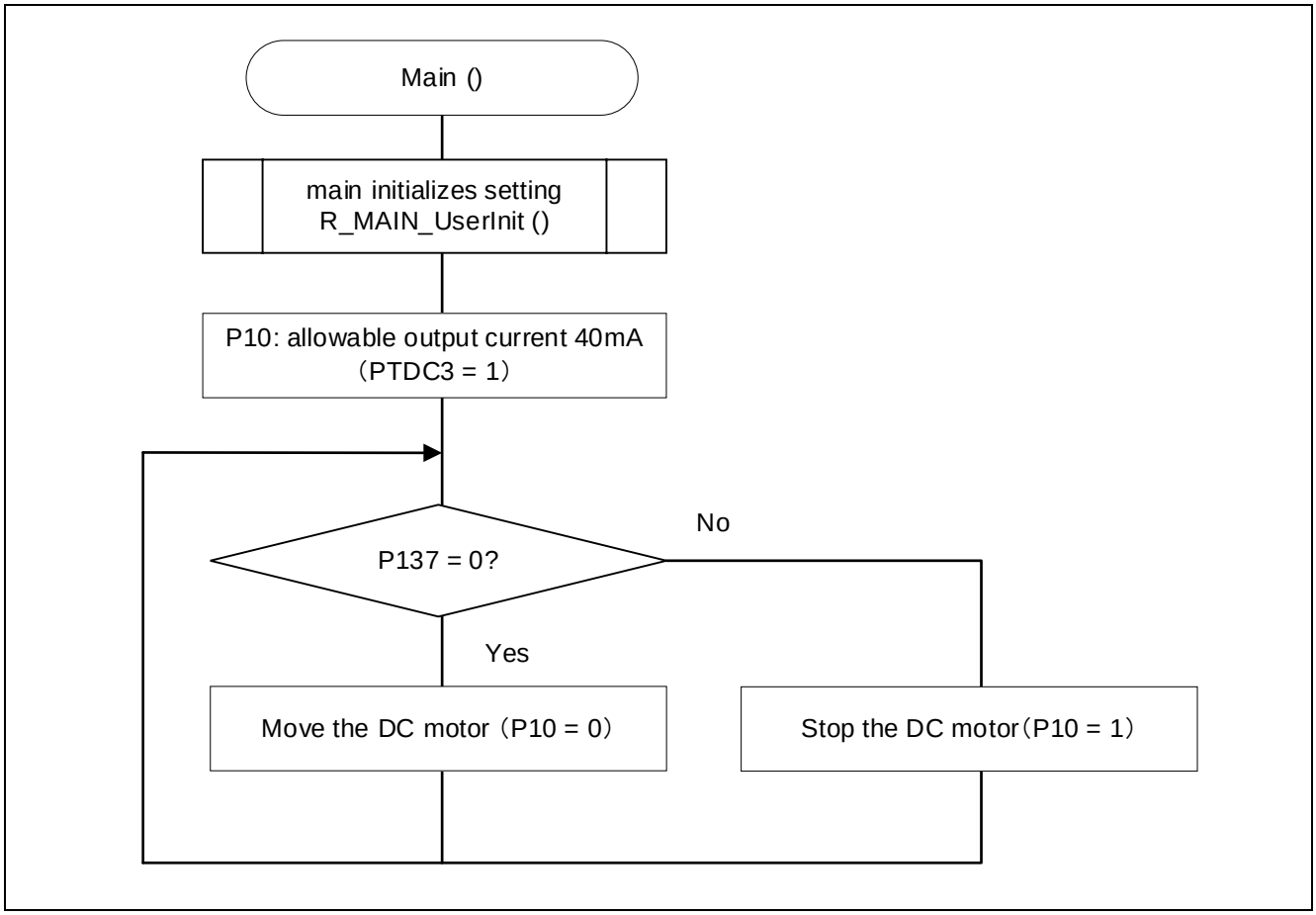
Only the main function except the initial settings.

4.4 Flowcharts

4.4.1 Main Function

Figure 4.1 show the flowchart for the main function.

Figure 4.1 Main Function



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896)
RL78 family User's Manual: Software (R01US0015)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.21	—	First Edition
2.00	Oct.25.21	Page4	TOOL Version Update
		Page6	Change Option Byte Value 0x6EFEE8→0xEFFEE8

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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