RL78/G14

Operation in Conjunction with Three Combined Events Using the ELC CC-RL

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Abstract

This document describes a method to mutually connect (link) the external interrupt (hereinafter called INTP0), timer array unit 0 (hereinafter called TAU0), and A/D converter using the RL78/G14 event link controller (hereinafter called ELC).

Product

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

The following operation is performed using the ELC without going through the CPU. A 2 ms count is started in TAU0 channel 0 (hereinafter called TAU00) at the rising edge input to the P137/INTP0 pin. After the count is completed, input voltage of the P20/ANI0 pin is A/D converted by the A/D converter and the converted result is stored to RAM.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows the Operation Overview.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
ELC	Connect (link) INTP0, TAU00, and the A/D converter.
External interrupt	Detect an external interrupt edge.
Timer array unit	Measure the A/D converter start timing.
A/D converter	Perform A/D conversion on analog input voltage.

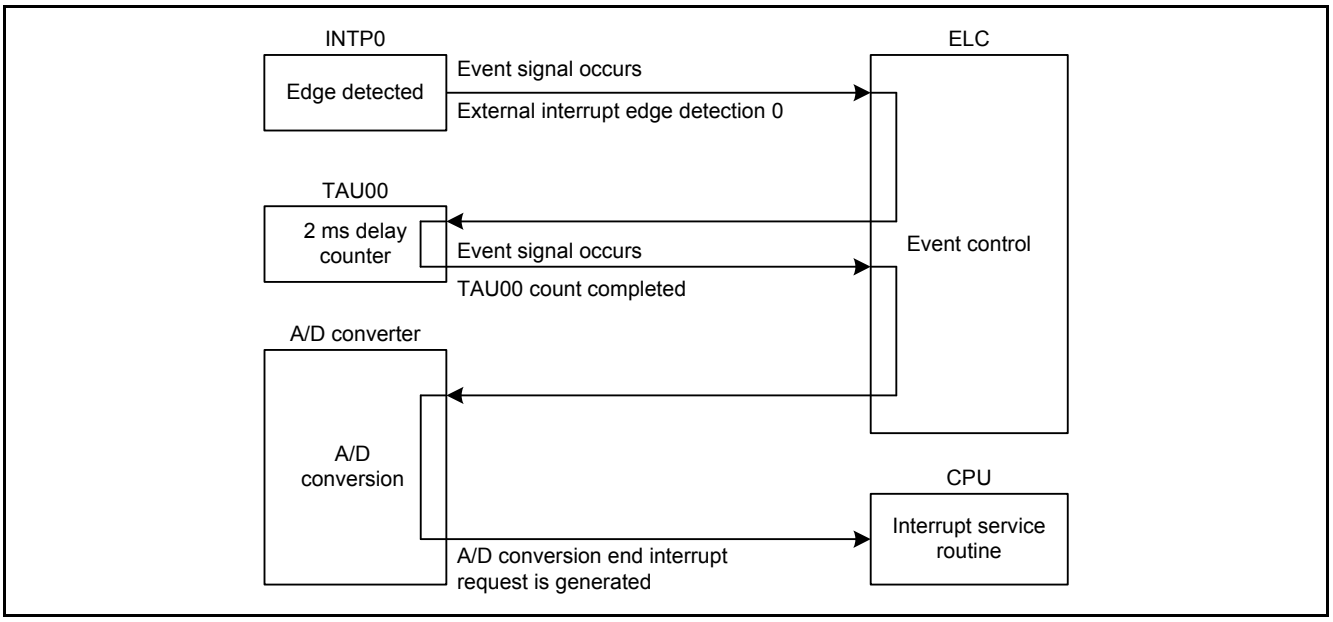


Figure 1.1 Operation Overview

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 64 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 32 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVD}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment (CS+)	Renesas Electronics Corporation CS+ V3.01.00
C compiler (CS+)	Renesas Electronics Corporation CC-RL V1.01.00
Integrated development environment (e^2 studio)	Renesas Electronics Corporation e^2 studio V4.0.0.26
C compiler (e^2 studio)	Renesas Electronics Corporation CC-RL V1.01.00

3. Reference Application Note

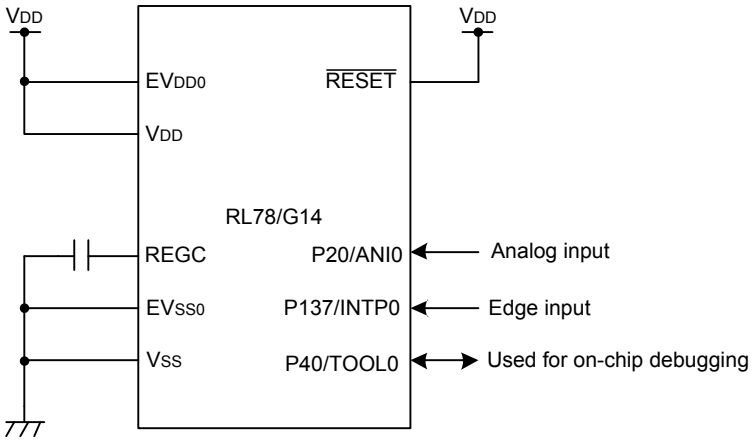
For additional information associated with this document, refer to the following application note.

• RL78/G14 How to Use the ELC for the RL78/G14 (R01AN0862E)

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows the Hardware Configuration used in this document.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics. Connect input-only ports independently to VDD or VSS via resistors.
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVD) specified by the LVD.

Figure 4.1 Hardware Configuration

4.2 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P20/ANI0	Input	Analog input of the A/D converter
P137/INTP0	Input	External interrupt input

5. Software

5.1 Operation Overview

Rising edge input detection to the P137/INTP0 pin is linked to TAU00 as the event generator and TAU00 starts counting 2 ms as the delay counter. Next, count completion of TAU00 is linked to the A/D converter as the event generator, and input voltage of the P20/ANI0 pin is A/D converted. When A/D conversion is completed, an interrupt request is generated, and the A/D converted result is stored to RAM in the interrupt service routine.

Table 5.1 lists the ELC Settings.

Table 5.1 ELC Settings

Event Generator	Link Destination Peripheral Function	Operation When Receiving Event
External interrupt edge detection 0 (INTP0)	TAU00 input source	Count for the delay counter is started
TAU00 count completion (INTTM00)	A/D converter	A/D conversion is started

(1) Perform the initial setting for INTP0, TAU00, and the A/D converter. Set TAU00 for the INTP0 event signal reception, and the A/D converter for the TAU00 event signal reception using the ELC.
(2) When the rising edge of the INTP0 pin is detected, the ELC is activated.
(3) The ELC is linked to TAU00, and TAU00 starts operating as the delay counter.
(4) The ELC is activated after 2 ms.
(5) The ELC is linked to the A/D converter, and the A/D converter starts A/D conversion.
(6) When A/D conversion is completed, an A/D conversion end interrupt request is generated, and the A/D converted result is stored to RAM in the interrupt service routine.
(7) Repeat steps (2) to (6) every time the rising edge is input to the INTP0 pin.

Figure 5.1 shows the Timing Diagram of the ELC and Peripheral Functions.

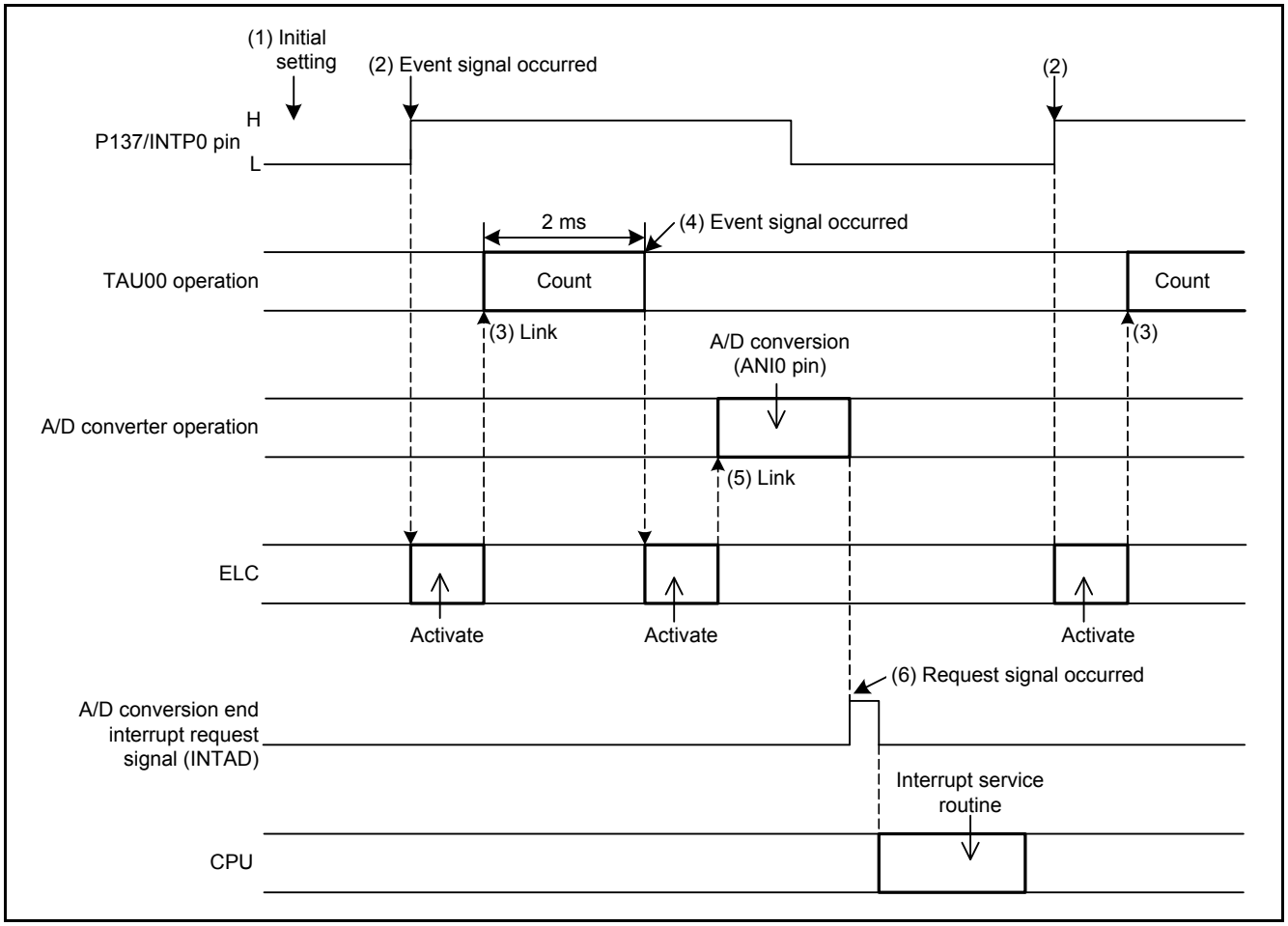


Figure 5.1 Timing Diagram of the ELC and Peripheral Functions

5.2 Option Byte Settings

Table 5.2 lists the Option Byte Settings. When necessary, set a value suited to the user system.

Table 5.2 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11111000B	Internal high-speed oscillation HS mode: 64 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

5.3 Variable

Table 5.3 lists the Global Variable.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
uint16_t	ad_value	A/D converted value	r_adc_Interrupt

5.4 Functions

Table 5.4 lists the Functions.

Table 5.4 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of CPU
R_ADC_Create	Initial setting of A/D converter
R_TAU0_Create	Initial setting of TAU0
R_INTC_Create	Initial setting of INTP0
R_ELC_Create	Initial setting of ELC
main	Main processing
R_TAU0_Channel0_Start	TAU00 start enable setting
R_ADC_Start	A/D conversion operation enable setting
r_adc_interrupt	A/D conversion interrupt
R_ADC_Get_Result	Obtain A/D conversion result

5.5 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	Initial setting of CPU
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_ADC_Create	
Outline	Initial setting of A/D converter
Header	None
Declaration	void R_ADC_Create(void)
Description	Perform the initial setting of the A/D converter to start A/D conversion by an event input signal from the ELC.
Argument	None
Return Value	None

R_TAU0_Create	
Outline	Initial setting of TAU0
Header	None
Declaration	void R_TAU0_Create(void)
Description	Perform the initial setting of TAU0 to operate as the delay counter by an event input signal from the ELC.
Argument	None
Return Value	None

R_INTC_Create	
Outline	Initial setting of INTP0
Header	None
Declaration	void R_INTC_Create(void)
Description	Enable the external interrupt rising edge as the ELC event generator.
Argument	None
Return Value	None

R_ELC_Create	
Outline	Initial setting of ELC
Header	None
Declaration	void R_ELC_Create(void)
Description	Perform the initial setting of the ELC to link INTP0 to TAU00, and TAU00 to the A/D converter.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

R_TAU0_Channel0_Start	
Outline	TAU00 operation enable setting
Header	None
Declaration	void R_TAU0_Channel0_Start(void)
Description	Enable TAU00 count operation.
Argument	None
Return Value	None

R_ADC_Start	
Outline	A/D conversion operation enable setting
Header	None
Declaration	void R_ADC_Start(void)
Description	Enable A/D conversion operation.
Argument	None
Return Value	None

r_adc_Interrupt	
Outline	A/D conversion interrupt
Header	None
Declaration	static void __near r_adc_interrupt(void)
Description	Perform an A/D conversion interrupt service routine.
Argument	None
Return Value	None

R_ADC_Get_Result	
Outline	Obtain A/D conversion result
Header	None
Declaration	void R_ADC_Get_Result(void)
Description	Obtain the A/D converted result and store it to the address specified as an argument.
Argument	uint16_t *buffer: Address where the A/D converted value is stored
Return Value	None

5.6 Flowcharts

5.6.1 Overall Flowchart

Figure 5.2 shows the Overall Flowchart.

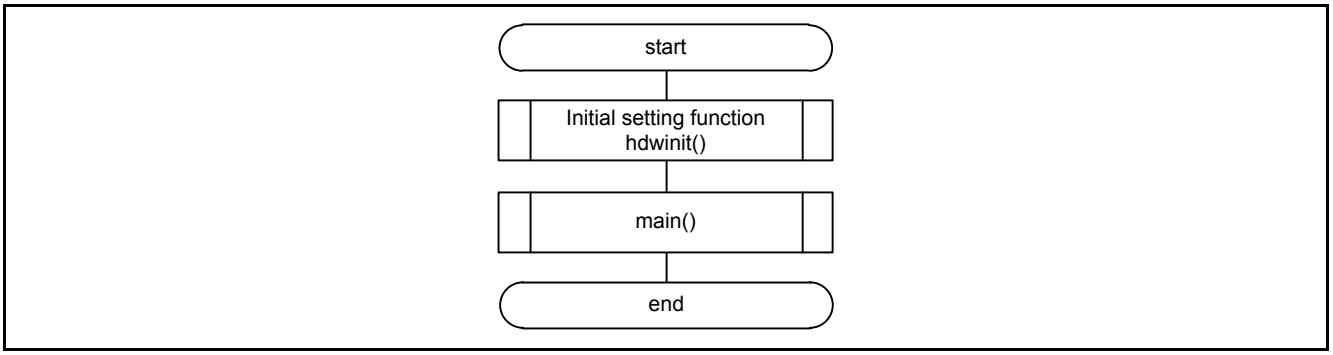


Figure 5.2 Overall Flowchart

5.6.2 Initial Setting

Figure 5.3 shows the Initial Setting.

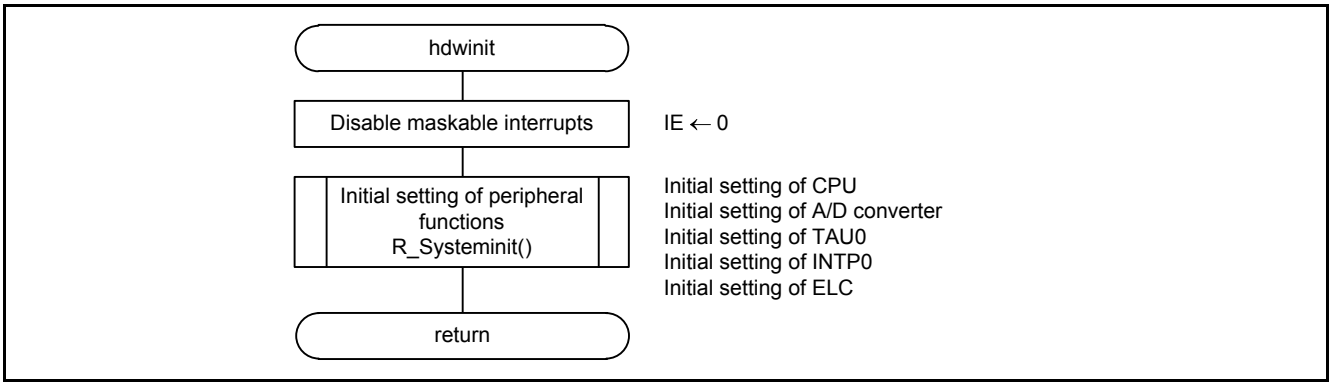


Figure 5.3 Initial Setting

5.6.3 Initial Setting of Peripheral Functions

Figure 5.4 shows the Initial Setting of Peripheral Functions.

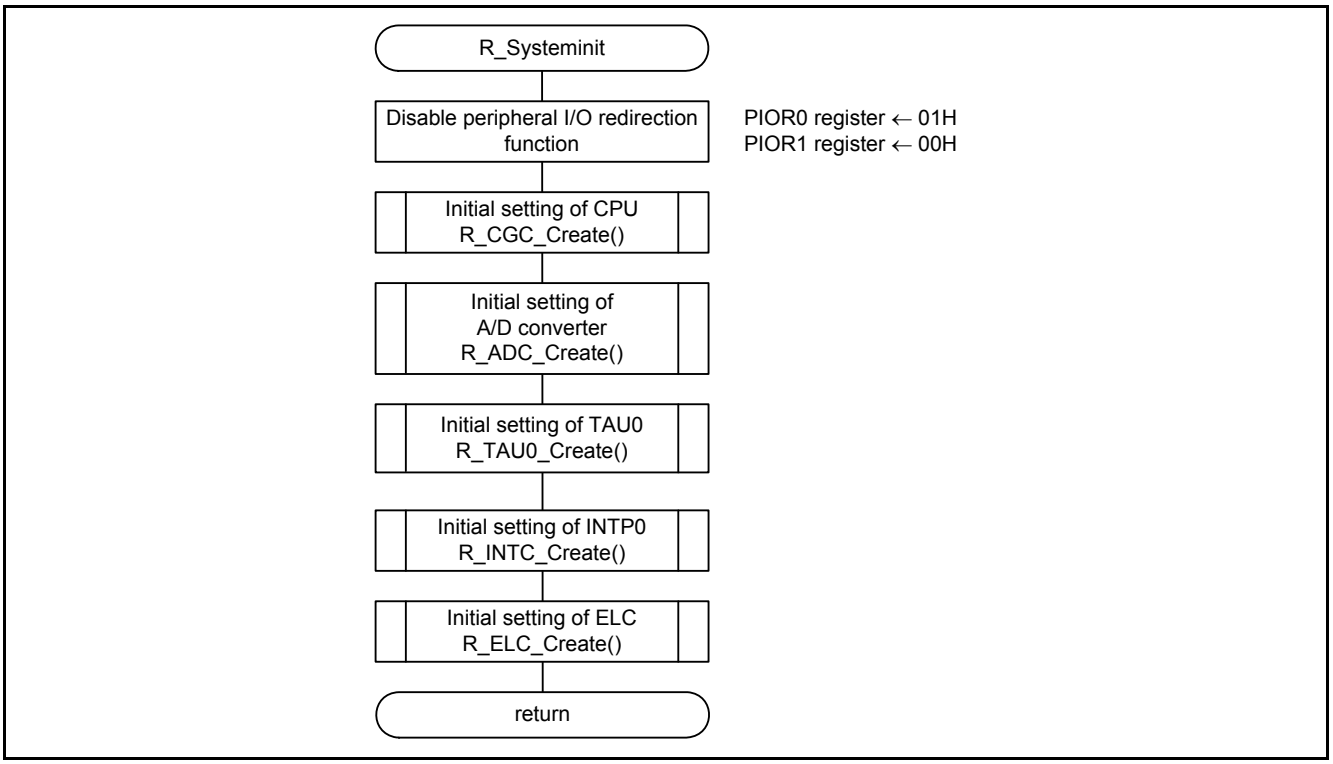


Figure 5.4 Initial Setting of Peripheral Functions

5.6.4 Initial Setting of CPU

Figure 5.5 shows the Initial Setting of the CPU.

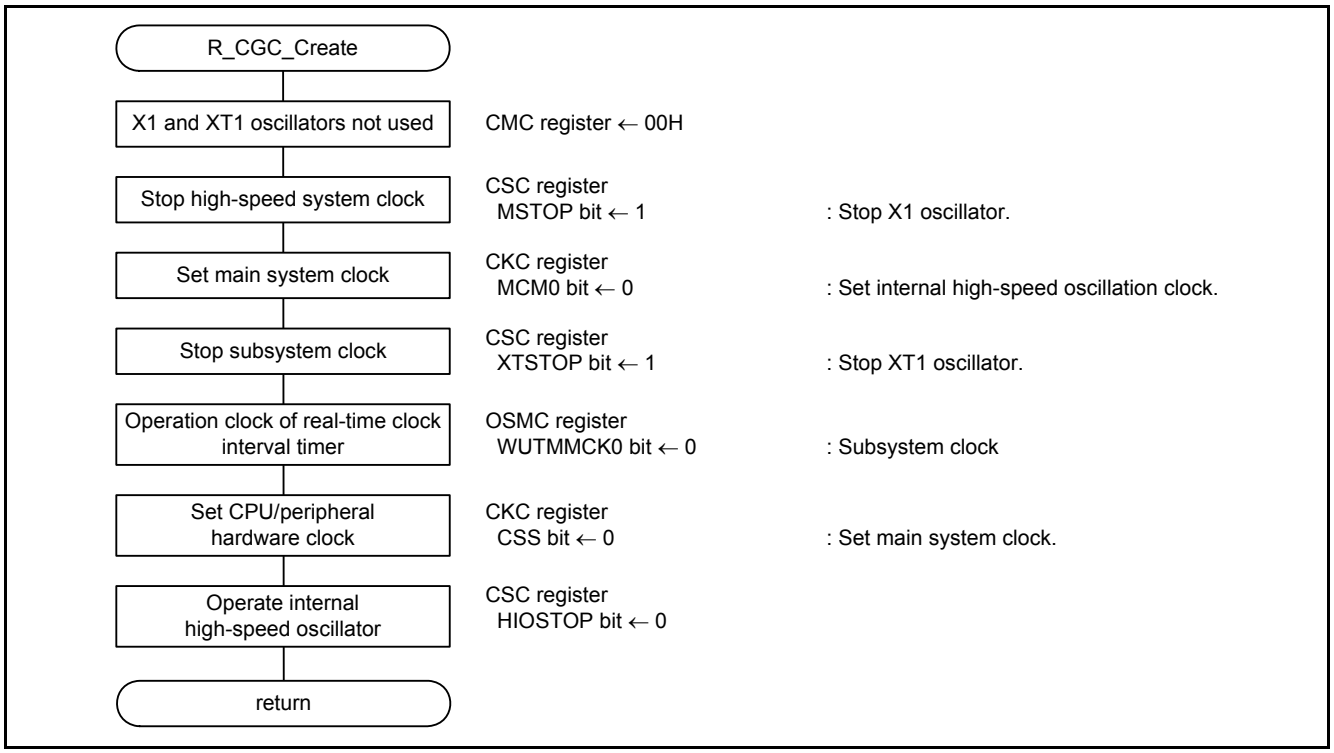


Figure 5.5 Initial Setting of the CPU

5.6.5 Initial Setting of the A/D Converter

Figure 5.6 shows the Initial Setting of the A/D Converter.

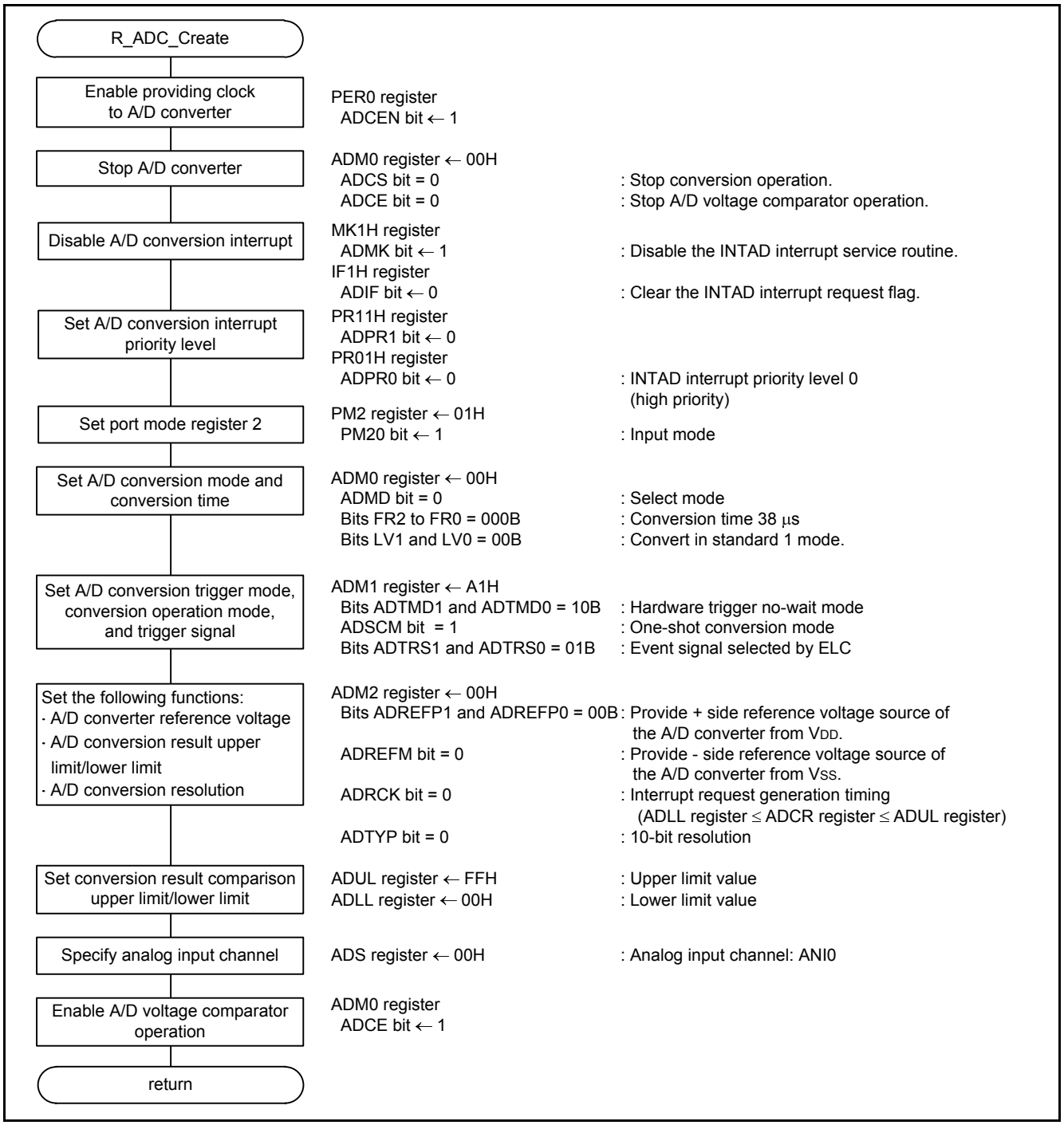


Figure 5.6 Initial Setting of the A/D Converter

Enable providing a clock to the A/D converter.

- Peripheral Enable Register 0 (PER0)
  Enable providing a clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
Setting Value	x	x	1	x	x	x	x	

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be read/written.

Stop the A/D converter.

- A/D Converter Mode Register 0 (ADM0)
  Stop A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value	0							0

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	Enables conversion operation [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: Stabilization wait status + conversion operation status

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable an A/D conversion interrupt.

- Interrupt Mask Flag Register (MK1H)
  Disable the INTAD interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
Setting Value	x	x	x	x	x	x	x	1

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt Request Flag Register (IF1H)
  Clear the INTAD interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	TIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
Setting Value	x	x	x	x	x	x	x	0

Bit 0

ADIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the A/D conversion interrupt priority level.

- Priority Specification Flag Registers (PR11H and PR01H)
  Set the INTAD interrupt priority level to level 0 (high priority).

Symbol	7	6	5	4	3	2	1	0
PR11H	TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
Setting Value	x	x	x	x	x	x	x	0

Symbol	7	6	5	4	3	2	1	0
PR01H	TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
Setting Value	x	x	x	x	x	x	x	0

ADPR1	ADPR0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Set port mode register 2.

- Port Mode Register 2 (PM2)
  Set the P20 pin to input mode.

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
Setting Value	x	x	x	x	x	x	x	1

Bit 0

PM20	P20 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set A/D conversion mode and conversion time.

- A/D Converter Mode Register 0 (ADM0)
  Set A/D conversion mode and conversion time.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value		0	0	0	0	0	0	

Bit 6

ADMD	Specification of the A/D conversion channel selection mode
0	Select mode
1	Scan mode

Bits 5 to 1

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 μs	f_{CLK}/64
0	0	1								38 μs	19 μs	f_{CLK}/32
0	1	0							38 μs	19 μs	9.5 μs	f_{CLK}/16
0	1	1						38 μs	19 μs	9.5 μs	4.75 μs	f_{CLK}/8
1	0	0						28.5 μs	14.25 μs	7.125 μs	3.5625 μs	f_{CLK}/6
1	0	1						23.75 μs	11.875 μs	5.938 μs	2.9688 μs	f_{CLK}/5
1	1	0					38 μs	19 μs	9.5 μs	4.75 μs	2.375 μs	f_{CLK}/4
1	1	1				38 μs	19 μs	9.5 μs	4.75 μs	2.375 μs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	34 μs	f_{CLK}/64
0	0	1								34 μs	17 μs	f_{CLK}/32
0	1	0							34 μs	17 μs	8.5 μs	f_{CLK}/16
0	1	1						34 μs	17 μs	8.5 μs	4.25 μs	f_{CLK}/8
1	0	0						25.5 μs	12.75 μs	6.375 μs	3.1875 μs	f_{CLK}/6
1	0	1						21.25 μs	10.625 μs	5.3125 μs	2.6563 μs	f_{CLK}/5
1	1	0					34 μs	17 μs	8.5 μs	4.25 μs	2.125 μs	f_{CLK}/4
1	1	1				34 μs	17 μs	8.5 μs	4.25 μs	2.125 μs	Setting prohibited	f_{CLK}/2
×	×	×	1	0	Low voltage 1	Setting prohibited						—
×	×	×	1	1	Low voltage 2	Setting prohibited						—

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set A/D conversion trigger mode, conversion operation mode, and trigger signal.

- A/D Converter Mode Register 1 (ADM1)

  Select A/D conversion trigger mode, A/D conversion operation mode, and hardware trigger signal.

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
Setting Value	1	0	1	—	—	—	0	1

Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	—	Software trigger mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

Bits 1 and 0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 1 count or capture interrupt signal (INTTM01)
0	1	Event signal selected by ELC
1	0	Real-time clock interrupt signal (INTRTC)
1	1	Interval timer interrupt signal (INTIT)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the A/D converter reference voltage, upper limit and lower limit conversion results, and resolution.

- A/D Converter Mode Register 2 (ADM2)

  Set the A/D converter reference voltage, upper limit and lower limit conversion results, and resolution.

Symbol	7	6	5	4	3	2	1	0
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
Setting Value	0	0	0	—	0	x	—	0

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V) Note
1	1	Setting prohibited

When ADREFP1 or ADREFP0 bit is rewritten, this must be configured in accordance with the following procedures.
(1) Set ADCE = 0
(2) Change the values of ADREFP1 and ADREFP0
(3) Reference voltage stabilization wait time (A)
(4) Set ADCE = 1
(5) Reference voltage stabilization wait time (B)
When ADREFP1 and ADREFP0 are set to 1 and 0, the setting is changed to A = 5μs, B = 1μs.
When ADREFP1 and ADREFP0 are set to 0 and 0 or 0 and 1, A needs no wait and B = 1μs.
When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output voltage and internal reference voltage.
Be sure to perform A/D conversion while ADISS = 0.

Note Operation is possible only in HS (high-speed main) mode.

Bit 5

ADREFM	Selection of the − side reference voltage source of the A/D converter
0	Supplied from V_{SS}
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking the upper limit and lower limit conversion result values
0	The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register
1	The interrupt signal (INTAD) is output when the ADCR register ≤ the ADLL register or the ADUL register ≤ the ADCR register

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	10-bit resolution
1	8-bit resolution

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the conversion result comparison upper limit/lower limit.

- Conversion Result Comparison Upper Limit Setting Register (ADUL)
  Set FFH to the conversion result comparison upper limit.

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
Setting Value	1	1	1	1	1	1	1	1

- Conversion Result Comparison Lower Limit Setting Register (ADLL)
  Set 00H to the conversion result comparison lower limit.

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
Setting Value	0	0	0	0	0	0	0	0

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set analog input channels.

- Analog Input Channel Specification Register (ADS)
  Set analog input channels to ANI0.

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
Setting Value	0	—	—	0	0	0	0	0

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AVREFP pin
0	0	0	0	0	1	ANI1	P21/ANI1/AVREFM pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	0	1	0	0	0	ANI8	P150/ANI8 pin
0	0	1	0	0	1	ANI9	P151/ANI9 pin
0	0	1	0	1	0	ANI10	P152/ANI10 pin
0	0	1	0	1	1	ANI11	P153/ANI11 pin
0	0	1	1	0	0	ANI12	P154/ANI12 pin
0	0	1	1	0	1	ANI13	P155/ANI13 pin
0	0	1	1	1	0	ANI14	P156/ANI14 pin
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P147/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
0	1	0	1	0	0	ANI20	P100/ANI20 pin
1	0	0	0	0	0	—	Temperature sensor 0 output
1	0	0	0	0	1	—	Internal reference voltage output (1.44 V)
Other than the above						Setting prohibited	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Enable A/D voltage comparator operation.

- A/D Converter Mode Register 0 (ADM0)
  Enable A/D voltage comparator operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value								1

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.6.6 Initial Setting of TAU0

Figure 5.7 shows the Initial Setting of TAU0.

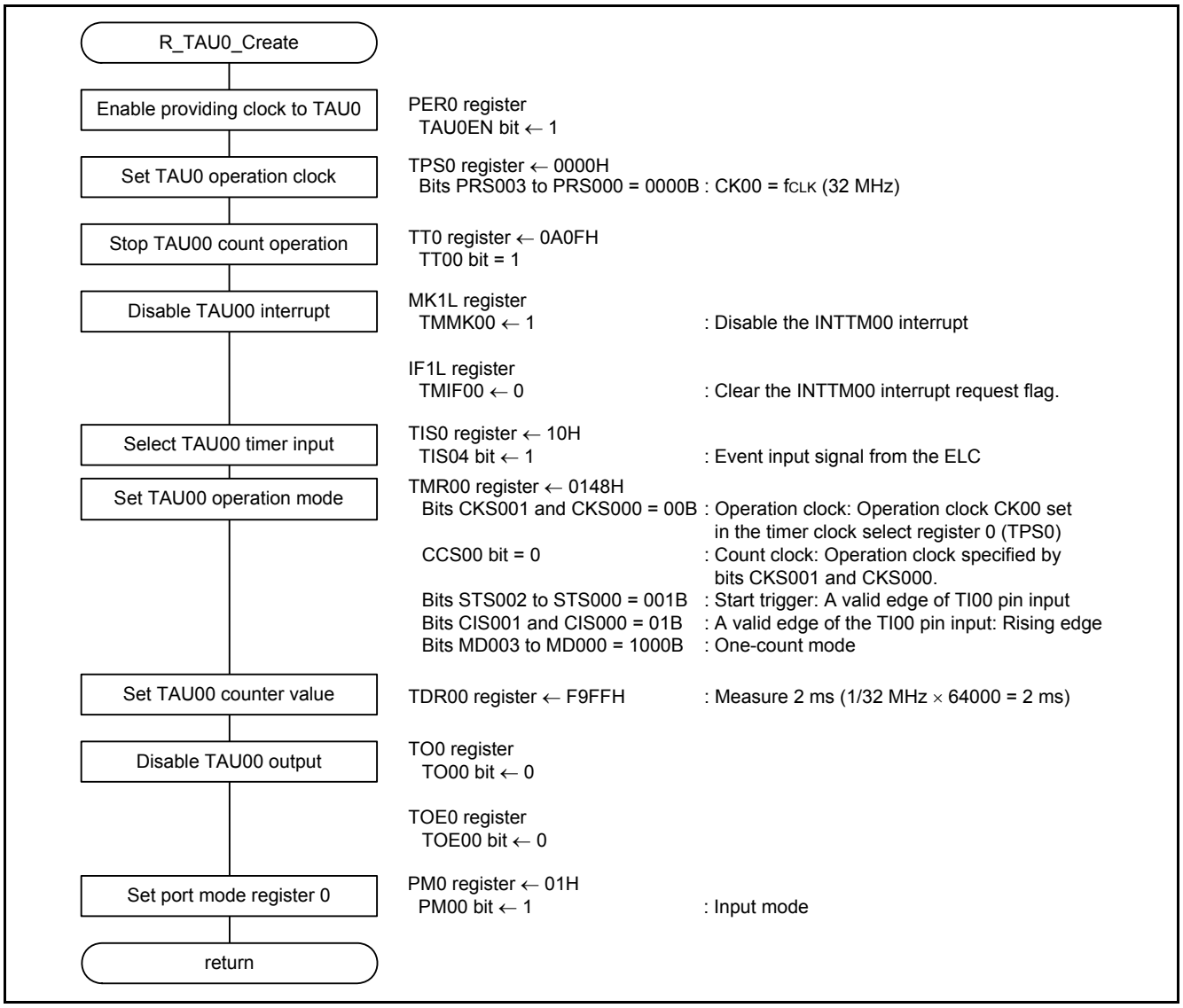


Figure 5.7 Initial Setting of TAU0

Enable providing a clock to TAU0.

- Peripheral Enable Register 0 (PER0)
  Enable providing a clock to TAU0.

Symbol	7	6	5	4	3	2	1	0
PER0	RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
Setting Value	x	x		x	x	x	x	1

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read and written.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the TAU0 operation clock.

- Timer Clock Select Register 0 (TPS0)
  Set the TAU0 operation clock.

Symbol	15	14	13	12	11	10	9	8
TT0	0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020
Setting Value	—	—	x	x	—	—	x	x

Symbol	7	6	5	4	3	2	1	0
TT0	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
Setting Value	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00)				
					f_{CLK} = 2 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz	f_{CLK} = 32 MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Stop TAU00 count operation.

- Timer Channel Stop Register 0 (TT0)
  Stop TAU00 count operation.

Symbol	15	14	13	12	11	10	9	8
TT0	0	0	0	0	TTH 03	0	TTH 01	0
Setting Value	—	—	—	—	x	—	x	—

Symbol	7	6	5	4	3	2	1	0
TT0	0	0	0	0	TT03	TT02	TT01	TT00
Setting Value	—	—	—	—	x	x	x	1

Bits 3 to 0

TT00	Operation stop trigger of channel 0
0	No trigger operation
1	Operation is stopped (stop trigger is generated). This bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in the 8-bit timer mode.

Disable INTTM00 interrupt.

- Interrupt Mask Flag Register (MK1L)
  Disable the INTTM00 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
Setting Value	x	x	x	1	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Interrupt Request Flag Register (IF1L)
Clear the INTTM00 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1L	TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
Setting Value	x	x	x	0	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Select TAU00 timer input.

• Timer Input Select Register 0 (TIS0)
Set timer input as an event input signal from the ELC.

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	TIS04	0	TIS02	TIS01	TIS00
Setting Value	—	—	—	1	—	x	x	x

Bit 4

TIS04	Selection of timer input used with channel 0
0	Input signal of timer input pin (TI00)
1	Event input signal from ELC

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set TAU00 operation mode.

- Timer Mode Register 00 (TMR00)
  Set TAU00 operation mode.

Symbol	15	14	13	12	11	10	9	8
TMR00	CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000
Setting Value	0	0	0	0	—	0	0	1

Symbol	7	6	5	4	3	2	1	0
TMR00	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
Setting Value	0	1	—	—	1	0	0	0

Bits 15 and 14

CKS 001	CKS 000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCS00 bit. The operation clocks CK02 and CK03 can only be selected for channels 1 and 3.		

Bit 12

CCS 00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of input signal input from the TI00 pin
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 10 to 8

STS 002	STS 001	STS 000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS 001	CKS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STS002 to STS000 bits is other than 010B, set the CIS001 to CIS000 bits to 10B.		

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 3 to 1

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		
The operation of the MD000 bit varies depending on each operation mode (see table below).						

Bit 0

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD 000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the TAU00 counter value.

- Timer Data Register 00 (TDR00)
  Set F9FFH as the count value and measure 2 ms.

Symbol	15	14	13	12	11	10	9	8
TDR00								
Setting Value	1	1	1	1	1	0	0	1

Symbol	7	6	5	4	3	2	1	0
TDR00								
Setting Value	1	1	1	1	1	1	1	1

Disable TAU00 output.

- Timer Output Register 0 (TO0)
  Set 0 as the timer output value.

Symbol	15	14	13	12	11	10	9	8
TO0	0	0	0	0	0	0	0	0
Setting Value	—	—	—	—	—	—	—	—

Symbol	7	6	5	4	3	2	1	0
TO0	0	0	0	0	TO03	TO02	TO01	TO00
Setting Value	—	—	—	—	x	x	x	0

Bit 0

TO00	Timer output of channel 0
0	Timer output value is “0”.
1	Timer output value is “1”.

Refer to the RL78/G14 user’s manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Timer Output Enable Register 0 (TOE0)
Disable TO00 pin output.

Symbol	15	14	13	12	11	10	9	8
TOE0	0	0	0	0	0	0	0	0
Setting Value	—	—	—	—	—	—	—	—

Symbol	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	TOE 03	TOE 02	TOE 01	TOE 00
Setting Value	—	—	—	—	x	x	x	0

Bit 0

TOE 00	Timer output enable/disable of channel 0
0	The TO00 operation stopped by count operation (timer channel output bit). Writing to the TO00 bit is enabled. The TO00 pin functions as data output, and it outputs the level set to the TO00 bit. The output level of the TO00 pin can be manipulated by software.
1	The TO00 operation enabled by count operation (timer channel output bit). Writing to the TO00 bit is disabled (writing is ignored). The TO00 pin functions as timer output, and output from the TO00 pin is set or reset depending on the timer operation. The TO00 pin outputs the square-wave or PWM depending on the timer operation.

Set port mode register 0.

• Port Mode Register 0 (PM0)
Set the P00 pin to input mode.

Symbol	7	6	5	4	3	2	1	0
PM0	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00
Setting Value	x	x	x	x	x	x	x	1

Bit 0

PM00	P00 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.6.7 Initial Setting of INTP0

Figure 5.8 shows the Initial Setting of INTP0.

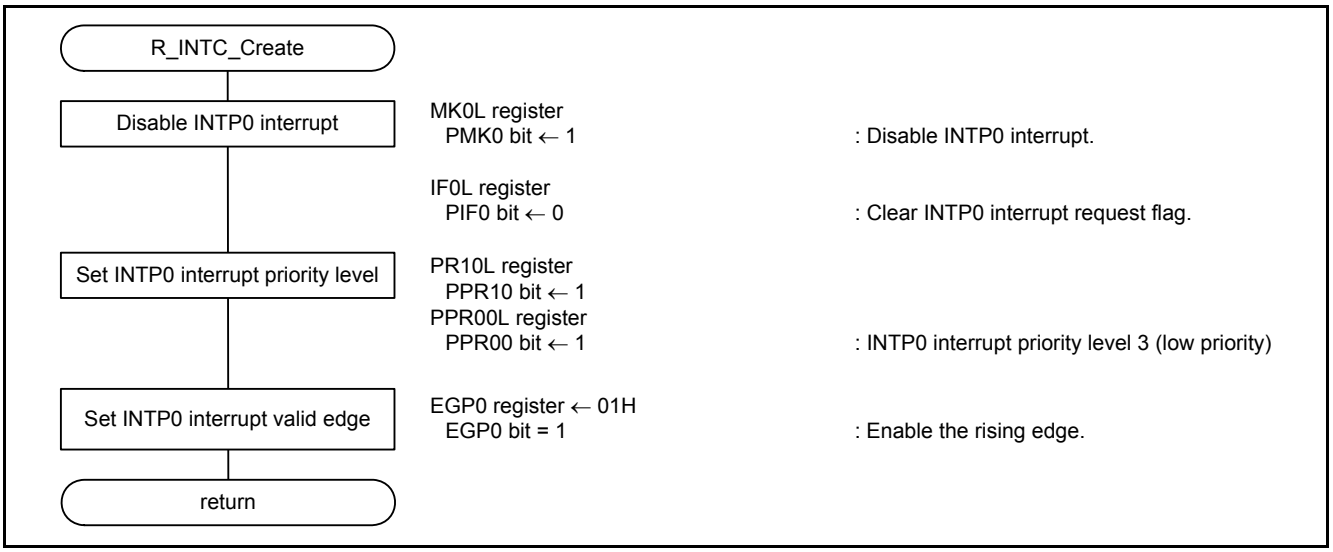


Figure 5.8 Initial Setting of INTP0

Disable the INTP0 interrupt.

- Interrupt Mask Flag Register (MK0L)
  Disable the INTP0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK0L	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
Setting Value	x	x	x	x	x	1	x	x

Bit 2

PMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Interrupt Request Flag Register (IF0L)
Clear the INTP0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF0L	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
Setting Value	x	x	x	x	x	0	x	x

Bit 2

PIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Set the INTP0 interrupt priority level.

• Priority Specification Flag Registers (PR00L, PR10L)
Set the INTP0 interrupt priority level to level 3 (low priority).

Symbol	7	6	5	4	3	2	1	0
PR10L	PPR15	PPR14	PPR13	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1
Setting Value	x	x	x	x	x	1	x	x

Symbol	7	6	5	4	3	2	1	0
PR00L	PPR05	PPR04	PPR03	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0
Setting Value	x	x	x	x	x	1	x	x

PPR10	PPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the INTP0 interrupt valid edge.

- External Interrupt Rising Edge Enable Register (EGP0).
- External Interrupt Falling Edge Enable Register (EGN0)
  Set the valid edge of the INTP0 pin to the rising edge.

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
Setting Value	x	x	x	x	x	x	x	1

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
Setting Value	x	x	x	x	x	x	x	0

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.6.8 Initial Setting of the ELC

Figure 5.9 shows the Initial Setting of the ELC.

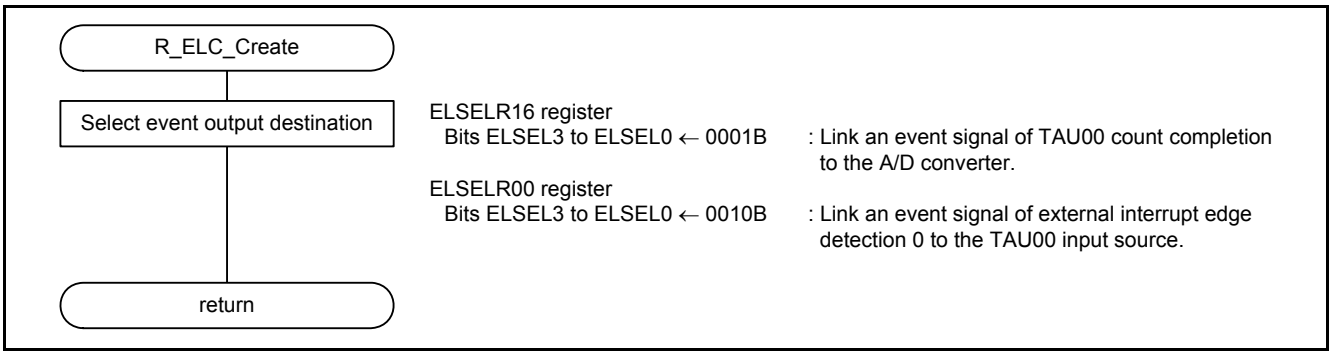


Figure 5.9 Initial Setting of the ELC

Select the event output destination.

- Event Output Destination Select Register 16 (ELSELR16)
  Link an event signal of TAU00 count completion to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
ELSELR16	—	—	—	—	ELSEL3	ELSEL2	ELSEL1	ELSEL0
Setting Value	—	—	—	—	0	0	0	1

- Event Output Destination Select Register 00 (ELSELR00)
  Link an event signal of external interrupt edge detection 0 to the TAU00 input source.

Symbol	7	6	5	4	3	2	1	0
ELSELR00	—	—	—	—	ELSEL3	ELSEL2	ELSEL1	ELSEL0
Setting Value	—	—	—	—	0	0	1	0

Bits 3 to 0

ELSEL3 (1)	ELSEL2	ELSEL1	ELSEL0	Event Link Selection	R/W
0	0	0	0	Event link disabled	R/W
0	0	0	1	Select operation of peripheral function to link	
0	0	1	0	Select operation of peripheral function to link	
0	0	1	1	Select operation of peripheral function to link	
0	1	0	0	Select operation of peripheral function to link	
0	1	0	1	Select operation of peripheral function to link	
1	1	1	0	Select operation of peripheral function to link	
1	1	1	1	Select operation of peripheral function to link	

Note:
1. Only for 80-pin and 100-pin products.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Register Name	Event Generator	Event Description
ELSELR00	External interrupt edge detection 0	INTP0
ELSELR01	External interrupt edge detection 1	INTP1
ELSELR02	External interrupt edge detection 2	INTP2
ELSELR03	External interrupt edge detection 3	INTP3
ELSELR04	External interrupt edge detection 4	INTP4
ELSELR05	External interrupt edge detection 5	INTP5
ELSELR06	Key return signal detection	INTKR
ELSELR07	RTC fixed-cycle signal/Alarm match detection	INTRTC
ELSELR08	Timer RD0 Input capture A/Compare match A	INTTRD0
ELSELR09	Timer RD0 Input capture B/Compare match B	INTTRD0
ELSELR10	Timer RD1 Input capture A/Compare match A	INTTRD1
ELSELR11	Timer RD1 Input capture B/Compare match B	INTTRD1
ELSELR12	Timer RD1 Underflow	TRD1 underflow signal
ELSELR13	Timer RJ0 Underflow	INTTRJ0
ELSELR14	Timer RG Input capture A/Compare match A	INTTRG
ELSELR15	Timer RG Input capture B/Compare match B	INTTRG
ELSELR16	TAU channel 00 Count end/Capture end	INTTM00
ELSELR17	TAU channel 01 Count end/Capture end	INTTM01
ELSELR18	TAU channel 02 Count end/Capture end	INTTM02
ELSELR19	TAU channel 03 Count end/Capture end	INTTM03
ELSELR20 (1)	TAU channel 10 Count end/Capture end	INTTM10
ELSELR21 (1)	TAU channel 11 Count end/Capture end	INTTM11
ELSELR22 (1)	TAU channel 12 Count end/Capture end	INTTM12
ELSELR23 (1)	TAU channel 13 Count end/Capture end	INTTM13
ELSELR24 (2)	Comparator detection 0	INTCMP0
ELSELR25 (2)	Comparator detection 1	INTCMP1

Notes:
1. Only for 80-pin and 100-pin products.
2. Only for products with a code flash memory size of 96 KB or more

Remarks: n = 00 to 25

Bits ELSEL3 to ELSEL0 in ELSELRn Register	Link Destination Peripheral Function	Operation When Receiving Event
0001B	A/D converter	A/D conversion starts
0010B	TAU0 channel 0 input source	Delay counter, input pulse interval measurement, external event counter
0011B	TAU0 channel 1 input source	Delay counter, input pulse interval measurement, external event counter
0100B	Timer RJ0	Count source
0101B	Timer RG	TRGIOB input capture
0110B	Timer RD0	TRDIOD0 input capture, pulse output forced cutoff
0111B	Timer RD1	TRDIOD1 input capture, pulse output forced cutoff
1000B	DA0	Real-time output (96 KB or more code flash memory products only.)
1001B	DA1	Real-time output (96 KB or more code flash memory products only.)

Remarks: n = 00 to 25

5.6.9 Main Processing

Figure 5.10 shows the Main Processing.

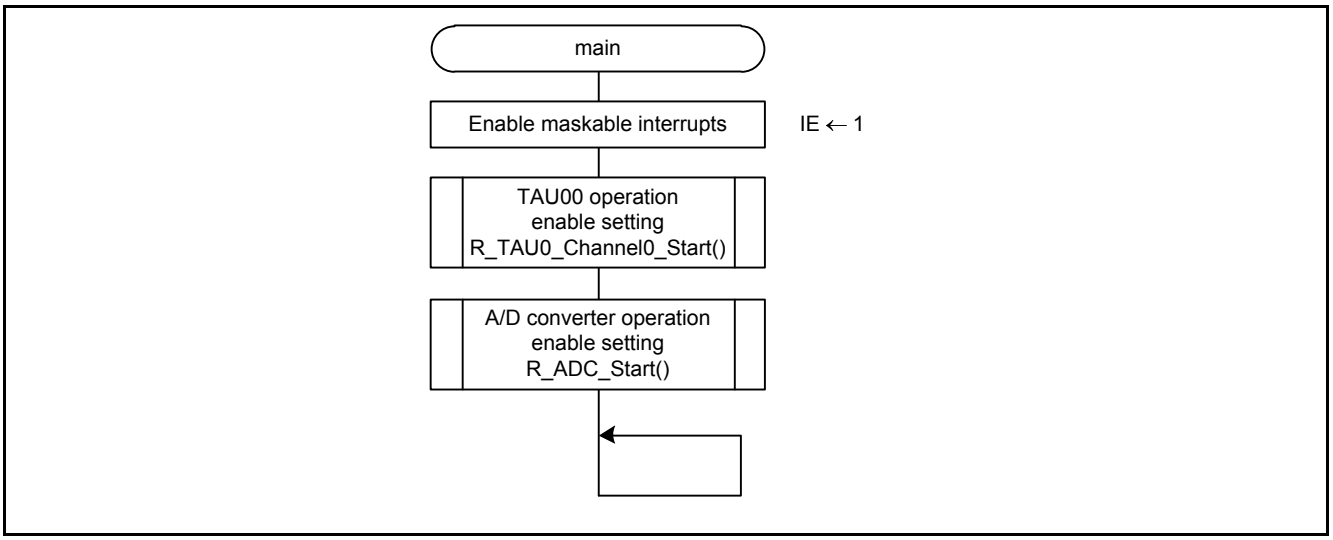


Figure 5.10 Main Processing

5.6.10 TAU00 Operation Enable Setting

Figure 5.11 shows the TAU00 Operation Enable Setting.

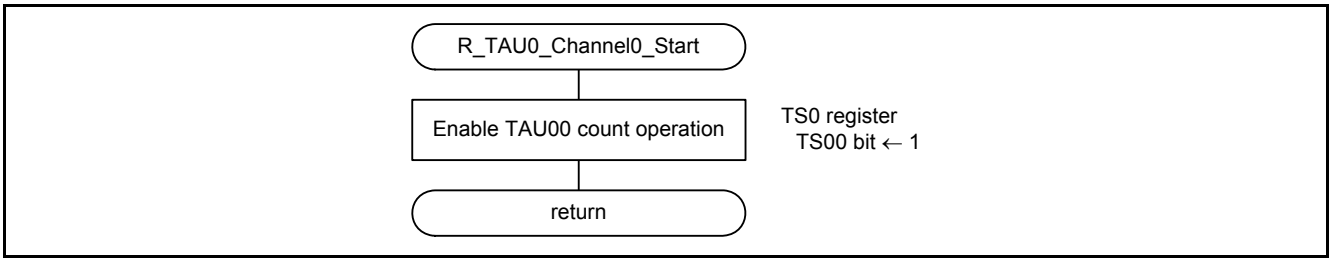


Figure 5.11 TAU00 Operation Enable Setting

Enable TAU00 count operation.

- Timer Channel Start Register 0 (TS0)
  Set TAU00 to count operation enabled.

Symbol	15	14	13	12	11	10	9	8
TS0	0	0	0	0	TSH 03	0	TSH 01	0
Setting Value	—	—	—	—	x	—	x	—

Symbol	7	6	5	4	3	2	1	0
TS0	0	0	0	0	TS03	TS02	TS01	TS00
Setting Value	—	—	—	—	x	x	x	1

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled. The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.6.11 A/D Conversion Operation Enable Setting

Figure 5.12 shows the A/D Conversion Operation Enable Setting.

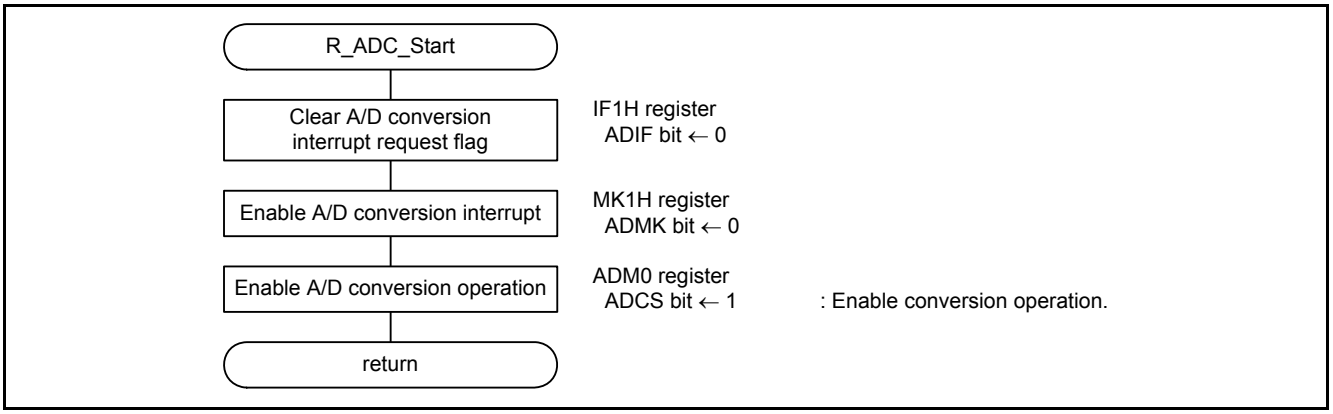


Figure 5.12 A/D Conversion Operation Enable Setting

Clear the A/D conversion interrupt request flag.

- Interrupt Request Flag Register (IF1H)
  Clear the INTAD interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF1H	TMIF10	TRJIF0	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
Setting Value	x	x	x	x	x	x	x	0

Bit 0

ADIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Enable the A/D conversion interrupt.

- Interrupt Mask Flag Register (MK1H)
  Enable the INTAD interrupt.

Symbol	7	6	5	4	3	2	1	0
MK1H	TMMK10	TRJMK0	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
Setting Value	x	x	x	x	x	x	x	0

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Enable A/D conversion operation.

- A/D Converter Mode Register 0 (ADM0)
  Enable A/D conversion operation.

Symbol	7	6	5	4	3	2	1	0
ADM0	ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
Setting Value	1							

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation [When read] Conversion stopped/standby status
1	Enables conversion operation [When read] While in the software trigger mode: Conversion operation status While in the hardware trigger wait mode: Stabilization wait status + conversion operation status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5.6.12 A/D Conversion Interrupt

Figure 5.13 shows the A/D Conversion Interrupt.

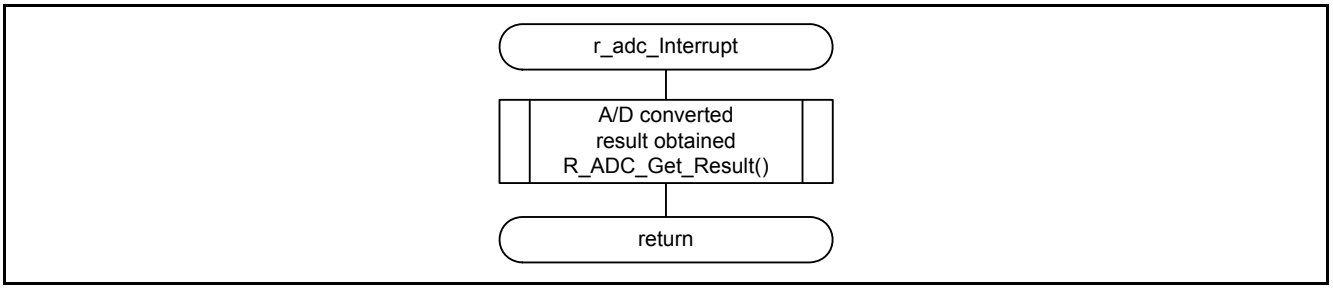


Figure 5.13 A/D Conversion Interrupt

5.6.13 Obtain A/D Converted Result

Figure 5.14 shows the A/D Converted Result Obtained.

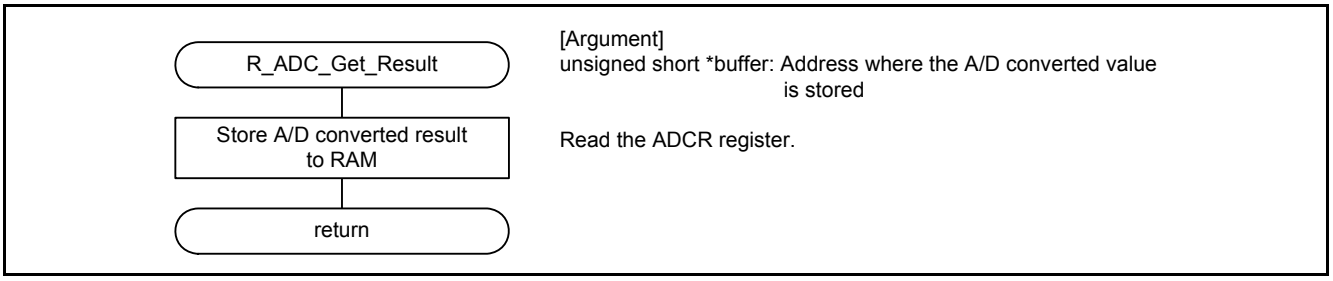


Figure 5.14 A/D Converted Result Obtained

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

User's Manual: Hardware

RL78/G14 Group User's Manual: Hardware (R01UH0186E)
RL78 Family User's Manual: Software (R01US0015E)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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REVISION HISTORY	RL78/G14 Operation in Conjunction with Three Combined Events Using the ELC

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 15, 2015	—	First edition issued

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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