RL78/G14, H8/36109

Migration Guide from H8 to RL78: Timer RD

Introduction

This application note describes how to migrate the Timer RD of the H8/36109 to the Timer RD of the RL78/G14.

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of Timer RD of H8/36109 and Timer RD of RL78/G14

Table 1.1 shows the functions of the Timer RD of H8/36109, and Table 1.2 shows the functions of the Timer RD of RL78/G14.

Table 1.1 Functions of H8/36109 Timer RD

Function	Explanation
Timer mode (Output compare function)	Function to perform 0 output / 1 output / toggle output from pin.
Timer mode (Input capture function)	The TRDCNT value can be transferred to GR on detection of the input edge of the input capture pin.
PWM mode	PWM waveforms are output from the FTIOB, FTIOC, and FTIOD output pins.
Reset synchronous PWM mode	Three normal- and counter-phase PWM waveforms are output by combining channels 0 and 1 that one of changing points of waveforms will be common.
Complementary PWM mode	Three PWM waveforms for non-overlapped normal and counter phases are output by combining channels 0 and 1.
PWM3 mode	Single-phase PWM waveforms can be output. The waveform does not overlap its counter-phase waveform.

Table 1.2 Functions of RL78/G14 Timer RD

Function	Explanation
Timer mode (Output compare function)	Detect register value matches with a counter (Pin output can be changed at detection)
Timer mode (Input capture function)	Transfer the counter value to a register with an external signal as the trigger
Timer mode (PWM function)	Output pulse of any width continuously
Reset synchronous PWM mode	Output three-phase waveforms (6) without sawtooth wave modulation and dead time
Complementary PWM mode	Output three-phase waveforms (6) with triangular wave modulation and dead time
PWM3 mode	Output PWM waveforms (2) with a fixed period

Table 1.3 shows the Timer RD functions of H8/36109 and RL78/G14.

Table 1.3 Correspondence between Functions

H8/36109 Timer RD	RL78/G14 Timer RD
Timer mode (Output compare function)	Timer mode (Output compare function)
Timer mode (Input capture function)	Timer mode (Input capture function)
PWM mode	Timer mode (PWM function)
Reset synchronous PWM mode	Reset synchronous PWM mode
Complementary PWM mode	Complementary PWM mode
PWM3 mode	PWM3 mode

2. Summary of Differences between Functions

Table 2.1 summarizes the differences between the functions of the Timer RD of H8/36109 and RL78/G14.

Table 2.1 Summary of Differences between Functions

Item	H8/36109	RL78/G14
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M (Note1), External clock (Note2)	f_{HOCO} (Note3), f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Maximum operating frequency	40MHz (Note4)	64MHz (Note5)
Operation Mode	Timer mode (Output compare function) Timer mode (Input capture function) PWM mode Reset synchronous PWM mode Complementary PWM mode PWM3 mode	Timer mode (Output compare function) Timer mode (Input capture function) Timer mode (PWM function) Reset synchronous PWM mode Complementary PWM mode PWM3 mode
Buffer operation	Yes	Yes
Timer output disabled mode	Yes	Yes
How to generate timer output disabled mode	Setting the PTO bit in the TRDOER2 register to 1 and then inputting a low level signal to the TRDOI pin.	- Setting the TRDPTO bit in the TRDOER2 register to 1 and then inputting a low level signal to the INTP0 pin. - Setting the TRDSHUTS bit in the TRDOER2 register to 1 - Issuing the interrupt request from the event link controller (ELC)
Operation mode in which the timer output disabling function can be used	- Output compare function - PWM mode - Reset synchronous PWM mode - Complementary PWM mode - PWM3 mode	- PWM mode - Reset synchronous PWM mode - Complementary PWM mode - PWM3 mode
How to set pin state in timer output disabled mode	Setting the I/O ports shared with the FTIOji pins	Setting the TRDDFi register
A/D conversion start trigger output signal	Yes (Only Complementary PWM mode)	None (substituted by ELC)
Shared pin for timer RD	PD0 to PD7, PE0 to PE7	P10 to P17
Interrupt source	Compare match / Input capture Overflow, Underflow	Compare match / Input capture Overflow, Underflow
Number of input / output pin	8 pins	8 pins

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Note 4. Maximum operating frequency of on-chip oscillator

Note 5. Maximum operating frequency of high-speed on-chip oscillator

Remarks 1. For H8/36109, j = A, B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = A, B, C, D i = 0, 1

2.1 Differences between Waveform Output by Compare Match

The waveform output by compare match of the timer RD of the H8/36109 correspond to the timer mode (Output compare function) of the Timer RD of the RL78/G14. Table 2.2 and Table 2.3 shows the differences between the waveform output by compare match.

Table 2.2 Differences between the waveform output by compare match (1/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Control of timer RD input clock supply	Setting the MSTTRDi bit in the MSTCR4 register to 0 (Initial value)	Setting the TRD0EN bit in the PER1 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), External clock (Note2)	f_{HOCO} (Note3) ,f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Count mode	Count up	Count up
Counter Clear	TRDCR_i register - CCLR2 to CCLR0 bit: B'000, B'100 Disables TRDCNT clearing - CCLR2 to CCLR0 bit: B'011, B'111 Synchronization clear; Clears TRDCNT in synchronous with counter clearing of the other channel's timer - CCLR2 to CCLR0 bit: Other than B'000, B'011, B'100, B'111 Clear TRDCNT by GRj compare match	TRDCRi register - CCLR2 to CCLR0 bit: 000B Clear disabled (free-running operation) - CCLR2 to CCLR0 bit: 011B Synchronous clear (clear simultaneously with other timer RDi counter) - CCLR2 to CCLR0 bit: 001B, 010B, 101B, 110B Clear by compare match with TRDGRji
Waveform output timing	compare match	compare match
Count start condition	Write 1 to the STRi bit in the TRDSTR register	Write 1 to the TSTARTi bit in the TRDSTR register
Count stop condition	- When CSTPNi bit in TRDSTR register is set to 1, write 0 to STRi bit. - When CSTPNi bit in TRDSTR register is set to 0, the count stops at the compare match with GRA_i register.	- When CSELi bit in TRDSTR register is set to 1, write 0 to TSTARTi bit. The output compare output pin holds the output level before the count stops. - When CSELi bit in TRDSTR register is set to 0, the count stops at the compare match with the TRDGRAi register. The output compare output pin holds the level after output change by compare match.
Interrupt request generation timing	- Compare match - TRDCNT_i register overflow	- Compare match - TRDi register overflow

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Remarks 1. For H8/36109, j = A, B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = A, B, C, D i = 0, 1

Table 2.3 Differences between the waveform output by compare match (2/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Acquire timer counter value	Reading TRDCNT_i register	Reading TRDi register
Write timer counter value	- When SYNC bit in TRDMDR register is set to 0 (TRDCNT_1 and TRDCNT_0 operate as independent timer counters). Data can be written to TRDCNT_i register. - When SYNC bit in TRDMDR register is set to 1 (TRDCNT_1 and TRDCNT_0 operate synchronously). Data can be written to both TRDCNT_0 and TRDCNT_1 register by writing to TRDCNT_i register.	- When the TRDSYNC bit in the TRDMR register is set to 0 (TRD0 and TRD1 operate independently). Data can be written to the TRDi register. - When the TRDSYNC bit in the TRDMR register is set to 1 (TRD0 and TRD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Output of the timer is disabled by external trigger	Yes	None
Select function	- Output level selection at compare match - Initial output level selection - Timing for setting TRDCNT_i register to H'0000 - Buffer operation - Synchronous operation - Changing output pin for register	- Output level selection at compare match - Initial output level selection - Timing for setting TRDi register to 0000H - Buffer operation - Synchronous operation - Changing output pin for register - Timer RD can be used as the internal timer without output. - Simultaneous operation (A/D trigger generation etc.) using ELC
Output pin	FTIOji pin	TRDIOji pin

Remarks 1. For H8/36109, j = A, B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = A, B, C, D i = 0, 1

2.2 Differences between Input Capture Function

The Input Capture Function of the timer RD of the H8/36109 correspond to the timer mode (Input Capture function) of the Timer RD of the RL78/G14. Table 2.4 shows the differences between input capture Function.

Table 2.4 Differences between the input capture function

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Control of timer RD input clock supply	Setting the MSTTRDi bit in the MSTCR4 register to 0 (Initial value)	Setting the TRD0EN bit in the PER1 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), External clock (Note2)	f_{HOCO} (Note3) ,f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Count mode	Count up	Count up
Counter Clear	TRDCR_i register - CCLR2 to CCLR0 bit: B'000, B'100 Disables TRDCNT clearing - CCLR2 to CCLR0 bit: B'011, B'111 Synchronization clear; Clears TRDCNT in synchronous with counter clearing of the other channel's timer - CCLR2 to CCLR0 bit: Other than B'000, B'011, B'100, B'111 Clear TRDCNT by GRj input capture	TRDCRi register - CCLR2 to CCLR0 bit: 000B Clear disabled (free-running operation) - CCLR2 to CCLR0 bit: 011B Synchronous clear (clear simultaneously with other timer RDi counter) - CCLR2 to CCLR0 bit: 001B, 010B, 101B, 110B Clear by input capture with TRDGRji register
Count start condition	Write 1 to the STRi bit in the TRDSTR register	Write 1 to the TSTARTi bit in the TRDSTR register
Count stop condition	Write 0 to the STRi bit in the TRDSTR register	Write 0 to the TSTARTi bit in the TRDSTR register
Interrupt request generation timing	- Input capture (Input edge of FTIOji pin) - TRDCNT_i register overflow	- Input capture (Active edge of TRDIOji input) - TRDi register overflow
Acquire timer counter value	Reading TRDCNT_i register	Reading TRDi register
Write timer counter value	- When SYNC bit in TRDMDR register is set to 0 (TRDCNT_1 and TRDCNT_0 operate as independent timer counters). Data can be written to TRDCNT_i register. - When SYNC bit in TRDMDR register is set to 1 (TRDCNT_1 and TRDCNT_0 operate synchronously). Data can be written to both TRDCNT_0 and TRDCNT_1 register by writing to TRDCNT_i register.	- When the TRDSYNC bit in the TRDMR register is set to 0 (TRD0 and TRD1 operate independently). Data can be written to the TRDi register. - When the TRDSYNC bit in the TRDMR register is set to 1 (TRD0 and TRD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Select function	- Input-capture input pin selection - Input-capture input active edge selection - Timing for setting TRDCNT_i register to H'0000 - Buffer operation - Synchronous operation - Digital filter	- Input-capture input pin selection - Input-capture input active edge selection - Timing for setting TRDi register to 0000H - Buffer operation - Synchronous operation - Digital filter - Input capture operation by event input from ELC
Input pin	FTIOji pin	TRDIOji pin

(Notes and Remarks are listed on the next page.)

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Remarks 1. For H8/36109, j = A, B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = A, B, C, D i = 0, 1

2.3 Differences between PWM mode

The PWM mode of the timer RD of the H8/36109 correspond to the timer mode (PWM function) of the Timer RD of the RL78/G14. Table 2.5 and Table 2.6 shows the differences between the PWM mode.

Table 2.5 Differences between the PWM mode (1/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Control of timer RD input clock supply	Setting the MSTTRDi bit in the MSTCR4 register to 0 (Initial value)	Setting the TRD0EN bit in the PER1 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), External clock (Note2)	f_{HOCO} (Note3) ,f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Count mode	Count up	Count up
PWM waveform	PWM period: 1/φ × (m + 1) Duty cycle: 1/φ × (m - n) φ: Frequency of count clock m: Value set in the GRA_j register n: Value set in the GRi_j register	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive level width: 1/fk × (n + 1) fk: Frequency of count clock m: Value set in the TRDGRAi register n: Value set in the TRDGRji register
Count start condition	Write 1 to the STRi bit in the TRDSTR register	Write 1 to the TSTARTi bit in the TRDSTR register
Count stop condition	- When CSTPNi bit in TRDSTR register is set to 1, write 0 to STRi bit. - When CSTPNi bit in TRDSTR register is set to 0, the count stops at the compare match with GRA_i register.	- When CSELi bit in TRDSTR register is set to 1, write 0 to TSTARTi bit. The PWM output pin holds the output level before the count stops. - When CSELi bit in TRDSTR register is set to 0, the count stops at the compare match with the TRDGRAi register. The PWM output pin holds the level after output change by compare match.
Interrupt request generation timing	- Compare match - TRDCNT_i register overflow	- Compare match - TRDi register overflow

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Remarks 1. For H8/36109, j = A, B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = A, B, C, D i = 0, 1

Table 2.6 Differences between the PWM mode (2/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Acquire timer counter value	Reading TRDCNT_i register	Reading TRDi register
Write timer counter value	- When SYNC bit in TRDMDR register is set to 0 (TRDCNT_1 and TRDCNT_0 operate as independent timer counters). Data can be written to TRDCNT_i register. - When SYNC bit in TRDMDR register is set to 1 (TRDCNT_1 and TRDCNT_0 operate synchronously). Data can be written to both TRDCNT_0 and TRDCNT_1 register by writing to TRDCNT_i register.	- When the TRDSYNC bit in the TRDMR register is set to 0 (TRD0 and TRD1 operate independently). Data can be written to the TRDi register. - When the TRDSYNC bit in the TRDMR register is set to 1 (TRD0 and TRD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Output of the timer is disabled by external trigger	Yes	Yes
Select function	- One to three PWM output pins selectable with timer RDi - Active level selectable for each pin - Initial output level selectable for each pin - Buffer operation - Synchronous operation	- One to three PWM output pins selectable with timer RDi - Active level selectable for each pin - Initial output level selectable for each pin - Buffer operation - Synchronous operation - Simultaneous operation (A/D trigger generation etc.) using ELC
Output pin	FTIOBi pin - FTIODipin	TRDIOBi pin - TRDIODi pin

Remarks 1. For H8/36109, j = B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = B, C, D i = 0, 1

2.4 Differences between Reset Synchronous PWM Mode

The Reset Synchronous PWM Mode of the timer RD of the H8/36109 correspond to the Reset Synchronous PWM Mode of the Timer RD of the RL78/G14. Table 2.7 and Table 2.8 shows the differences between the Reset Synchronous PWM Mode.

Table 2.7 Differences between the Reset Synchronous PWM Mode (1/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Control of timer RD input clock supply	Setting the MSTTRDi bit in the MSTCR4 register to 0 (Initial value)	Setting the TRD0EN bit in the PER1 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), External clock (Note2)	f_{HOCO} (Note3) ,f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Count mode	Count up	Count up
PWM waveform	PWM period: 1/φ × (m + 1) Active level of normal-phase: 1/φ × (m - n) Inactive level of counter-phase:1/φ × (n + 1) φ: Frequency of count clock m: Value set in the TRDGRA0_0 register n: Value set in the GRB_0 register (PWM1 output) Value set in the GRA_1 register (PWM2 output) Value set in the GRB_1 register (PWM3 output)	PWM period: 1/fk × (m + 1) Active level of normal-phase: 1/fk × (m - n) Inactive level of counter-phase:1/fk × (n + 1) fk: Frequency of count clock m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output)
Count start condition	Write 1 to the STRi bit in the TRDSTR register	Write 1 to the TSTARTi bit in the TRDSTR register
Count stop condition	- When CSTPN0 bit in TRDSTR register is set to 1, write 0 to STR0 bit. - When CSTPN0 bit in TRDSTR register is set to 0, the count stops at the compare match with GRA_0 register.	- When the CSEL0 bit in the TRDSTR register is set to 1, write 0 to TSTART0 bit. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register. - When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRA0 register. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.
Interrupt request generation timing	- Compare match - TRDCNT_0 register overflow	- Compare match - TRD0 register overflow
Write timer counter value	Reading TRDCNT_0 register	Reading TRD0 register
Write timer counter value	Writing TRDCNT_0 register	Writing TRD0 register
Output of the timer is disabled by external trigger	Yes	Yes

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Table 2.8 Differences between the Reset Synchronous PWM Mode (2/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Toggle output in synchronous with PWM cycle	FTIOC0 pin	TRDIOC0 pin
PWM output 1	FTIOB0 pin	TRDIOB0 pin
PWM output 1 (counter-phase waveform of PWM output 1)	FTIOD0 pin	TRDIOD0 pin
PWM output 2	FTIOA1 pin	TRDIOA1 pin
PWM output 2 (counter-phase waveform of PWM output 2)	FTIOC1 pin	TRDIOC1 pin
PWM output 3	FTIOB1 pin	TRDIOB1 pin
PWM output 3 (counter-phase waveform of PWM output 3)	FTIOD1 pin	TRDIOD1 pin
Select function	- The normal-phase and counter-phase active level and initial output level are selected individually. - Buffer operation - A/D トリガ発生	- The normal-phase and counter-phase active level and initial output level are selected individually. - Buffer operation - Simultaneous operation (A/D trigger generation etc.) using ELC

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

2.5 Differences between Complementary PWM mode

The Complementary PWM mode of the timer RD of the H8/36109 correspond to the Complementary PWM mode of the Timer RD of the RL78/G14. Table 2.9 and Table 2.10 shows the differences between the Complementary PWM mode.

Table 2.9 Differences between the Complementary PWM mode (1/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Control of timer RD input clock supply	Setting the MSTTRDi bit in the MSTCR4 register to 0 (Initial value)	Setting the TRD0EN bit in the PER1 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), External clock (Note2)	f_{HOCO} (Note3) ,f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Count mode	Increment or decrement operation. When TRDCNT_0 and GRA_0 are compared and their contents match, the counter is decremented, and when TRDCNT_1 underflow, the counter is incremented.	Increment or decrement. Registers TRD0 and TRD1 are decremented with the compare match with registers TRD0 and TRDGRA0 during increment operation. When the TRD1 register changes from 0000H to FFFFH during decrement operation, and registers TRD0 and TRD1 are incremented.
PWM 波形	PWM period: 1/φ × (m + 2 - p) × 2 Non-overlapped period: p Active level width of normal-phase: 1/φ × (m - n - p + 1) × 2 Active level width of counter-phase: 1/φ × (n + 1 - p) × 2 φ: Frequency of count source m: Value set in the GRA_0 register n: Value set in the GRB_0 register (PWM1 output) Value set in the GRA_1 register (PWM2 output) Value set in the GRB_1 (PWM3 output) Non-overlapped period: Value set in the TRDCNT_0 register	PWM period: 1/fk × (m + 2 - p) × 2 (Note4) Dead time: p Active level width of normal-phase: 1/fk × (m - n - p + 1) × 2 Active level width of counter-phase: 1/fk × (n + 1 - p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) TValue set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register
Count start condition	Write 1 to the STR0 bit in the TRDSTR register	Write 1 to the TSTART0 bit and TSTART1 bit in the TRDSTR register
Count stop condition	Clear bit CMD1 in TRDFCR to 0, and set channels 0 and 1 to normal operation. After setting channels 0 and 1 to normal operation, clear bits STR0 and STR1 in TRDSTR to 0 and stop TRDCNT_0 and TRDCNT_1.	When the CSEL0 bit in the TRDSTR register is set to 1, write 0 to TSTART0 bit and TSTART1 bit. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Remarks 1. For H8/36109, j = B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = B, C, D i = 0, 1

Table 2.10 Differences between the Complementary PWM mode (2/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Interrupt request generation timing	- Compare match between TRDCNT_0 and GRA_0 - TRDCNT_1 register underflow - Compare match (GRB_0, GRA_1, GRB_1)	- Compare match (content of the TRDi register matches content of the TRDGRji register) - TRD1 register underflow
Acquire timer counter value	Reading TRDCNT_0, TRDCNT_1 register	Reading TRDi register
Write timer counter value	Writing TRDCNT_0, TRDCNT_1 register	Writing TRDi register
Output of the timer is disabled by external trigger	Yes	Yes
Output inverted every 1/2 period of PWM	FTIOC0 pin	TRDIOC0 pin
PWM1 output normal-phase output	FTIOB0 pin	TRDIOB0 pin
PWM1 output counter-phase output	FTIOD0 pin	TRDIOD0 pin
PWM2 output normal-phase output	FTIOA1 pin	TRDIOA1 pin
PWM2 output counter-phase output	FTIOC1 pin	TRDIOC1 pin
PWM3 output normal-phase output	FTIOB1 pin	TRDIOB1 pin
PWM3 output counter-phase output	FTIOD1 pin	TRDIOD1 pin
Select function	- The normal-phase and counter-phase active level and initial output level are selected individually. - Transfer timing from the buffer register selection - A/D conversion start trigger	- The normal-phase and counter-phase active level and initial output level are selected individually. - Transfer timing from the buffer register selection - Simultaneous operation (A/D trigger generation etc.) using ELC

Remarks 1. For H8/36109, j = B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = B, C, D i = 0, 1

2.6 Differences between PWM3 mode

The PWM3 mode of the timer RD of the H8/36109 correspond to the PWM3 mode of the Timer RD of the RL78/G14. Table 2.11 and Table 2.12 shows the differences between the PWM3 mode.

Table 2.11 Differences between the PWM3 mode (1/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Control of timer RD input clock supply	Setting the MSTTRDi bit in the MSTCR4 register to 0 (Initial value)	Setting the TRD0EN bit in the PER1 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), External clock (Note2)	f_{HOCO} (Note3) ,f_{CLK}, f_{CLK}/2, f_{CLK}/4, f_{CLK}/8, f_{CLK}/32, TRDCLK input (Note2)
Count mode	The TRDCNT0 register is incremented (the TRDCNT1 register is not used)	The TRD0 register is incremented (the TRD1 register is not used)
PWM waveform	PWM period: 1/φ × (m + 1) Active level width of FTIOA0 output: 1/φ × (m - n) Active level width of FTIOB0 output: 1/φ × (p - q) φ: Frequency of count clock m: Value set in the GRA_0 register n: Value set in the GRA_1 register p: Value set in the GRB_0 register q: Value set in the GRB_1 register	PWM period: 1/fk × (m + 1) Active level width of TRDIOA0 output: 1/fk × (m - n) Active level width of TRDIOB0 output: 1/fk × (p - q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register
Count start condition	Write 1 to the STR0 bit in the TRDSTR register	Write 1 to the TSTART0 bit in the TRDSTR register
Count stop condition	- When CSTPNi bit in TRDSTR register is set to 1, write 0 to STRi bit. - When CSTPNi bit in TRDSTR register is set to 0, the count stops at the compare match with the GRA_i register.	- When CSEL0 bit in TRDSTR register is set to 1, write 0 to TSTART0 bit. The PWM output pin holds the output level before the count stops. - When CSEL0 bit in TRDSTR register is set to 0, the count stops at the compare match with the TRDGRA0 register. The PWM output pin holds the level after output change by compare match.
Interrupt request generation timing	- Compare match (content of the TRDCNT_0 register matches content of the GRj_i register) - TRDCNT_0 register overflow	- Compare match (content of the TRD0 register matches content of the TRDGRji register) - TRD0 register overflow

Note 1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note 2. Valid when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Note 3. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H).

Remarks 1. For H8/36109, j = B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Remarks 2. For RL78/G14, j = B, C, D i = 0, 1

Table 2.12 Differences between the PWM3 mode (2/2)

Item	H8/36109 Timer RD	RL78/G14 Timer RD
Acquire timer counter value	Reading TRDCNT_0 register	Reading TRD0 register
Write timer counter value	Writing TRDCNT_0 register	Writing TRD0 register
Output of the timer is disabled by external trigger	Yes	Yes
PWM output normal-phase output	FTIOA0 pin	TRDIOA0 pin
PWM output counter-phase output	FTIOB0 pin	TRDIOB0 pin
Select function	- Active level selectable for each pin - Buffer operation - A/D conversion start trigger	- Active level selectable for each pin - Buffer operation - Simultaneous operation (A/D trigger generation etc.) using ELC

Remarks. For H8/36109, j = B, C, D i = 0, 1
Timer RD_1 has the same functions as timer RD_0. Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

3. Comparison between Registers

Table 3.1 to Table 3.5 compares the registers for the H8/36109 Timer RD and the registers for the RL78/G14 Timer RD.

Table 3.1 Comparison between Registers (1/5)

Item	H8/36109	RL78/G14
Control of timer RD input clock supply	MSTCR4 register MSTTRD0 bit, MSTTRD1 bit	PER1 register TRD0EN bit
Timer RD start register	TRDSTR register	
Channel 1 Counter Stop	TRDSTR register CSTPN1 bit	TRDSTR register CSEL1 bit
Channel 0 Counter Stop	TRDSTR register CSTPN0 bit	TRDSTR register CSEL0 bit
Channel 1 Counter Start	TRDSTR register STR1 bit	TRDSTR register TSTART1 bit
Channel 0 Counter Start	TRDSTR register STR0 bit	TRDSTR register TSTART0 bit
Timer RD mode register	TRDMDR register	TRDMR register
Buffer Operation D1	TRDMDR register BFD1 bit	TRDMR register TRDBFD1 bit
Buffer Operation C1	TRDMDR register BFC1 bit	TRDMR register TRDBFC1 bit
Buffer Operation D0	TRDMDR register BFD0 bit	TRDMR register TRDBFD0 bit
Buffer Operation C0	TRDMDR register BFC0 bit	TRDMR register TRDBFC0 bit
Timer Synchronization	TRDMDR register SYNC bit	TRDMR register TRDSYNC bit
Timer RD PWM mode register	TRDPMR register	TRDPMR register
PWM Mode D1	TRDPMR register PWMD1 bit	TRDPMR register TRDPWMD1 bit
PWM Mode C1	TRDPMR register PWMC1 bit	TRDPMR register TRDPWMC1 bit
PWM Mode B1	TRDPMR register PWMB1 bit	TRDPMR register TRDPWMB1 bit
PWM Mode D0	TRDPMR register PWMD0 bit	TRDPMR register TRDPWMD0 bit
PWM Mode C0	TRDPMR register PWMC0 bit	TRDPMR register TRDPWMC0 bit
PWM Mode B0	TRDPMR register PWMB0 bit	TRDPMR register TRDPWMB0 bit

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Table 3.2 Comparison between Registers (2/5)

Item	H8/36109	RL78/G14
Timer RD function control register	TRDFCR register	TRDFCR register
PWM3 Mode Select	TRDFCR register PWM3 bit	TRDFCR register PWM3 bit
External Clock Input Select	TRDFCR register STCLK bit	TRDFCR register STCLK bit
A/D Trigger Edge Select	TRDFCR register ADEG bit	None
External Trigger Disable	TRDFCR register ADTRG bit	None
Output Level Select 1	TRDFCR register OLS1 bit	TRDFCR register OLS1 bit
Output Level Select 0	TRDFCR register OLS0 bit	TRDFCR register OLS0 bit
Combination Mode 1 and 0	TRDFCR register CMD1 bit, CMD0 bit	TRDFCR register CMD1 bit, CMD0 bit
Timer RD output master enable register 1	TRDOER1 register	TRDOER1 register
Master Enable D1	TRDOER1 register ED1 bit	TRDOER1 register ED1 bit
Master Enable C1	TRDOER1 register EC1 bit	TRDOER1 register EC1 bit
Master Enable B1	TRDOER1 register EB1 bit	TRDOER1 register EB1 bit
Master Enable A1	TRDOER1 register EA1 bit	TRDOER1 register EA1 bit
Master Enable D0	TRDOER1 register ED0 bit	TRDOER1 register ED0 bit
Master Enable C0	TRDOER1 register EC0 bit	TRDOER1 register EC0 bit
Master Enable B0	TRDOER1 register EB0 bit	TRDOER1 register EB0 bit
Master Enable A0	TRDOER1 register EA0 bit	TRDOER1 register EA0 bit
Timer RD output master enable register 2	TRDOER2 register	TRDOER2 register
Timer Output Disabled Mode	TRDOER2 register PTO bit	TRDOER2 register TRDPTO bit
Forced cutoff flag	None	TRDOER2 register TRDSHUTS bit

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Table 3.3 Comparison between Registers (3/5)

Item	H8/36109	RL78/G14
Timer RD Output Control Register	TRDOCR register	TRDOCR register
Output Level Select D1	TRDOCR register TOD1 bit	TRDOCR register TOD1 bit
Output Level Select C1	TRDOCR register TOC1 bit	TRDOCR register TOC1 bit
Output Level Select B1	TRDOCR register TOB1 bit	TRDOCR register TOB1 bit
Output Level Select A1	TRDOCR register TOA1 bit	TRDOCR register TOA1 bit
Output Level Select D0	TRDOCR register TOD0 bit	TRDOCR register TOD0 bit
Output Level Select C0	TRDOCR register TOC0 bit	TRDOCR register TOC0 bit
Output Level Select B0	TRDOCR register TOB0 bit	TRDOCR register TOB0 bit
Output Level Select A0	TRDOCR register TOA0 bit	TRDOCR register TOA0 bit
Timer RD Counter_0	TRDCNT_0 register	TRD0 register
Timer RD Counter_1	TRDCNT_1 register	TRD1 register
General Register A_0	GRA_0 register	TRDGRA0 register
General Register B_0	GRB_0 register	TRDGRB0 register
General Register C_0	GRC_0 register	TRDGRC0 register
General Register D_0	GRD_0 register	TRDGRD0 register
General Register A_1	GRA_1 register	TRDGRA1 register
General Register B_1	GRB_1 register	TRDGRB1 register
General Register C_1	GRC_1 register	TRDGRC1 register
General Register D_1	GRD_1 register	TRDGRD1 register
Timer RD I/O Control Register	TRDCR register	TRDCRi register
Counter Clear 2 to 0	TRDCR register CCLR2 - CCLR0 bit	TRDCRi register CCLR2 - CCLR0 bit
Clock Edge 1 and 0	TRDCR register CKEG1 bit, CKEG0 bit	TRDCRi register CKEG1 bit, CKEG0 bit
Time Prescaler 2 to 0	TRDCR register TPSC2 - TPSC0 bit	TRDCRi register TCK2 - TCK0 bit

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Table 3.4 Comparison between Registers (4/5)

Item	H8/36109	RL78/G14
Timer RD I/O Control Register A	TRDIORA register	TRDIORAi register
I/O Control B2	TRDIORA register IOB2 bit	TRDIORAi register IOB2 bit
I/O Control B1, B0	TRDIORA register IOB1, IOB0 bit	TRDIORAi register IOB1, IOB0 bit
I/O Control A2	TRDIORA register IOA2 bit	TRDIORAi register IOA2 bit
I/O Control A1, A0	TRDIORA register IOA1 bit, IOA0 bit	TRDIORAi register IOA1 bit, IOA0 bit
Timer RD I/O Control Register C	TRDIORC register	TRDIORCi register
I/O Control D3	TRDIORC register IOD3 bit	TRDIORCi register IOD3 bit
I/O Control D2	TRDIORC register IOD2 bit	TRDIORCi register IOD2 bit
I/O Control D1, D0	TRDIORC register IOD1, IOD0 bit	TRDIORCi register IOD1, IOD0 bit
I/O Control C3	TRDIORC register IOC3 bit	TRDIORCi register IOC3 bit
I/O Control C2	TRDIORC register IOC2 bit	TRDIORCi register IOC2 bit
I/O Control C1, C0	TRDIORC register IOC1 bit, IOC0 bit	TRDIORCi register IOC1 bit, IOC0 bit
Timer RD Status Register	TRDSR register	TRDSRi register
Underflow Flag	TRDSR register UDF bit	TRDSR1 register UDF bit
Overflow Flag	TRDSR register OVF bit	TRDSRi register OVF bit
Input Capture/Compare Match Flag D	TRDSR register IMFD bit	TRDSRi register IMFD bit
Input Capture/Compare Match Flag C	TRDSR register IMFC bit	TRDSRi register IMFC bit
Input Capture/Compare Match Flag B	TRDSR register IMFB bit	TRDSRi register IMFB bit
Input Capture/Compare Match Flag A	TRDSR register IMFA bit	TRDSRi register IMFA bit

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

Table 3.5 Comparison between Registers (5/5)

Item	H8/36109	RL78/G14
Timer RD Interrupt Enable Register	TRDIER register	TRDIERi register
Overflow Interrupt Enable	TRDIER register OVIE bit	TRDIERi register OVIE bit
Input Capture/Compare Match Interrupt Enable D	TRDIER register IMIED bit	TRDIERi register IMIED bit
Input Capture/Compare Match Interrupt Enable C	TRDIER register IMIEC bit	TRDIERi register IMIEC bit
Input Capture/Compare Match Interrupt Enable B	TRDIER register IMIEB bit	TRDIERi register IMIEB bit
Input Capture/Compare Match Interrupt Enable A	TRDIER register IMIEA bit	TRDIERi register IMIEA bit
PWM Mode Output Level Control Register	POCR register	TRDPOCRi register
PWM Mode Output Level Control D	POCR register POLD bit	TRDPOCRi register POLD bit
PWM Mode Output Level Control C	POCR register POLC bit	TRDPOCRi register POLC bit
PWM Mode Output Level Control B	POCR register POLB bit	TRDPOCRi register POLB bit
Timer RD Digital Filtering Function Select Register	TRDDF register	TRDDFi register
Select the clock to be used by the digital filter	TRDDF register DFCK1 bit, DFCK0 bit	TRDDFi register DFCK1 bit, DFCK0 bit
Enables or disables the digital filter for the FTIOD pin	TRDDF register DFD bit	TRDDFi register DFD bit
Enables or disables the digital filter for the FTIOC pin	TRDDF register DFC bit	TRDDFi register DFC bit
Enables or disables the digital filter for the FTIOB pin	TRDDF register DFB bit	TRDDFi register DFB bit
Enables or disables the digital filter for the FTIOA pin	TRDDF register DFA bit	TRDDFi register DFA bit
Timer RD ELC register	None	TRDELC register

Remarks. For H8/36109,Timer RD_1 has the same functions as timer RD_0.
Therefore, the unit number (_0 or _1) is not explicitly mentioned in this section unless otherwise noted.

4. Sample Code for Timer RD

The sample code for the Timer RD is explained in the following application notes.

- RL78/G14 Timer RD Using Input Capture Function and Output Compare Function CC-RL (R01AN 2852)
- RL78/G14 Timer RD in Timer Mode (PWM Function) CC-RL (R01AN2851)
- RL78/G14 Timer RD in Reset Synchronous PWM Mode CC-RL (R01AN2506)
- RL78/G14 Timer RD in Complementary PWM Mode CC-RL (R01AN2572)
- RL78/G14 Timer RD in PWM3 Mode CC-RL (R01AN2781)

5. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan.23, 2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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