RL78/G14, H8/36109

Migration Guide from H8 to RL78: Timer RC

Introduction

This application note describes how to migrate the Timer RC of the H8/36109 to the timer array unit (TAU) of the RL78/G14.

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of Timer RC of H8/36109 and Timer Array Unit of RL78/G14

Table 1.1 shows the functions of the Timer RC of H8/36109, and Table 1.2 shows the functions of the timer array unit (TAU) of RL78/G14.

Table 1.1 Functions Timer RC

Function	Explanation
Timer mode (Output compare function)	0, 1, or toggle is output from the FTIOA, FTIOB, FTIOC, and FTIOD pins.
Timer mode (Input capture function)	Input edges in the FTIOA, FTIOB, FTIOC, and FTIOD pins are detected and TRDCNT values are transferred to GRA, GRB, GRC, and GRD.
PWM mode	PWM waveforms are output from the FTIOB, FTIOC, and FTIOD pins.
PWM2 mode	Waveforms are output on the FTIOB pin when a compare match occurs on GRB or GRC.

Table 1.2 Functions of Timer Array Unit

Function	Explanation
Interval timer	Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.
Square wave output	A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOmn).
External event counter	Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TImn) has reached a specific value.
Divider	A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).
Input pulse interval measurement	Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.
Measurement of high-/low-level width of input signal	Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.
Delay counter	Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period.
One-shot pulse output	Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.
PWM output	Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.
Multiple PWM output	By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.

Timer RC of H8/36109 is a 16-bit timer having output compare and input capture functions. Timer RC can count external events and output pulses with a desired duty cycle using the compare match function between the timer counter and four general registers. Thus, it can be applied to various systems.

Figure 1.1 shows a block diagram of the Timer RC.

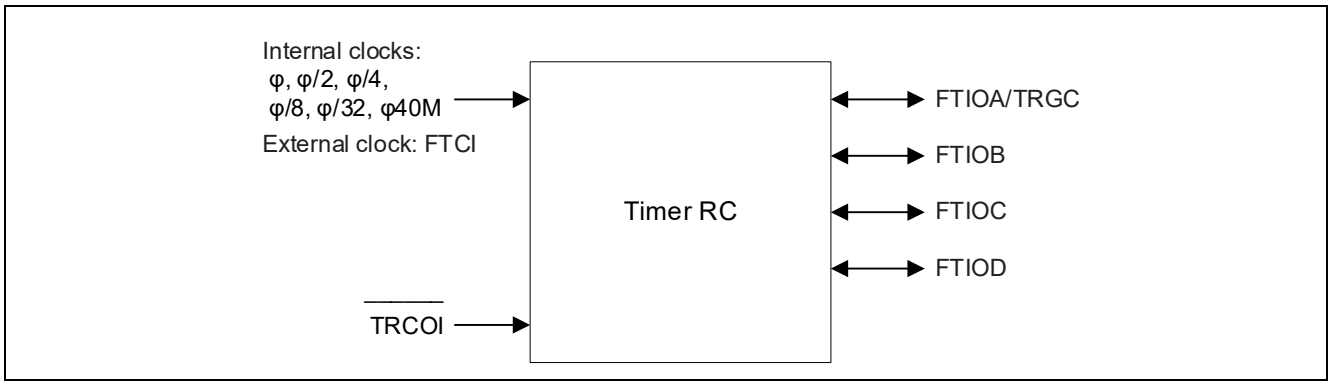

Figure 1.1 Block diagram of the Timer RC

The timer array unit (TAU) incorporated in the RL78/G14 has four 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be combined to serve as a higher-accuracy timer.

Each channel has one timer counter register, one timer data register, one input pin, and one output pin.

Figure 1.2 shows a block diagram of the timer array unit (TAU).

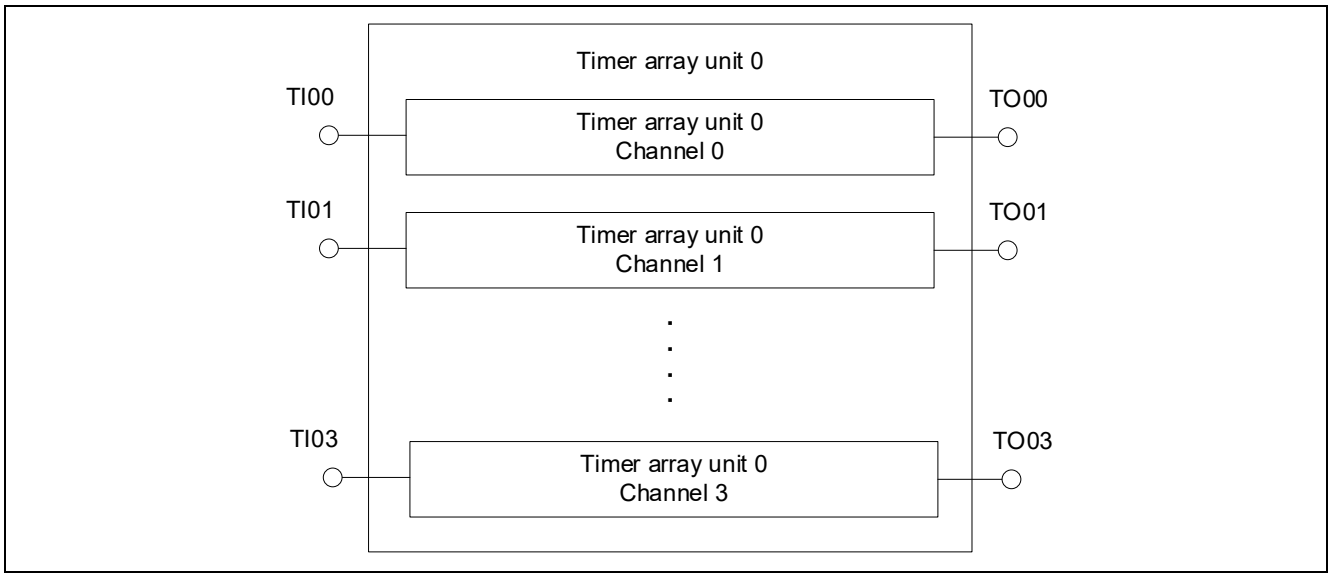

Figure 1.2 Block Diagram of Timer Array Unit

Table 1.3 shows the TAU functions corresponding to the Timer RC.

Table 1.3 Correspondence between Functions

H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU)
Timer mode (Output compare function)	Interval timer / Square wave output, Divider
Timer mode (Input capture function)	Input pulse interval measurement, External event counter, Measurement of high-/low-level width of input signal
PWM mode	PWM output, Multiple PWM output
PWM2 mode	None

The timer array unit (TAU) can implement the functions equivalent to those provided in the Timer RC by using each channel independently or a combination of multiple channels simultaneously.

Timer mode (Output compare function) of the Timer RC corresponds to the Interval timer/Square wave output, or Divider of the TAU. This application note describes the differences between the timer mode (output compare function) of the timer RC and the interval timer of the TAU.

Timer mode (input capture function) of the Timer RC corresponds to the input pulse interval measurement/external event counter, or input signal high-/low-level width measurement of the TAU. This application note describes the differences between timer mode (input capture function) of the timer RC and the input pulse interval measurement of the TAU.

PWM mode of Timer RC corresponds to the Multiple PWM output of the TAU.

The equivalent function to PWM2 mode of the Timer RC is not incorporated in the TAU.

2. Summary of Differences between Functions

Table 2.1 summarizes the differences between the functions of Timer RC and TAU.

Table 2.1 Summary of Differences between Functions

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU)
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note1), FTCI(Note2)	f_{TCLK} (f_{CLK}, to $f_{CLK}/2^{15}$), f_{SUB}(Note3), f_{IL}(Note3)
Maximum operating frequency	40MHz (Note4)	32MHz (Note5)
Operation Mode	Timer mode (Output compare function) Timer mode (Input capture function) PWM mode PWM2 mode	- Interval timer - Square wave output - External event counter - Frequency divider - Input pulse interval measurement - Input signal high-/low-level width measurement - Delay counter - One-shot pulse output function - PWM output - Multiple PWM output
Buffer operation	Yes	Yes
Timer output disabled mode (pulse output forced cutoff)	Yes	None
How to generate the timer output disable mode	Setting the PTO bit in the TRCOER register to 1 and then inputting a low level signal to the TRCOI pin.	None
Operation mode in which the timer output disabling function can be used	- Timer mode (Output compare function) - PWM mode - PWM2 mode	None
How to set pin state in timer output disabled mode	Setting the I/O ports shared with the TRCIOi pins	None
Shared pin	PG5 / $\overline{\text{TRCOI}}$ PH3 / FTCI PH4 / FTIOA, PH5 / FTIOB PH6 / FTIOC, PH7 / FTIOD	Unit 0: P00 / TI00, P01 / TO00, P16 / TI01 / TO01 P17 / TI02 / TO02, P31 / TI03 / TO03 Unit 1: TI10 / TO10 / P64, TI11 / TO11 / P65 TI12 / TO12 / P66, TI13 / TO13 / P67
Interrupt source	Compare match / Input capture, Overflow	Compare match / Input capture, Overflow, Underflow

Note1. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note2. Count the rising edge of the external event (FTCI)

Note3. Channel 1 only

Note4. Maximum operating frequency of on-chip oscillator

Note5. Maximum operating frequency of main system clock frequency

Remark. For H8/36109, i = A, B, C, D

2.1 Differences between Timer mode (Output compare function)

The timer mode (Output compare function) of timer RC of the H8/36109 correspond to the square wave output of the TAU of the RL78/G14. Table 2.2 shows the differences between the timer mode (Output compare function).

Table 2.2 Differences between the timer mode (Output compare function)

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU) Square wave output
Control of timer RC input clock supply	Setting the MSTTRC bit in the MSTCR4 register to 0 (Initial value)	Setting the TAU1EN(Note1) bit or TAU0EN bit in the PER0 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M (Note2), External clock (FTCI) (Note3)	f_{TCLK} (f_{CLK}, to $f_{CLK}/2^{15}$), f_{SUB} (Note4), f_{IL} (Note4)
Count mode	- Count up - The TRCCNT value is cleared by compare match A (CCLR bit in TRCCR1 is ”1”)	Count down The TCRmn register is loaded with the TDRmn register value at the next count clock after TCRmn = 0000H.
Output inversion timing	Compare match	The next count clock after TCRmn = 0000H
Count start condition	Setting the CTS bit in the TRCMR register to 1	Setting the TSmn bit in the TSm register to 1
Count stop condition	Setting the CTS bit in the TRCMR register to 0	Setting the TTmn bit in the TTm register to 1
Interrupt request generation timing	- Compare match - TRCCNT register overflow	- When TCRmn reaches 0000H and then the next count clock pulse is generated - When count operation starts (only if MDmn0 bit in TMRmn register is set to 1)
Acquire timer counter value	Reading TRCCNT register	Reading TCRmn register
Write timer counter value	Writing TRCCNT register	None (Writing TDRmn register)
Output of the timer is disabled by external trigger (Pulse forced cutoff control)	Yes	None
Selectable functions	- Output level selection at compare match - Initial output level selection - Buffer operation	- Interrupt request generation at count start - Default level of TOmn pin
Output pin	FTIOi pin	TOmn pin

Note1. 80 and 100-pin products only.

Note2. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note3. Count the rising edge of the external event (FTCI)

Note4. Channel 1 only

Remarks1. For H8/36109, i = A, B, C, D

Remarks2. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0-3)

2.2 Differences between Timer mode (Input capture function)

The timer mode (Input capture function) of timer RC of the H8/36109 correspond to the input pulse interval measurement of the TAU of the RL78/G14. Table 2.3 shows the differences between the timer mode (Input capture function).

Table 2.3 Differences between the timer mode (Input capture function)

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU) Input pulse interval measurement
Control of timer RC input clock supply	Setting the MSTTRC bit in the MSTCR4 register to 0 (Initial value)	Setting the TAU1EN(Note1) bit or TAU0EN bit in the PER0 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note2), External clock (Note3)	f_{TCLK} (f_{CLK}, to $f_{CLK}/2^{15}$), f_{SUB}(Note4), f_{IL}(Note4)
Count mode	- Count up - TRCCR1 register CCLR = 0: TRCCNT functions as a free-running counter CCLR = 1: The TRCCNT value is cleared by compare match A	Count up When the TImn pin input valid edge is detected, the TCRmn register is cleared to 0000H.
Input capture timing	When the valid input edge is detected in the FTIOi pin.	When the valid input edge is detected in the TImn pin.
Count start condition	Setting the CTS bit in the TRCMR register to 1	Setting the TSmn bit in the TSm register to 1
Count stop condition	Setting the CTS bit in the TRCMR register to 0	Setting the TTmn bit in the TTm register to 1
Interrupt request generation timing	- When valid edge of input capture is detected - TRCCNT register overflow	- When count operation starts (only if MDmn0 bit in TMRmn register is set to 1) - When the valid input edge is detected in the TImn pin.
Acquire timer counter value	Reading TRCCNT register	Reading TCRmn register
Write timer counter value	Writing TRCCNT register	None
Selectable functions	- Select the input capture valid edge - Buffer operation - Digital filter	- Valid edge select - Noise filter
Input pin	FTIOi pin	TImn pin

Note1. 80 and 100-pin products only.

Note2. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note3. Count the rising edge of the external event (FTCI)

Note4. Channel 1 only

Remarks1. For H8/36109, i = A, B, C, D

Remarks2. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0-3)

2.3 Differences between PWM mode

The PWM mode of the timer RC of the H8/36109 correspond to the PWM function or multiple PWM output function of the TAU of the RL78/G14. Table 2.4 shows the differences between the PWM mode.

Table 2.4 Differences between PWM mode

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU) PWM mode, multiple PWM output function
Control of timer RC input clock supply	Setting the MSTTRC bit in the MSTCR4 register to 0 (Initial value)	Setting the TAU1EN(Note1) bit or TAU0EN bit in the PER0 register to 1
Count clock	φ, φ/2, φ/4, φ/8, φ/32, φ40M(Note2), External clock (FTCI)(Note3)	f_{TCLK} (f_{CLK}, to $f_{CLK}/2^{15}$), f_{SUB}(Note4), f_{IL}(Note4)
Count mode	Count up	Count down
PWM waveform	PWM period: 1/φ × (m + 1) Duty cycle: 1/φ × (m - n) φ: Frequency of count clock m: Value set in the GRA register n: Value set in the GRi register	Pulse period = { Set value of TDRmn (master) + 1 } × Count clock period Duty factor [%] = { Set value of TDRmp (slave) } / { Set value of TDRmn (master) + 1} × 100
Count start condition	Setting the CTS bit in the TRCMR register to 1	Setting the TSmn bit in the TSm register to 1
Count stop condition	Setting the CTS bit in the TRCMR register to 0	Setting the TTmn bit in the TTm register to 1
Interrupt request generation timing	- Compare match	- When count operation starts (only if MDmn0 bit in TMRmn register is set to 1) - When TCRmn reaches 0000H and then the next count clock is generated. - When TCRmp reaches 0000H and then the next count clock is generated.
Acquire timer counter value	Reading TRCCNT register	Reading TCRmn, TCRmp register
Write timer counter value	Writing TRCCNT register	Writing TDRmn, TDRmp register
Output of the timer is disabled by external trigger (Pulse forced cutoff control)	Yes	None
Selectable functions	- One to three PWM output pins selectable - Active level selectable for each pin - Initial output level selectable for each pin - Buffer operation	- Output pin level when pulse output is started - Active high / low level selection
Output pin	FTIOi pin	TOmp pin

Note1. 80 and 100-pin products only.

Note2. 40-MHz/32-MHz clock derived from the on-chip oscillator

Note3. Count the rising edge of the external event (FTCI)

Note4. Channel 1 only

Remarks 1. For H8/36109, i = B, C, D

Remarks 2. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

3. Comparison between Registers

Table 3.1 to Table 3.3 compares the registers for the H8/36109 Timer RC and the registers for the RL78/G14 Timer Array Unit.

Table 3.1 Comparison between Registers (1/3)

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU)
Control of timer RC input clock supply	MSTCR4 register MSTTRC bit	None
Control of timer array unit input clock	None	PER0 register TAU1EN bit (Note), TAU0EN bit
Timer RC Mode Register	TRCMR register	None
Counter Start	TRCMR register CTS bit	TSm register TSmn bit
Timer channel stop register	None	TTm register
Buffer Operation B	TRCMR register BUFEB bit	None
Buffer Operation A	TRCMR register BUFEA bit	None
PWM2 Mode	TRCMR register PWM2 bit	None
PWM Mode D	TRCMR register PWMD bit	TMRmn register MDmn3 - MDmn1 bit
PWM Mode C	TRCMR register PWMC bit	
PWM Mode B	TRCMR register PWMB bit	
Timer RC Control Register 1	TRCCR1 register	None
Counter Clear	TRCCR1 register CCLR bit	None
Clock Select 2 to 0	TRCCR1 register CKS2 - CKS0 bit	TPSm register TMRmn register CKSmn1 bit, CKSmn0 bit
Timer Output Level Setting	TRCCR1 register TOD bit, TOC bit, TOB bit, TOA bit	TOm register TOmn bit
Timer RC Control Register 2	TRCCR2 register	None
TRGC Input Edge Select	TRCCR2 register TCEG1 bit, TCEG0 bit	None
Specifies whether TRCCNT counting up is halted or continued by the compare match A signal	TRCCR2 register CSTP bit	None

Note. 80 and 100-pin products only.

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

Table 3.2 Comparison between Registers (2/3)

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU)
Timer RC Interrupt Enable Register	TRCIER register	None
Timer Overflow Interrupt Enable	TRCIER register OVIE bit	None
Input Capture/Compare Match Interrupt Enable D	TRCIER register IMIED bit	None
Input Capture/Compare Match Interrupt Enable C	TRCIER register IMIEC bit	None
Input Capture/Compare Match Interrupt Enable B	TRCIER register IMIEB bit	None
Input Capture/Compare Match Interrupt Enable A	TRCIER register IMIEA bit	None
Timer RC Status Register	TRCSR register	None
Timer Overflow Flag	TRCSR register OVF bit	TSRmn register OVF bit
Input Capture/Compare Match Flag D	TRCSR register IMFD bit	None
Input Capture/Compare Match Flag C	TRCSR register IMFC bit	None
Input Capture/Compare Match Flag B	TRCSR register IMFB bit	None
Input Capture/Compare Match Flag A	TRCSR register IMFA bit	None
Timer RC I/O Control Register 0	TRCIOR0 register	None
Timer RC I/O Control Register 1	TRCIOR1 register	None
I/O Control B2, B1, B0	TRCIOR0 register IOB2 - IOB0 bit	TMRmn register CISmn1 bit, CISmn0 bit
I/O Control A2, A1, A0	TRCIOR0 register IOA2 - IOA0 bit	
I/O Control D2, D1, D0	TRCIOR1 register IOD2 - IOD0 bit	
I/O Control C2, C1, C0	TRCIOR1 register IOC2 - IOC0 bit	
Timer RC Output Enable Register	TRCOER register	None
Timer Output Disabled Mode	TRCOER register PTO bit	None
Master Enable	TRCOER register ED bit, EC bit EB bit, EA bit	TOEm register TOEm3 - TOEm0 bit

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

Table 3.3 Comparison between Registers (3/3)

Item	H8/36109 Timer RC	RL78/G14 Timer Array Unit (TAU)
Timer RC Digital Filtering Function Select Register	TRCDF register	None
Select the clock to be used by the digital filter	TRCDF register DFCK1 bit, DFCK0 bit	None
Enables or disables the digital filter for the TRGC pin	TRCDF register DFTRG bit	NFEN1 register, NFEN2 register
Enables or disables the digital filter for the FTIOD - FTIOA pin	TRCDF register DFD bit, DFC bit DFB bit, DFA bit	NFEN1 register, NFEN2 register
Timer RC Counter	TRCCNT register	TCRmn register
General Registers	GRA register, GRB register GRC register, GRD register	TDRmn register
Selection of count clock (f_{TCLK}) of channel n	None	TMRmn register CCSmn bit
Selection between using channel n independently or simultaneously with another channel (as a slave or master)	None	TMRmn register MASTERmn bit
Selection of 8 or 16-bit timer operation for channels 1 and 3	None	TMRmn register SPLITmn bit
Setting of start trigger or capture trigger of channel n	None	TMRmn register STSmn2 - STSmn0 bit
Setting of starting counting and interrupt	None	TMRmn register MDmn0 bit
Timer channel enable status register	None	TEm register
Selection of timer input used with channel 0	None	TIS0 register TIS04 bit
Selection of timer input used with channel 1	None	TIS0 register TIS02 - TIS00 bit
Control of timer output level of channel n	None	TOLm register TOLmn bit
Control of timer output mode of channel n	None	TOMm register TOMmn bit
Input switch control register	None	ISC register SSIE00 bit ISC1 bit, ISC0 bit

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
p: Slave channel number (n = 0: p = 1, 2, 3; n = 2: p = 3)

4. Sample Code for Timer Array Unit

The sample code for the timer Array Unit is explained in the following application notes.

- RL78/G13 Timer Array Unit (Interval Timer) CC-RL (R01AN2576)
- RL78/G13 Timer Array Unit (Pulse Interval Measurement) CC-RL (R01AN2702)
- RL78/G13 Timer Array Unit (Pulse Interval Measurement (Both edges)) CC-RL (R01AN4259)
- RL78/G13 Timer Array Unit (PWM Output) CC-RL (R01AN2589)

5. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.19, 2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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