RL78/F23, F24
List of Special Function Registers

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Introduction

The purpose of this application note is to show all special function registers (SFRs) used for each model of the RL78/F23 and F24 microcontrollers.

For details, be sure to refer to User's Manual: Hardware.

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1. List of Special Function Registers for RL78/F23, F24

The table below lists the special function registers (SFR) for RL78/F23, F24 products.

Table 1-1. List of Special Function Registers (SFR) for RL78/F23, F24 (1/4)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
FFF00H	Port register 0	P0	00H	1, 8	√	√	√	√	—	√	√	√	—
FFF01H	Port register 1	P1	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF03H	Port register 3	P3	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF04H	Port register 4	P4	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF05H	Port register 5	P5	00H	1, 8	√	√	√	—	—	√	√	—	—
FFF06H	Port register 6	P6	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF07H	Port register 7	P7	00H	1, 8	√	√	√	√	—	√	√	√	—
FFF08H	Port register 8	P8	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF09H	Port register 9	P9	00H	1, 8	√	√	√	√	—	√	√	√	—
FFF0AH	Port register 10	P10	00H	1, 8	√	—	—	—	—	—	—	—	—
FFF0CH	Port register 12	P12	UND	1, 8	√	√	√	√	√	√	√	√	√
FFF0DH	Port register 13	P13	UND	1, 8	√	√	√	√	√	√	√	√	√
FFF0EH	Port register 14	P14	00H	1, 8	√	√	√	√	—	√	√	√	—
FFF0FH	Port register 15	P15	00H	1, 8	√	—	—	—	—	—	—	—	—
FFF10H	Serial data register 00	SDR00	0000H	16	√	√	√	√	√	√	√	√	√
		SDR00L		8									
FFF11H		—		—									
FFF12H	Serial data register 01	SDR01	0000H	16	√	√	√	√	√	√	√	√	√
		SDR01L		8									
FFF13H		—		—									
FFF18H FFF19H	Timer data register 00	TDR00	0000H	16	√	√	√	√	√	√	√	√	√
FFF1AH	Timer data register 01	TDR01	0000H	16	√	√	√	√	√	√	√	√	√
		TDR01L		8									
FFF1BH		TDR01H		8									
FFF20H	Port mode register 0	PM0	FFH	1, 8	√	√	√	√	—	√	√	√	—
FFF21H	Port mode register 1	PM1	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFF23H	Port mode register 3	PM3	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFF24H	Port mode register 4	PM4	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFF25H	Port mode register 5	PM5	FFH	1, 8	√	√	√	—	—	√	√	—	—
FFF26H	Port mode register 6	PM6	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFF27H	Port mode register 7	PM7	FFH	1, 8	√	√	√	√	—	√	√	√	—
FFF28H	Port mode register 8	PM8	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFF29H	Port mode register 9	PM9	FFH	1, 8	√	√	√	√	—	√	√	√	—
FFF2AH	Port mode register 10	PM10	FFH	1, 8	√	—	—	—	—	—	—	—	—
FFF2CH	Port mode register 12	PM12	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFF2EH	Port mode register 14	PM14	FFH	1, 8	√	√	√	√	—	√	√	√	—
FFF2FH	Port mode register 15	PM15	FFH	1, 8	√	—	—	—	—	—	—	—	—
FFF30H	A/D converter access window register	ADWINR	00H	8	√	√	√	√	√	√	√	√	√
FFF32H	Application accelerator unit access window register	AAUWINR	00H	8	√	√	√	√	√	√	√	√	√
FFF34H	D/A conversion value setting register 0	DACS0	00H	8	√	√	√	√	√	—	—	—	—
FFF36H	D/A converter mode register	DAM	00H	1, 8	√	√	√	√	√	—	—	—	—
FFF37H	Key return mode register	KRM	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF38H	External interrupt rising edge enable register 0	EGP0	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF39H	External interrupt falling edge enable register 0	EGN0	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF3AH	External interrupt rising edge enable register 1	EGP1	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF3BH	External interrupt falling edge enable register 1	EGN1	00H	1, 8	√	√	√	√	√	√	√	√	√

“UND” Undefined value

Table 1-1. List of Special Function Registers (SFR) for RL78/F23, F24 (2/4)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
FFF48H	Serial data register 10	SDR10	0000H	16	√	√	√	√	√	√	√	√	√
		SDR10L		8									
FFF49H		—		—									
FFF4AH	Serial data register 11	SDR11	0000H	16	√	√	√	√	√	√	√	√	√
		SDR11L		8									
FFF4BH		—		—									
FFF50H	IICA shift register 0	IICA0	00H	8	√	√	√	√	√	√	√	√	√
FFF51H	IICA status register 0	IICS0	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF52H	IICA flag register 0	IICF0	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF54H FFF55H	16-bit watch error correction register	SUBCUDW	0000H	16	√	√	√	√	√	√	√	√	√
FFF58H FFF59H	Timer RDe general register C0	TRDGRC0	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF5AH FFF5BH	Timer RDe general register D0	TRDGRD0	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF5CH FFF5DH	Timer RDe general register C1	TRDGRC1	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF5EH FFF5FH	Timer RDe general register D1	TRDGRD1	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF60H FFF61H	Timer RDe extended compare register D0	TRDCMPD0	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF62H FFF63H	Timer RDe extended compare register C1	TRDCMPC1	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF64H FFF65H	Timer RDe extended compare register D1	TRDCMPD1	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF66H FFF67H	Timer RDe A/D trigger buffer register 0	TRDADTB0	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF68H FFF69H	Timer RDe A/D trigger buffer register 1	TRDADTB1	FFFFH	16	√	√	√	√	√	√	√	√	√
FFF6AH	Timer RDe reload trigger register	TRDRDT01	0000H	16	√	√	√	√	√	√	√	√	√
	Timer RDe reload trigger register 0	TRDRDT0		1, 8									
FFF6BH	Timer RDe reload trigger register 1	TRDRDT1		1, 8									
FFF6CH	Timer RDe dithering/gate control register 0	TRDDGCR0	0000H	16	√	√	√	√	√	√	√	√	√
	Timer RDe dithering number register 0	TRDDNR0		1, 8									
FFF6DH	Timer RDe gate pattern register 0	TRDGPR0		1, 8									
FFF6EH	Timer RDe dithering/gate control register 1	TRDDGCR1	0000H	16	√	√	√	√	√	√	√	√	√
	Timer RDe dithering number register 1	TRDDNR1		1, 8									
FFF6FH	Timer RDe gate pattern register 1	TRDGPR1		1, 8									
FFF74H FFF75H	Timer data register 02	TDR02	0000H	16	√	√	√	√	√	√	√	√	√
FFF76H	Timer data register 03	TDR03	0000H	16	√	√	√	√	√	√	√	√	√
		TDR03L		8									
FFF77H		TDR03H		8									
FFF78H FFF79H	Timer data register 04	TDR04	0000H	16	√	√	√	√	√	√	√	√	√
FFF7AH FFF7BH	Timer data register 05	TDR05	0000H	16	√	√	√	√	√	√	√	√	√
FFF7CH FFF7DH	Timer data register 06	TDR06	0000H	16	√	√	√	√	√	√	√	√	√
FFF7EH FFF7FH	Timer data register 07	TDR07	0000H	16	√	√	√	√	√	√	√	√	√
FFF80H FFF81H	Timer data register 10	TDR10	0000H	16	√	√	√	√	√	√	√	√	√
FFF82H	Timer data register 11	TDR11	0000H	16	√	√	√	√	√	√	√	√	√
		TDR11L		8									
FFF83H		TDR11H		8									
FFF84H FFF85H	Timer data register 12	TDR12	0000H	16	√	√	√	√	√	√	√	√	√

Table 1-1. List of Special Function Registers (SFR) for RL78/F23, F24 (3/4)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
FFF86H	Timer data register 13	TDR13	0000H	16	√	√	√	√	√	√	√	√	√
		TDR13L		8									
FFF87H		TDR13H		8									
FFF88H FFF89H	Timer data register 14	TDR14	0000H	16	√	√	√	√	√	—	—	—	—
FFF8AH FFF8BH	Timer data register 15	TDR15	0000H	16	√	√	√	√	√	—	—	—	—
FFF8CH FFF8DH	Timer data register 16	TDR16	0000H	16	√	√	√	√	√	—	—	—	—
FFF8EH FFF8FH	Timer data register 17	TDR17	0000H	16	√	√	√	√	√	—	—	—	—
FFF92H	SEC count register	SEC	00H	8	√	√	√	√	√	√	√	√	√
FFF93H	MIN count register	MIN	00H	8	√	√	√	√	√	√	√	√	√
FFF94H	HOUR count register	HOUR	12H Note 1	8	√	√	√	√	√	√	√	√	√
FFF95H	WEEK count register	WEEK	00H	8	√	√	√	√	√	√	√	√	√
FFF96H	DAY count register	DAY	01H	8	√	√	√	√	√	√	√	√	√
FFF97H	MONTH count register	MONTH	01H	8	√	√	√	√	√	√	√	√	√
FFF98H	YEAR count register	YEAR	00H	8	√	√	√	√	√	√	√	√	√
FFF99H	Watch error correction register	SUBCUD	00H	8	√	√	√	√	√	√	√	√	√
FFF9AH	Alarm MIN register	ALARMWM	00H	8	√	√	√	√	√	√	√	√	√
FFF9BH	Alarm HOUR register	ALARMWH	12H	8	√	√	√	√	√	√	√	√	√
FFF9CH	Alarm WEEK register	ALARMWW	00H	8	√	√	√	√	√	√	√	√	√
FFF9DH	Real-time clock control register 0	RTCC0	00H	1, 8	√	√	√	√	√	√	√	√	√
FFF9EH	Real-time clock control register 1	RTCC1	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFA0H	Clock operation mode control register	CMC	00H	8	√	√	√	√	√	√	√	√	√
FFFA1H	Clock operation status control register	CSC	C0H	1, 8	√	√	√	√	√	√	√	√	√
FFFA2H	Oscillation stabilization time counter status register	OSTC	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFA3H	Oscillation stabilization time select register	OSTS	07H	8	√	√	√	√	√	√	√	√	√
FFFA4H	System clock control register	CKC	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFA5H	Clock output select register 0	CKS0	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFA8H	Reset control flag register	RESF	(Note 2)	8	√	√	√	√	√	√	√	√	√
FFFA9H	Voltage detection register	LVIM	(Note 3)	1, 8	√	√	√	√	√	√	√	√	√
FFFAAH	Voltage detection level register	LVIS	(Note 4)	1, 8	√	√	√	√	√	√	√	√	√
FFFABH	Watchdog timer enable register	WDTE	(Note 5)	8	√	√	√	√	√	√	√	√	√
FFFACH	CRC input register	CRCIN	00H	8	√	√	√	√	√	√	√	√	√
FFFB0H FFFB1H	Flash security flag monitoring register	FLSEC	(Note 6)	16	√	√	√	√	√	√	√	√	√
FFFB2H FFFB3H	Flash FSW monitoring register S	FLFSWS	(Note 7)	16	√	√	√	√	√	√	√	√	√
FFFB4H FFFB5H	Flash FSW monitoring register E	FLFSWE	(Note 7)	16	√	√	√	√	√	√	√	√	√
FFFB6H	Flash memory sequencer initial setting register	FSSET	00H	8	√	√	√	√	√	√	√	√	√
FFFB7H	Extra area sequencer control register	FSSE	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFC0H	Flash protect command register	PFCMD	UND	8	√	√	√	√	√	√	√	√	√
FFFC1H	Flash status register	PFS	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFC6H	Flash ECC write buffer register	FLWE	00H	8	√	√	√	√	√	√	√	√	√

"UND" Undefined value

Notes 1. The value of the HOUR register is 00H if the AMPM bit of the RTCC0 register is set to 1 after reset.
2. The value after reset varies depending on the reset source.
3. The reset value changes depending on the reset source.
4. The reset value changes depending on the reset source and the setting of the user option byte (000C1H/040C1H).
5. The value of the WDTE register is 1AH or 9AH. The value changes depending on the user option byte (000C0H/040C0H).
6. The reset value changes depending on the security flag setting.
7. The reset value changes depending on the flash shield window setting.

Table 1-1. List of Special Function Registers (SFR) for RL78/F23, F24 (4/4)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
FFFD0H	Interrupt request flag register 2L	IF2L	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFD1H	Interrupt request flag register 2H	IF2H	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFD2H	Interrupt request flag register 3L	IF3L	00H	1, 8	√	√	√	√	√	√	√	—	—
FFFD3H	Interrupt request flag register 3H	IF3H	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFD4H	Interrupt mask flag register 2L	MK2L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFD5H	Interrupt mask flag register 2H	MK2H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFD6H	Interrupt mask flag register 3L	MK3L	FFH	1, 8	√	√	√	√	√	√	√	—	—
FFFD7H	Interrupt mask flag register 3H	MK3H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFD8H	Interrupt priority specification flag 0 register 2L	PR02L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFD9H	Interrupt priority specification flag 0 register 2H	PR02H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFDAH	Interrupt priority specification flag 0 register 3L	PR03L	FFH	1, 8	√	√	√	√	√	√	√	—	—
FFFDBH	Interrupt priority specification flag 0 register 3H	PR03H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFDCH	Interrupt priority specification flag 1 register 2L	PR12L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFDDH	Interrupt priority specification flag 1 register 2H	PR12H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFDEH	Interrupt priority specification flag 1 register 3L	PR13L	FFH	1, 8	√	√	√	√	√	√	√	—	—
FFFDFH	Interrupt priority specification flag 1 register 3H	PR13H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFE0H	Interrupt request flag register 0L	IF0L	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFE1H	Interrupt request flag register 0H	IF0H	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFE2H	Interrupt request flag register 1L	IF1L	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFE3H	Interrupt request flag register 1H	IF1H	00H	1, 8	√	√	√	√	√	√	√	√	√
FFFE4H	Interrupt mask flag register 0L	MK0L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFE5H	Interrupt mask flag register 0H	MK0H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFE6H	Interrupt mask flag register 1L	MK1L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFE7H	Interrupt mask flag register 1H	MK1H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFE8H	Interrupt priority specification flag 0 register 0L	PR00L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFE9H	Interrupt priority specification flag 0 register 0H	PR00H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFEAH	Interrupt priority specification flag 0 register 1L	PR01L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFEBH	Interrupt priority specification flag 0 register 1H	PR01H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFECH	Interrupt priority specification flag 1 register 0L	PR10L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFEDH	Interrupt priority specification flag 1 register 0H	PR10H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFEEH	Interrupt priority specification flag 1 register 1L	PR11L	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFEFH	Interrupt priority specification flag 1 register 1H	PR11H	FFH	1, 8	√	√	√	√	√	√	√	√	√
FFFF0H FFFF1H	Multiply and accumulation register (L)	MACRL	0000H	16	√	√	√	√	√	√	√	√	√
FFFF2H FFFF3H	Multiply and accumulation register (H)	MACRH	0000H	16	√	√	√	√	√	√	√	√	√
FFFFEH	Processor mode control register	PMC	00H	1, 8	√	√	√	√	√	√	√	√	√

2. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24

The table below lists the extended special function registers (2nd SFR) for RL78/F23, F24 products.

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (1/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0016H	Peripheral I/O redirection register 0	PIOR0	00H	8	√	√	√	√	—	√	√	√	—
F0017H	Peripheral I/O redirection register 1	PIOR1	00H	8	√	√	√	√	√	√	√	√	√
F0018H	Peripheral I/O redirection register 2	PIOR2	00H	8	√	√	—	—	—	√	—	—	—
F0019H	Peripheral I/O redirection register 3	PIOR3	00H	8	√	√	—	—	—	√	—	—	—
F001AH	Peripheral I/O redirection register 4	PIOR4	00H	8	√	√	√	√	√	√	√	√	√
F001BH	Peripheral I/O redirection register 5	PIOR5	00H	8	√	√	√	√	√	√	√	√	√
F001CH	Peripheral I/O redirection register 6	PIOR6	00H	8	√	√	—	—	—	√	—	—	—
F001DH	Peripheral I/O redirection register 7	PIOR7	00H	8	√	√	√	√	√	√	√	√	√
F001EH	Peripheral I/O redirection register 8	PIOR8	00H	8	√	—	—	—	—	—	—	—	—
F001FH	Peripheral I/O redirection register 9	PIOR9	00H	8	√	√	√	√	√	√	√	√	√
F0021H	Port input threshold control register 1	PITHL1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0023H	Port input threshold control register 3	PITHL3	00H	1, 8	√	√	√	√	√	√	√	√	√
F0024H	Port input threshold control register 4	PITHL4	00H	1, 8	√	√	√	√	√	√	√	√	√
F0025H	Port input threshold control register 5	PITHL5	00H	1, 8	√	√	√	—	—	√	√	—	—
F0026H	Port input threshold control register 6	PITHL6	00H	1, 8	√	√	√	√	√	√	√	√	√
F0027H	Port input threshold control register 7	PITHL7	00H	1, 8	√	√	√	√	—	√	√	√	—
F002AH	Port input threshold control register 10	PITHL10	00H	1, 8	√	—	—	—	—	—	—	—	—
F002CH	Port input threshold control register 12	PITHL12	00H	1, 8	√	√	√	√	√	√	√	√	√
F002FH	Port input threshold control register 15	PITHL15	00H	1, 8	√	—	—	—	—	—	—	—	—
F0030H	Pull-up resistor option register 0	PU0	00H	1, 8	√	√	√	√	—	√	√	√	—
F0031H	Pull-up resistor option register 1	PU1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0033H	Pull-up resistor option register 3	PU3	00H	1, 8	√	√	√	√	√	√	√	√	√
F0034H	Pull-up resistor option register 4	PU4	01H	1, 8	√	√	√	√	√	√	√	√	√
F0035H	Pull-up resistor option register 5	PU5	00H	1, 8	√	√	√	—	—	√	√	—	—
F0036H	Pull-up resistor option register 6	PU6	00H	1, 8	√	√	√	√	√	√	√	√	√
F0037H	Pull-up resistor option register 7	PU7	00H	1, 8	√	√	√	√	—	√	√	√	—
F003AH	Pull-up resistor option register 10	PU10	00H	1, 8	√	—	—	—	—	—	—	—	—
F003CH	Pull-up resistor option register 12	PU12	00H	1, 8	√	√	√	√	√	√	√	√	√
F003EH	Pull-up resistor option register 14	PU14	00H	1, 8	√	√	√	√	—	√	√	√	—
F003FH	Pull-up resistor option register 15	PU15	00H	1, 8	√	—	—	—	—	—	—	—	—
F0041H	Port input mode register 1	PIM1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0043H	Port input mode register 3	PIM3	00H	1, 8	√	√	√	√	√	√	√	√	√
F0045H	Port input mode register 5	PIM5	00H	1, 8	√	√	—	—	—	√	—	—	—
F0046H	Port input mode register 6	PIM6	00H	1, 8	√	√	√	√	√	√	√	√	√
F0047H	Port input mode register 7	PIM7	00H	1, 8	√	√	√	√	—	√	√	√	—
F004CH	Port input mode register 12	PIM12	00H	1, 8	√	√	√	√	√	√	√	√	√
F0051H	Port output mode register 1	POM1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0053H	Port output mode register 3	POM3	00H	1, 8	√	√	√	√	—	√	√	√	—
F0056H	Port output mode register 6	POM6	00H	1, 8	√	√	√	√	√	√	√	√	√
F0057H	Port output mode register 7	POM7	00H	1, 8	√	√	√	√	—	√	√	√	—
F005CH	Port output mode register 12	POM12	00H	1, 8	√	√	√	√	√	√	√	√	√
F0063H	Port mode control register 3	PMC3	FFH	1, 8	√	√	√	√	√	√	√	√	√
F0067H	Port mode control register 7	PMC7	FFH	1, 8	√	√	√	√	—	√	√	√	—
F0068H	Port mode control register 8	PMC8	FFH	1, 8	√	√	√	√	√	√	√	√	√
F0069H	Port mode control register 9	PMC9	FFH	1, 8	√	√	√	√	—	√	√	√	—
F006AH	Port mode control register 10	PMC10	FFH	1, 8	√	—	—	—	—	—	—	—	—
F006CH	Port mode control register 12	PMC12	FFH	1, 8	√	√	√	√	√	√	√	√	√

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (2/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0070H	Noise filter enable register 0	NFEN0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0071H	Noise filter enable register 1	NFEN1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0072H	Noise filter enable register 2	NFEN2	00H	1, 8	√	√	√	√	√	√	√	√	√
F0073H	Input switch control register	ISC	00H	1, 8	√	√	√	√	√	√	√	√	√
F0074H	Timer input select register 0	TIS0	00H	8	√	√	√	√	√	√	√	√	√
F0075H	Timer input select register 1	TIS1	00H	8	√	√	√	√	√	√	√	√	√
F0076H	RAM start address setting register	RAMSAR	EFH	8	√	√	√	√	√	√	√	√	√
F0077H	Port mode select register	PMS	00H	1, 8	√	√	√	√	√	√	√	√	√
F0078H	Invalid memory access detection control register	IAWCTL	00H	8	√	√	√	√	√	√	√	√	√
F0079H	Interrupt source determination flag register 0	INTFLG0	00H	8	√	√	√	√	√	√	√	√	√
F007AH	Timer input select register 2	TIS2	00H	8	√	√	√	√	√	√	√	√	√
F007BH	LIN channel select register	LCHSEL	00H	8	√	√	√	√	√	√	√	√	√
F007CH	Interrupt mask register	INTMSK	FFH	8	√	√	√	√	√	√	√	√	√
F0090H	Data flash control register	DFLCTL	00H	1, 8	√	√	√	√	√	√	√	√	√
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM	UND	8	√	√	√	√	√	√	√	√	√
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV	(Note 1)	8	√	√	√	√	√	√	√	√	√
F00B8H	Code flash bit error detection function control register	CFERRCTLR	00H	8	√	√	√	√	√	√	√	√	√
F00B9H	Code flash bit error detection function status register	CFERRSTR	00H	8	√	√	√	√	√	√	√	√	√
F00BAH F00BBH	Code flash bit error detection address register L / Code flash bit error detection address register n L [n = 1 to 3]	ERRADRL / ERRADRnL	FFFCH	16	√	√	√	√	√	√	√	√	√
F00BCH F00BDH	Code flash bit error detection address register H / Code flash bit error detection address register n H [n = 1 to 3]	ERRADRH / ERRADRnH	3F0FH	16	√	√	√	√	√	√	√	√	√
F00C0H	Flash programming mode control register	FLPMC	08H	8	√	√	√	√	√	√	√	√	√
F00C1H	Flash area selection register	FLARS	00H	1, 8	√	√	√	√	√	√	√	√	√
F00C2H F00C3H	Flash address pointer register L	FLAPL	0000H	16	√	√	√	√	√	√	√	√	√
F00C4H	Flash address pointer register H	FLAPH	00H	8	√	√	√	√	√	√	√	√	√
F00C5H	Flash memory sequencer control register	FSSQ	00H	1, 8	√	√	√	√	√	√	√	√	√
F00C6H F00C7H	Flash end address pointer register L	FLSEDL	0000H	16	√	√	√	√	√	√	√	√	√
F00C8H	Flash end address pointer register H	FLSEDH	00H	8	√	√	√	√	√	√	√	√	√
F00C9H	Flash registers initialization register	FLRST	00H	1, 8	√	√	√	√	√	√	√	√	√
F00CAH	Flash memory sequencer status register L	FSASTL	(Note 2)	1, 8	√	√	√	√	√	√	√	√	√
F00CBH	Flash memory sequencer status register H	FSASTH	00H	1, 8	√	√	√	√	√	√	√	√	√
F00CCH F00CDH	Flash write buffer register L	FLWL	0000H	16	√	√	√	√	√	√	√	√	√
F00CEH F00CFH	Flash write buffer register H	FLWH	0000H	16	√	√	√	√	√	√	√	√	√
F00D8H	SPM control register	SPMCTRL	00H	8	√	√	√	√	√	√	√	√	√
F00DAH F00DBH	SP overflow address setting register	SPOFR	FFFEH	16	√	√	√	√	√	√	√	√	√
F00DCH F00DDH	SP underflow address setting register	SPUFR	0000H	16	√	√	√	√	√	√	√	√	√
F00E0H	A/D conversion clock control register	ADCKS	00H	8	√	√	√	√	√	√	√	√	√
F00F0H	Peripheral enable register 0	PER0	00H	1, 8	√	√	√	√	√	√	√	√	√
F00F3H	Operation speed mode control register	OSMC	00H	8	√	√	√	√	√	√	√	√	√

"UND" Undefined value

Notes 1. The value set with the FRQSEL2 to FRQSEL0 bits of the user option byte (000C2H/040C2H).

2. The value of the MBTSEL bit depends on the value of the BTFLG bit stored in the extra area.

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (3/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F00FEH	BCD correction result register	BCDADJ	UND	8	√	√	√	√	√	√	√	√	√
F0100H	Serial status register 00	SSR00	0000H	16	√	√	√	√	√	√	√	√	√
		SSR00L		8									
F0101H		—		—									
F0102H	Serial status register 01	SSR01	0000H	16	√	√	√	√	√	√	√	√	√
		SSR01L		8									
F0103H		—		—									
F0104H	Serial flag clear trigger register 00	SIR00	0000H	16	√	√	√	√	√	√	√	√	√
		SIR00L		8									
F0105H		—		—									
F0106H	Serial flag clear trigger register 01	SIR01	0000H	16	√	√	√	√	√	√	√	√	√
		SIR01L		8									
F0107H		—		—									
F0108H F0109H	Serial mode register 00	SMR00	0020H	16	√	√	√	√	√	√	√	√	√
F010AH F010BH	Serial mode register 01	SMR01	0020H	16	√	√	√	√	√	√	√	√	√
F010CH F010DH	Serial communication operation setting register 00	SCR00	0087H	16	√	√	√	√	√	√	√	√	√
F010EH F010FH	Serial communication operation setting register 01	SCR01	0087H	16	√	√	√	√	√	√	√	√	√
F0110H	Serial channel enable status register 0	SE0	0000H	16	√	√	√	√	√	√	√	√	√
		SE0L		1, 8									
F0111H		—		—									
F0112H	Serial channel start register 0	SS0	0000H	16	√	√	√	√	√	√	√	√	√
		SS0L		1, 8									
F0113H		—		—									
F0114H	Serial channel stop register 0	ST0	0000H	16	√	√	√	√	√	√	√	√	√
		ST0L		1, 8									
F0115H		—		—									
F0116H	Serial clock select register 0	SPS0	0000H	16	√	√	√	√	√	√	√	√	√
		SPS0L		8									
F0117H		—		—									
F0118H F0119H	Serial output register 0	SO0	0303H	16	√	√	√	√	√	√	√	√	√
F011AH	Serial output enable register 0	SOE0	0000H	16	√	√	√	√	√	√	√	√	√
		SOE0L		1, 8									
F011BH		—		—									
F0120H	Serial output level register 0	SOL0	0000H	16	√	√	√	√	√	√	√	√	√
		SOL0L		8									
F0121H		—		—									
F0122H	Serial slave select enable register 0	SSE0	0000H	16	√	√	√	√	√	√	√	√	√
		SSE0L		8									
F0123H		—		—									
F0140H	Serial status register 10	SSR10	0000H	16	√	√	√	√	√	√	√	√	√
		SSR10L		8									
F0141H		—		—									
F0142H	Serial status register 11	SSR11	0000H	16	√	√	√	√	√	√	√	√	√
		SSR11L		8									
F0143H		—		—									
F0144H	Serial flag clear trigger register 10	SIR10	0000H	16	√	√	√	√	√	√	√	√	√
		SIR10L		8									
F0145H		—		—									

“UND” Undefined value

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (4/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0146H	Serial flag clear trigger register 11	SIR11	0000H	16	√	√	√	√	√	√	√	√	√
		SIR11L		8									
F0147H		—		—									
F0148H F0149H	Serial mode register 10	SMR10	0020H	16	√	√	√	√	√	√	√	√	√
F014AH F014BH	Serial mode register 11	SMR11	0020H	16	√	√	√	√	√	√	√	√	√
F014CH F014DH	Serial communication operation setting register 10	SCR10	0087H	16	√	√	√	√	√	√	√	√	√
F014EH F014FH	Serial communication operation setting register 11	SCR11	0087H	16	√	√	√	√	√	√	√	√	√
F0150H	Serial channel enable status register 1	SE1	0000H	16	√	√	√	√	√	√	√	√	√
		SE1L		1, 8									
F0151H		—		—									
F0152H	Serial channel start register 1	SS1	0000H	16	√	√	√	√	√	√	√	√	√
		SS1L		1, 8									
F0153H		—		—									
F0154H	Serial channel stop register 1	ST1	0000H	16	√	√	√	√	√	√	√	√	√
		ST1L		1, 8									
F0155H		—		—									
F0156H	Serial clock select register 1	SPS1	0000H	16	√	√	√	√	√	√	√	√	√
		SPS1L		8									
F0157H		—		—									
F0158H F0159H	Serial output register 1	SO1	0303H	16	√	√	√	√	√	√	√	√	√
F015AH	Serial output enable register 1	SOE1	0000H	16	√	√	√	√	√	√	√	√	√
		SOE1L		1, 8									
F015BH		—		—									
F0160H	Serial output level register 1	SOL1	0000H	16	√	√	√	√	√	√	√	√	√
		SOL1L		8									
F0161H		—		—									
F0162H	Serial slave select enable register 1	SSE1	0000H	16	√	√	√	√	√	√	√	√	√
		SSE1L		8									
F0163H		—		—									
F0180H F0181H	Timer count register 00	TCR00	FFFFH	16	√	√	√	√	√	√	√	√	√
F0182H F0183H	Timer count register 01	TCR01	FFFFH	16	√	√	√	√	√	√	√	√	√
F0184H F0185H	Timer count register 02	TCR02	FFFFH	16	√	√	√	√	√	√	√	√	√
F0186H F0187H	Timer count register 03	TCR03	FFFFH	16	√	√	√	√	√	√	√	√	√
F0188H F0189H	Timer count register 04	TCR04	FFFFH	16	√	√	√	√	√	√	√	√	√
F018AH F018BH	Timer count register 05	TCR05	FFFFH	16	√	√	√	√	√	√	√	√	√
F018CH F018DH	Timer count register 06	TCR06	FFFFH	16	√	√	√	√	√	√	√	√	√
F018EH F018FH	Timer count register 07	TCR07	FFFFH	16	√	√	√	√	√	√	√	√	√
F0190H F0191H	Timer mode register 00	TMR00	0000H	16	√	√	√	√	√	√	√	√	√
F0192H F0193H	Timer mode register 01	TMR01	0000H	16	√	√	√	√	√	√	√	√	√
F0194H F0195H	Timer mode register 02	TMR02	0000H	16	√	√	√	√	√	√	√	√	√
F0196H F0197H	Timer mode register 03	TMR03	0000H	16	√	√	√	√	√	√	√	√	√

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (5/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0198H F0199H	Timer mode register 04	TMR04	0000H	16	√	√	√	√	√	√	√	√	√
F019AH F019BH	Timer mode register 05	TMR05	0000H	16	√	√	√	√	√	√	√	√	√
F019CH F019DH	Timer mode register 06	TMR06	0000H	16	√	√	√	√	√	√	√	√	√
F019EH F019FH	Timer mode register 07	TMR07	0000H	16	√	√	√	√	√	√	√	√	√
F01A0H	Timer status register 00	TSR00	0000H	16	√	√	√	√	√	√	√	√	√
		TSR00L		8									
F01A1H		—		—									
F01A2H	Timer status register 01	TSR01	0000H	16	√	√	√	√	√	√	√	√	√
		TSR01L		8									
F01A3H		—		—									
F01A4H	Timer status register 02	TSR02	0000H	16	√	√	√	√	√	√	√	√	√
		TSR02L		8									
F01A5H		—		—									
F01A6H	Timer status register 03	TSR03	0000H	16	√	√	√	√	√	√	√	√	√
		TSR03L		8									
F01A7H		—		—									
F01A8H	Timer status register 04	TSR04	0000H	16	√	√	√	√	√	√	√	√	√
		TSR04L		8									
F01A9H		—		—									
F01AAH	Timer status register 05	TSR05	0000H	16	√	√	√	√	√	√	√	√	√
		TSR05L		8									
F01ABH		—		—									
F01ACH	Timer status register 06	TSR06	0000H	16	√	√	√	√	√	√	√	√	√
		TSR06L		8									
F01ADH		—		—									
F01AEH	Timer status register 07	TSR07	0000H	16	√	√	√	√	√	√	√	√	√
		TSR07L		8									
F01AFH		—		—									
F01B0H	Timer channel enable status register 0	TE0	0000H	16	√	√	√	√	√	√	√	√	√
		TE0L		1, 8									
F01B1H		—		—									
F01B2H	Timer channel start register 0	TS0	0000H	16	√	√	√	√	√	√	√	√	√
		TS0L		1, 8									
F01B3H		—		—									
F01B4H	Timer channel stop register 0	TT0	0000H	16	√	√	√	√	√	√	√	√	√
		TT0L		1, 8									
F01B5H		—		—									
F01B6H F01B7H	Timer clock select register 0	TPS0	0000H	16	√	√	√	√	√	√	√	√	√
F01B8H	Timer output register 0	TO0	0000H	16	√	√	√	√	√	√	√	√	√
		TO0L		8									
F01B9H		—		—									
F01BAH	Timer output enable register 0	TOE0	0000H	16	√	√	√	√	√	√	√	√	√
		TOE0L		1, 8									
F01BBH		—		—									
F01BCH	Timer output level register 0	TOL0	0000H	16	√	√	√	√	√	√	√	√	√
		TOL0L		8									
F01BDH		—		—									
F01BEH	Timer output mode register 0	TOM0	0000H	16	√	√	√	√	√	√	√	√	√
		TOM0L		8									
F01BFH		—		—									

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (6/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F01C0H F01C1H	Timer count register 10	TCR10	FFFFH	16	√	√	√	√	√	√	√	√	√
F01C2H F01C3H	Timer count register 11	TCR11	FFFFH	16	√	√	√	√	√	√	√	√	√
F01C4H F01C5H	Timer count register 12	TCR12	FFFFH	16	√	√	√	√	√	√	√	√	√
F01C6H F01C7H	Timer count register 13	TCR13	FFFFH	16	√	√	√	√	√	√	√	√	√
F01C8H F01C9H	Timer count register 14	TCR14	FFFFH	16	√	√	√	√	√	—	—	—	—
F01CAH F01CBH	Timer count register 15	TCR15	FFFFH	16	√	√	√	√	√	—	—	—	—
F01CCH F01CDH	Timer count register 16	TCR16	FFFFH	16	√	√	√	√	√	—	—	—	—
F01CEH F01CFH	Timer count register 17	TCR17	FFFFH	16	√	√	√	√	√	—	—	—	—
F01D0H F01D1H	Timer mode register 10	TMR10	0000H	16	√	√	√	√	√	√	√	√	√
F01D2H F01D3H	Timer mode register 11	TMR11	0000H	16	√	√	√	√	√	√	√	√	√
F01D4H F01D5H	Timer mode register 12	TMR12	0000H	16	√	√	√	√	√	√	√	√	√
F01D6H F01D7H	Timer mode register 13	TMR13	0000H	16	√	√	√	√	√	√	√	√	√
F01D8H F01D9H	Timer mode register 14	TMR14	0000H	16	√	√	√	√	√	—	—	—	—
F01DAH F01DBH	Timer mode register 15	TMR15	0000H	16	√	√	√	√	√	—	—	—	—
F01DCH F01DDH	Timer mode register 16	TMR16	0000H	16	√	√	√	√	√	—	—	—	—
F01DEH F01DFH	Timer mode register 17	TMR17	0000H	16	√	√	√	√	√	—	—	—	—
F01E0H	Timer status register 10	TSR10	0000H	16	√	√	√	√	√	√	√	√	√
		TSR10L		8									
F01E1H		—		—									
F01E2H	Timer status register 11	TSR11	0000H	16	√	√	√	√	√	√	√	√	√
		TSR11L		8									
F01E3H		—		—									
F01E4H	Timer status register 12	TSR12	0000H	16	√	√	√	√	√	√	√	√	√
		TSR12L		8									
F01E5H		—		—									
F01E6H	Timer status register 13	TSR13	0000H	16	√	√	√	√	√	√	√	√	√
		TSR13L		8									
F01E7H		—											
F01E8H	Timer status register 14	TSR14	0000H	16	√	√	√	√	√	—	—	—	—
		TSR14L		8									
F01E9H		—		—									
F01EAH	Timer status register 15	TSR15	0000H	16	√	√	√	√	√	—	—	—	—
		TSR15L		8									
F01EBH		—		—									
F01ECH	Timer status register 16	TSR16	0000H	16	√	√	√	√	√	—	—	—	—
		TSR16L		8									
F01EDH		—		—									
F01EEH	Timer status register 17	TSR17	0000H	16	√	√	√	√	√	—	—	—	—
		TSR17L		8									
F01EFH		—		—									
F01F0H	Timer channel enable status register 1	TE1	0000H	16	√	√	√	√	√	√	√	√	√
		TE1L		1, 8									
F01F1H		—		—									

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (7/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F01F2H	Timer channel start register 1	TS1	0000H	16	√	√	√	√	√	√	√	√	√
		TS1L		1, 8									
F01F3H		—		—									
F01F4H	Timer channel stop register 1	TT1	0000H	16	√	√	√	√	√	√	√	√	√
		TT1L		1, 8									
F01F5H		—		—									
F01F6H F01F7H	Timer clock select register 1	TPS1	0000H	16	√	√	√	√	√	√	√	√	√
F01F8H	Timer output register 1	TO1	0000H	16	√	√	√	√	√	√	√	√	√
		TO1L		8									
F01F9H		—		—									
F01FAH	Timer output enable register 1	TOE1	0000H	16	√	√	√	√	√	√	√	√	√
		TOE1L		1, 8									
F01FBH		—		—									
F01FCH	Timer output level register 1	TOL1	0000H	16	√	√	√	√	√	√	√	√	√
		TOL1L		8									
F01FDH		—		—									
F01FEH	Timer output mode register 1	TOM1	0000H	16	√	√	√	√	√	√	√	√	√
		TOM1L		8									
F01FFH		—		—									
F0200H F0201H	Error address store register	ERADR	0000H	16	√	√	√	√	√	√	√	√	√
F0202H	1-bit error detection interrupt enable register	ECCIER	00H	8	√	√	√	√	√	√	√	√	√
F0203H	Bit error detection register	ECCER	00H	8	√	√	√	√	√	√	√	√	√
F0204H	ECC test protect register	ECCTPR	00H	8	√	√	√	√	√	√	√	√	√
F0205H	ECC test mode register	ECCTMDR	00H	8	√	√	√	√	√	√	√	√	√
F0206H F0207H	Write data inversion register	ECCDWRVR	0000H	16	√	√	√	√	√	√	√	√	√
F0220H	Port output slew rate register	PSRSEL	00H	1, 8	√	√	√	√	√	√	√	√	√
F0222H	SNOOZE status output control register 0	PSNZCNT0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0223H	SNOOZE status output control register 1	PSNZCNT1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0224H	SNOOZE status output control register 2	PSNZCNT2	00H	1, 8	√	√	√	√	—	√	√	√	—
F0225H	SNOOZE status output control register 3	PSNZCNT3	00H	1, 8	√	√	√	√	—	√	√	√	—
F0227H	D/A converter mode register 2	DAM2	00H	1, 8	√	√	√	√	√	—	—	—	—
F0228H F0229H	PWM output delay control register 0	PWMDLY0	0000H	16	√	√	√	√	√	√	√	√	√
F022AH F022BH	PWM output delay control register 1	PWMDLY1	0000H	16	√	√	√	√	√	√	√	√	√
F022CH F022DH	PWM output delay control register 2	PWMDLY2	0000H	16	√	√	√	√	√	√	√	√	√
F0230H	IICA control register 00	IICCTL00	00H	1, 8	√	√	√	√	√	√	√	√	√
F0231H	IICA control register 01	IICCTL01	00H	1, 8	√	√	√	√	√	√	√	√	√
F0232H	IICA low-level width setting register 0	IICWL0	FFH	8	√	√	√	√	√	√	√	√	√
F0233H	IICA high-level width setting register 0	IICWH0	FFH	8	√	√	√	√	√	√	√	√	√
F0234H	Slave address register 0	SVA0	00H	8	√	√	√	√	√	√	√	√	√
F0240H	Timer RJ control register 0	TRJCR0	00H	8	√	√	√	√	√	√	√	√	√
F0241H	Timer RJ I/O control register 0	TRJIOC0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0242H	Timer RJ mode register 0	TRJMR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0243H	Timer RJ event pin select register 0	TRJISR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0248H	PWMOPA control register 0	OPCTL0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0249H	PWMOPA cutoff control register 0	OPDF0	00H	8	√	√	√	√	√	√	√	√	√
F024AH	PWMOPA cutoff control register 1	OPDF1	00H	8	√	√	√	√	√	√	√	√	√
F024BH	PWMOPA edge selection register	OPEDGE	00H	8	√	√	√	√	√	√	√	√	√

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (8/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F024CH	PWMOPA status register	OPSR	00H	1, 8	√	√	√	√	√	√	√	√	√
F024EH	Timer RDe decimation control register	TRDMBKCTL	00H	8	√	√	√	√	√	√	√	√	√
F024FH	Timer RDe decimation count register	TRDMBKCMP	00H	8	√	√	√	√	√	√	√	√	√
F0250H	Timer RDe ELC register	TRDELC	00H	1, 8	√	√	√	√	√	√	√	√	√
F0253H	Timer RDe start register	TRDSTR	0CH	8	√	√	√	√	√	√	√	√	√
F0254H	Timer RDe mode register	TRDMR	00H	1, 8	√	√	√	√	√	√	√	√	√
F0255H	Timer RDe PWM function select register	TRDPMR	00H	1, 8	√	√	√	√	√	√	√	√	√
F0256H	Timer RDe function control register	TRDFCR	80H	1, 8	√	√	√	√	√	√	√	√	√
F0257H	Timer RDe output master enable register 1	TRDOER1	FFH	1, 8	√	√	√	√	√	√	√	√	√
F0258H	Timer RDe output master enable register 2	TRDOER2	00H	1, 8	√	√	√	√	√	√	√	√	√
F0259H	Timer RDe output control register	TRDOCR	00H	1, 8	√	√	√	√	√	√	√	√	√
F025AH	Timer RDe digital filter function select register 0	TRDDF0	00H	1, 8	√	√	√	√	√	√	√	√	√
F025BH	Timer RDe digital filter function select register 1	TRDDF1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0260H	Timer RDe control register 0	TRDCR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0261H	Timer RDe I/O control register A0	TRDIORA0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0262H	Timer RDe I/O control register C0	TRDIORC0	88H	1, 8	√	√	√	√	√	√	√	√	√
F0263H	Timer RDe status register 0	TRDSR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0264H	Timer RDe interrupt enable register 0	TRDIER0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0265H	Timer RDe PWM output level control register 0	TRDPOCR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F0266H F0267H	Timer RDe counter 0	TRD0	0000H	16	√	√	√	√	√	√	√	√	√
F0268H F0269H	Timer RDe general register A0	TRDGRA0	FFFFH	16	√	√	√	√	√	√	√	√	√
F026AH F026BH	Timer RDe general register B0	TRDGRB0	FFFFH	16	√	√	√	√	√	√	√	√	√
F0270H	Timer RDe control register 1	TRDCR1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0271H	Timer RDe I/O control register A1	TRDIORA1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0272H	Timer RDe I/O control register C1	TRDIORC1	88H	1, 8	√	√	√	√	√	√	√	√	√
F0273H	Timer RDe status register 1	TRDSR1	40H	1, 8	√	√	√	√	√	√	√	√	√
F0274H	Timer RDe interrupt enable register 1	TRDIER1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0275H	Timer RDe PWM output level control register 1	TRDPOCR1	00H	1, 8	√	√	√	√	√	√	√	√	√
F0276H F0277H	Timer RDe counter 1	TRD1	0000H	16	√	√	√	√	√	√	√	√	√
F0278H F0279H	Timer RDe general register A1	TRDGRA1	FFFFH	16	√	√	√	√	√	√	√	√	√
F027AH F027BH	Timer RDe general register B1	TRDGRB1	FFFFH	16	√	√	√	√	√	√	√	√	√
F0280H F0281H	Timer RDe extended compare register B0	TRDCMPB0	FFFFH	16	√	√	√	√	√	√	√	√	√
F0284H F0285H	Timer RDe extended compare register A1	TRDCMPA1	FFFFH	16	√	√	√	√	√	√	√	√	√
F0288H F0289H	Timer RDe extended compare register B1	TRDCMPB1	FFFFH	16	√	√	√	√	√	√	√	√	√
F028CH F028DH	Timer RDe A/D trigger compare register 0	TRDADTC0	FFFFH	16	√	√	√	√	√	√	√	√	√
F0290H F0291H	Timer RDe A/D trigger compare register 1	TRDADTC1	FFFFH	16	√	√	√	√	√	√	√	√	√
F0296H	Timer RDe reload status flag register	TRDRSF01	0000H	16	√	√	√	√	√	√	√	√	√
	Timer RDe reload status flag register 0	TRDRSF0		1, 8									
F0297H	Timer RDe reload status flag register 1	TRDRSF1		1, 8									
F0298H	Timer RDe A/D trigger control register	TRDADCR	00H	1, 8	√	√	√	√	√	√	√	√	√
F029AH	Timer RDe extended PWM mode register 0	TRDEMR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F029BH	Timer RDe extended PWM mode register 1	TRDEMR1	00H	1, 8	√	√	√	√	√	√	√	√	√
F02A0H	Comparator control register	CMPCTL	00H	1, 8	√	√	√	√	√	—	—	—	—
F02A1H	Comparator I/O select register	CMPSEL	00H	1, 8	√	√	√	√	√	—	—	—	—
F02A2H	Comparator output monitor register	CMPMON	00H	1, 8	√	√	√	√	√	—	—	—	—

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (9/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F02B0H to F02BFH	Application Accelerator Unit (AAU) window registers See Table 3-1 to Table 3-3.	—	—	—	√	√	√	√	√	√	√	√	√
F02C0H	Peripheral enable register 1	PER1	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C1H	Peripheral enable register 2	PER2	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C2H	CAN clock select register	CANCKSEL	00H	1, 8	√	√	√	√	√	—	—	—	—
F02C3H	LIN clock select register	LINCKSEL	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C4H	Clock select register	CKSEL	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C5H	PLL control register	PLLCTL	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C6H	PLL status register	PLLSTS	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C7H	f_{MP} clock division register	MDIV	00H/01H	8	√	√	√	√	√	√	√	√	√
F02C8H	RTC clock select register	RTCCL	00H	1, 8	√	√	√	√	√	√	√	√	√
F02C9H	POR/CLM reset confirmation register	POCRES	00H	1, 8	√	√	√	√	√	√	√	√	√
F02CAH	STOP status output control register	STPSTC	00H	1, 8	√	√	√	√	—	√	√	√	—
F02CCH	Clock monitor test register	CLMTES	00H	1, 8	√	√	√	√	√	√	√	√	√
F02D0H	High-speed DTC control register 0	HDTCCR0	00H	1, 8	√	√	√	√	√	√	√	√	√
F02D2H	High-speed DTC transfer count register 0	HDTCCT0	00H	1, 8	√	√	√	√	√	√	√	√	√
F02D3H	High-speed DTC transfer count reload register 0	HDTRLD0	00H	1, 8	√	√	√	√	√	√	√	√	√
F02D4H F02D5H	High-speed DTC source address register 0	HDTSAR0	0000H	16	√	√	√	√	√	√	√	√	√
F02D6H F02D7H	High-speed DTC destination address register 0	HDTDAR0	0000H	16	√	√	√	√	√	√	√	√	√
F02D8H	High-speed DTC control register 1	HDTCCR1	00H	1, 8	√	√	√	√	√	√	√	√	√
F02DAH	High-speed DTC transfer count register 1	HDTCCT1	00H	1, 8	√	√	√	√	√	√	√	√	√
F02DBH	High-speed DTC transfer count reload register 1	HDTRLD1	00H	1, 8	√	√	√	√	√	√	√	√	√
F02DCH F02DDH	High-speed DTC source address register 1	HDTSAR1	0000H	16	√	√	√	√	√	√	√	√	√
F02DEH F02DFH	High-speed DTC destination address register 1	HDTDAR1	0000H	16	√	√	√	√	√	√	√	√	√
F02E0H	DTC base address register	DTCBAR	FDH	8	√	√	√	√	√	√	√	√	√
F02E1H	High-speed DTC channel select register 0	SELHS0	3FH	1, 8	√	√	√	√	√	√	√	√	√
F02E2H	High-speed DTC channel select register 1	SELHS1	3FH	1, 8	√	√	√	√	√	√	√	√	√
F02E8H	DTC activation enable register 0	DTCEN0	00H	1, 8	√	√	√	√	√	√	√	√	√
F02E9H	DTC activation enable register 1	DTCEN1	00H	1, 8	√	√	√	√	√	√	√	√	√
F02EAH	DTC activation enable register 2	DTCEN2	00H	1, 8	√	√	√	√	√	√	√	√	√
F02EBH	DTC activation enable register 3	DTCEN3	00H	1, 8	√	√	√	√	√	√	√	√	√
F02ECH	DTC activation enable register 4	DTCEN4	00H	1, 8	√	√	√	√	√	√	√	√	√
F02EDH	DTC activation enable register 5	DTCEN5	00H	1, 8	√	√	√	√	√	—	—	—	—
F02F0H	Flash memory CRC control register	CRC0CTL	00H	1, 8	√	√	√	√	√	√	√	√	√
F02F2H F02F3H	Flash memory CRC operation result register	PGCRCL	0000H	16	√	√	√	√	√	√	√	√	√
F02F9H	CRC operation mode control register	CRCMD	00H	8	√	√	√	√	√	√	√	√	√
F02FAH F02FBH	CRC data register	CRCD	0000H	16	√	√	√	√	√	√	√	√	√
F0300H	Channel 0 nominal bitrate configuration register L	C0NCFGL	0000H	16	√	√	√	√	√	—	—	—	—
		C0NCFGLL		8									
F0301H		C0NCFGLH		8									
F0302H	Channel 0 nominal bitrate configuration register H	C0NCFGH	0000H	16	√	√	√	√	√	—	—	—	—
		C0NCFGHL		8									
F0303H		C0NCFGHH		8									
F0304H	Channel 0 control register L	C0CTRL	0005H	16	√	√	√	√	√	—	—	—	—
		C0CTRLL		8									
F0305H		C0CTRLH		8									
F0306H	Channel 0 control register H	C0CTRH	0000H	16	√	√	√	√	√	—	—	—	—
		C0CTRHL		8									
F0307H		C0CTRHH		8									

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (10/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0308H	Channel 0 status register L	C0STSL	0005H	16	√	√	√	√	√	—	—	—	—
		C0STSLL		8									
F0309H		C0STSLH		8									
F030AH	Channel 0 status register H	C0STSH	0000H	16	√	√	√	√	√	—	—	—	—
		C0STSHL		8									
F030BH		C0STSHH		8									
F030CH	Channel 0 error flag register L	C0ERFLL	0000H	16	√	√	√	√	√	—	—	—	—
		C0ERFLLL		8									
F030DH		C0ERFLLH		8									
F030EH	Channel 0 error flag register H	C0ERFLH	0000H	16	√	√	√	√	√	—	—	—	—
		C0ERFLHL		8									
F030FH		C0ERFLHH		8									
F0310H	Global IP version register L	GIPVL	8143H	16	√	√	√	√	√	—	—	—	—
		GIPVLL		8									
F0311H		GIPVLH		8									
F0312H	Global IP version register H	GIPVH	3C8BH	16	√	√	√	√	√	—	—	—	—
		GIPVHL		8									
F0313H		GIPVHH		8									
F0314H	Global configuration register L	GCFGL	0000H	16	√	√	√	√	√	—	—	—	—
		GCFGLL		8									
F0315H		GCFGLH		8									
F0316H	Global configuration register H	GCFGH	0000H	16	√	√	√	√	√	—	—	—	—
		GCFGHL		8									
F0317H		GCFGHH		8									
F0318H	Global control register L	GCTRL	0000H	16	√	√	√	√	√	—	—	—	—
		GCTRLL		8									
F0319H		GCTRLH		8									
F031AH	Global control register H	GCTRH	0000H	16	√	√	√	√	√	—	—	—	—
		GCTRHL		8									
F031BH		—		—									
F031CH	Global status register	GSTS	000DH	16	√	√	√	√	√	—	—	—	—
		GSTSL		8									
F031DH		—		—									
F0320H	Global error flag register L	GERFLL	0000H	16	√	√	√	√	√	—	—	—	—
		GERFLLL		8									
F0321H		—		—									
F0322H	Global error flag register H	GERFLH	0000H	16	√	√	√	√	√	—	—	—	—
		GERFLHL		8									
F0323H		—		—									
F0324H F0325H	Global timestamp counter register	GTSC	0000H	16	√	√	√	√	√	—	—	—	—
F0328H	Global acceptance filter list entry control register	GAFLECTR	0000H	16	√	√	√	√	√	—	—	—	—
		—		—									
F0329H		GAFLECTRH		8									
F032EH	Global acceptance filter list configuration register	GAFLCFG	0000H	16	√	√	√	√	√	—	—	—	—
		GAFLCFGL		8									
F032FH		—		—									
F0330H	RX message buffer number register	RMNB	0000H	16	√	√	√	√	√	—	—	—	—
		RMNBL		8									
F0331H		RMNBH		8									

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (11/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0334H	RX message buffer new data register	RMND	0000H	16	√	√	√	√	√	—	—	—	—
		RMNDL		8									
F0335H		RMNDH		8									
F0338H	RX message buffer interrupt enable configuration register	RMIEC	0000H	16	√	√	√	√	√	—	—	—	—
		RMIECL		8									
F0339H		RMIECH		8									
F033CH	RX FIFO configuration / control register 0	RFCC0	0000H	16	√	√	√	√	√	—	—	—	—
		RFCC0L		8									
F033DH		RFCC0H		8									
F0340H	RX FIFO configuration / control register 1	RFCC1	0000H	16	√	√	√	√	√	—	—	—	—
		RFCC1L		8									
F0341H		RFCC1H		8									
F0344H	RX FIFO status register 0	RFSTS0	0000H	16	√	√	√	√	√	—	—	—	—
		RFSTS0L		8									
F0345H		RFSTS0H		8									
F0348H	RX FIFO status register 1	RFSTS1	0000H	16	√	√	√	√	√	—	—	—	—
		RFSTS1L		8									
F0349H		RFSTS1H		8									
F034CH	RX FIFO pointer control register 0	RFPCTR0	0000H	16	√	√	√	√	√	—	—	—	—
		RFPCTR0L		8									
F034DH		—		—									
F0350H	RX FIFO pointer control register 1	RFPCTR1	0000H	16	√	√	√	√	√	—	—	—	—
		RFPCTR1L		8									
F0351H		—		—									
F0354H	Common FIFO configuration / control register L	CFCCL	0000H	16	√	√	√	√	√	—	—	—	—
		CFCCLL		8									
F0355H		CFCCLH		8									
F0356H	Common FIFO configuration / control register H	CFCCH	0000H	16	√	√	√	√	√	—	—	—	—
		CFCCHL		8									
F0357H		CFCCHH		8									
F0358H	Common FIFO status register	CFSTS	0000H	16	√	√	√	√	√	—	—	—	—
		CFSTSL		8									
F0359H		CFSTSH		8									
F035CH	Common FIFO pointer control register	CFPCTR	0000H	16	√	√	√	√	√	—	—	—	—
		CFPCTRL		8									
F035D		—		—									
F0360H	FIFO empty status register	FESTS	0103H	16	√	√	√	√	√	—	—	—	—
		FESTSL		8									
F0361H		FESTSH		8									
F0364H	FIFO full status register	FFSTS	0000H	16	√	√	√	√	√	—	—	—	—
		FFSTSL		8									
F0365H		FFSTSH		8									
F0368H	FIFO message lost status register	FMSTS	0000H	16	√	√	√	√	√	—	—	—	—
		FMSTSL		8									
F0369H		FMSTSH		8									
F036CH	RX FIFO interrupt flag status register	RFISTS	0000H	16	√	√	√	√	√	—	—	—	—
		RFISTSL		8									
F036DH		—		—									
F0370H	TX message buffer control register 0	TMC0	00H	8	√	√	√	√	√	—	—	—	—
F0371H	TX message buffer control register 1	TMC1	00H	8	√	√	√	√	√	—	—	—	—
F0372H	TX message buffer control register 2	TMC2	00H	8	√	√	√	√	√	—	—	—	—
F0373H	TX message buffer control register 3	TMC3	00H	8	√	√	√	√	√	—	—	—	—

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (12/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F0374H	TX message buffer status register 0	TMSTS0	00H	8	√	√	√	√	√	—	—	—	—
F0375H	TX message buffer status register 1	TMSTS1	00H	8	√	√	√	√	√	—	—	—	—
F0376H	TX message buffer status register 2	TMSTS2	00H	8	√	√	√	√	√	—	—	—	—
F0377H	TX message buffer status register 3	TMSTS3	00H	8	√	√	√	√	√	—	—	—	—
F0378H	TX message buffer transmission request status register	TMTRSTS	0000H	16	√	√	√	√	√	—	—	—	—
		TMTRSTSL		8									
F0379H		—		—									
F037CH	TX message buffer transmission abort request status register	TMTARSTS	0000H	16	√	√	√	√	√	—	—	—	—
		TMTARSTSL		8									
F037DH		—		—									
F0380H	TX message buffer transmission completion status register	TMTCSTS	0000H	16	√	√	√	√	√	—	—	—	—
		TMTCSTSL		8									
F0381H		—		—									
F0384H	TX message buffer transmission abort status register	TMTASTS	0000H	16	√	√	√	√	√	—	—	—	—
		TMTASTSL		8									
F0385H		—		—									
F0388H	TX message buffer interrupt enable configuration register	TMIEC	0000H	16	√	√	√	√	√	—	—	—	—
		TMIECL		8									
F0389H		—		—									
F0398H	TX history list configuration / control register	THLCC	0000H	16	√	√	√	√	√	—	—	—	—
		THLCCL		8									
F0399H		THLCCH		8									
F039CH	TX history list status register	THLSTS	0001H	16	√	√	√	√	√	—	—	—	—
		THLSTSL		8									
F039DH		THLSTSH		8									
F03A0H	TX history list pointer control register	THLPCTR	0000H	16	√	√	√	√	√	—	—	—	—
		THLPCTRL		8									
F03A1H		—		—									
F03A4H	Global TX interrupt status register	GTINTSTS	0000H	16	√	√	√	√	√	—	—	—	—
		GTINTSTSL		8									
F03A5H		—		—									
F03AAH	Global test configuration register	GTSTCFG	0000H	16	√	√	√	√	√	—	—	—	—
		GTSTCFGL		8									
F03ABH		—		—									
F03ACH	Global test control register	GTSTCTR	0000H	16	√	√	√	√	√	—	—	—	—
		GTSTCTRL		8									
F03ADH		—		—									
F03B0H	Global FD configuration register	GFDCFG	0000H	16	√	√	√	√	√	—	—	—	—
		GFDCFGL		8									
F03B1H		GFDCFGH		8									
F03B8H F03B9H	Global lock key register	GLOCKK	0000H	16	√	√	√	√	√	—	—	—	—
F03C0H	Global AFL ignore entry register	GAFLIGNENT	0000H	16	√	√	√	√	√	—	—	—	—
		GAFLIGNENTL		8									
F03C1H		—		—									
F03C4H F03C5H	Global AFL ignore control register	GAFLIGNCTR	0000H	16	√	√	√	√	√	—	—	—	—
F03D0H	Global pretended network filter list entry control register	GPFLECTR	0000H	16	√	√	√	√	√	—	—	—	—
		—		—									
F03D1H		GPFLECTRH		8									
F03D6H	Global pretended network filter list configuration register	GPFLCFG	0000H	16	√	√	√	√	√	—	—	—	—
		—		—									
F03D7H		GPFLCFGH		8									

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (13/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F03D8H F03D9H	Global reset control register	GRSTC	0000H	16	√	√	√	√	√	—	—	—	—
F03DCH F03DDH	RS-CANFD lite global RAM window control register	CFDGRWC	0000H	16	√	√	√	√	√	—	—	—	—
F0400H	Channel 0 data bit rate configuration register L	C0DCFGL	0000H	16	√	√	√	√	√	—	—	—	—
		C0DCFGLL		8									
F0401H		C0DCFGLH		8									
F0402H	Channel 0 data bit rate configuration register H	C0DCFGH	0000H	16	√	√	√	√	√	—	—	—	—
		C0DCFGHL		8									
F0403H		C0DCFGHH		8									
F0404H	Channel 0 CAN-FD configuration register L	C0FDCFGL	0000H	16	√	√	√	√	√	—	—	—	—
		C0FDCFGLL		8									
F0405H		C0FDCFGLH		8									
F0406H	Channel 0 CAN-FD configuration register H	C0FDCFGH	0000H	16	√	√	√	√	√	—	—	—	—
		C0FDCFGHL		8									
F0407H		C0FDCFGHH		8									
F0408H	Channel 0 CAN-FD control register L	C0FDCTRL	0000H	16	√	√	√	√	√	—	—	—	—
		C0FDCTRLL		8									
F0409H		—		—									
F040AH F040BH	Channel 0 CAN-FD control register H	C0FDCTRH	0000H	16	√	√	√	√	√	—	—	—	—
F040CH	Channel 0 CAN-FD status register L	C0FDSTSL	0000H	16	√	√	√	√	√	—	—	—	—
		C0FDSTSLL		8									
F040DH		C0FDSTSLH		8									
F040EH	Channel 0 CAN-FD status register H	C0FDSTSH	0000H	16	√	√	√	√	√	—	—	—	—
		C0FDSTSHL		8									
F040FH		C0FDSTSHH		8									
F0410H F0411H	Channel 0 CAN-FD CRC register L	C0FDCRCL	0000H	16	√	√	√	√	√	—	—	—	—
F0412H F0413H	Channel 0 CAN-FD CRC register H	C0FDCRCH	0000H	16	√	√	√	√	√	—	—	—	—
F0420H to F067FH	RS-CANFD lite window registers See Table 4-1 to Table 4-4.	—	—	—	√	√	√	√	√	—	—	—	—
F06A0H F06A1H	A/D data register 0 mirror area	ADDR0M	0000H	16	√	√	√	√	√	√	√	√	√
F06A2H F06A3H	A/D data register 1 mirror area	ADDR1M	0000H	16	√	√	√	√	√	√	√	√	√
F06A4H F06A5H	A/D data register 2 mirror area	ADDR2M	0000H	16	√	√	√	√	√	√	√	√	√
F06A6H F06A7H	A/D data register 3 mirror area	ADDR3M	0000H	16	√	√	√	√	√	√	√	√	√
F06A8H F06A9H	A/D data register 4 mirror area	ADDR4M	0000H	16	√	√	√	√	√	√	√	√	√
F06AAH F06ABH	A/D data register 5 mirror area	ADDR5M	0000H	16	√	√	√	√	√	√	√	√	√
F06ACH F06ADH	A/D data register 6 mirror area	ADDR6M	0000H	16	√	√	√	√	√	√	√	√	√
F06AEH F06AFH	A/D data register 7 mirror area	ADDR7M	0000H	16	√	√	√	√	√	√	√	√	√
F06B0H to F06BFH	A/D converter window registers See Table 5-1 to Table 5-11.	—	—	—	√	√	√	√	√	√	√	√	√
F06C1H to F06EEH	LIN/UART module (RLIN3) window registers See Table 6-1 and Table 6-2.	—	—	—	√	√	√	√	√	√	√	√	√

Table 2-1. List of Extended Special Function Registers (2nd SFR) for RL78/F23, F24 (14/14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06F0H F06F1H	Timer RJ counter register 0	TRJ0	FFFFH	16	√	√	√	√	√	√	√	√	√
F0780H	Event output destination select register 00	ELSELR00	00H	1, 8	√	√	√	√	√	—	—	—	—
F0781H	Event output destination select register 01	ELSELR01	00H	1, 8	√	√	√	√	√	—	—	—	—
F0782H	Event output destination select register 02	ELSELR02	00H	1, 8	√	√	√	√	√	—	—	—	—
F0783H	Event output destination select register 03	ELSELR03	00H	1, 8	√	√	√	√	√	—	—	—	—
F0784H	Event output destination select register 04	ELSELR04	00H	1, 8	√	√	√	√	√	—	—	—	—
F0785H	Event output destination select register 05	ELSELR05	00H	1, 8	√	√	√	√	√	—	—	—	—
F0786H	Event output destination select register 06	ELSELR06	00H	1, 8	√	√	√	√	√	—	—	—	—
F0787H	Event output destination select register 07	ELSELR07	00H	1, 8	√	√	√	√	√	—	—	—	—
F0788H	Event output destination select register 08	ELSELR08	00H	1, 8	√	√	√	√	√	—	—	—	—
F0789H	Event output destination select register 09	ELSELR09	00H	1, 8	√	√	√	√	√	—	—	—	—
F078AH	Event output destination select register 10	ELSELR10	00H	1, 8	√	√	√	√	√	—	—	—	—
F078BH	Event output destination select register 11	ELSELR11	00H	1, 8	√	√	√	√	√	—	—	—	—
F078CH	Event output destination select register 12	ELSELR12	00H	1, 8	√	√	√	√	√	—	—	—	—
F078DH	Event output destination select register 13	ELSELR13	00H	1, 8	√	√	√	√	√	—	—	—	—
F078EH	Event output destination select register 14	ELSELR14	00H	1, 8	√	√	√	√	√	—	—	—	—
F078FH	Event output destination select register 15	ELSELR15	00H	1, 8	√	√	√	√	√	—	—	—	—
F0790H	Event output destination select register 16	ELSELR16	00H	1, 8	√	√	√	√	√	—	—	—	—
F0791H	Event output destination select register 17	ELSELR17	00H	1, 8	√	√	√	√	√	—	—	—	—
F0792H	Event output destination select register 18	ELSELR18	00H	1, 8	√	√	√	√	√	—	—	—	—
F0793H	Event output destination select register 19	ELSELR19	00H	1, 8	√	√	√	√	√	—	—	—	—
F0794H	Event output destination select register 20	ELSELR20	00H	1, 8	√	√	√	√	√	—	—	—	—
F0795H	Event output destination select register 21	ELSELR21	00H	1, 8	√	√	√	√	√	—	—	—	—
F0796H	Event output destination select register 22	ELSELR22	00H	1, 8	√	√	√	√	√	—	—	—	—
F0797H	Event output destination select register 23	ELSELR23	00H	1, 8	√	√	√	√	√	—	—	—	—
F0798H	Event output destination select register 24	ELSELR24	00H	1, 8	√	√	√	√	√	—	—	—	—
F0799H	Event output destination select register 25	ELSELR25	00H	1, 8	√	√	√	√	√	—	—	—	—
F07C0H	CAN RAM ECC control register	CFDECCTL	0010H	16	√	√	√	√	√	—	—	—	—
		CFDECCTLL		8									
F07C1H		CFDECCTLH		8									
F07C4H	CAN RAM ECC test mode control register	CFDECTMC	0000H	16	√	√	√	√	√	—	—	—	—
		CFDECTMCL		8									
F07C5H		CFDECTMCH		8									
F07C8H	CAN RAM ECC decoder input ECC bit replacement test register	CFDECERDB	00H	8	√	√	√	√	√	—	—	—	—
F07CAH	CAN RAM ECC redundant bit test register	CFDECHORD	00H	8	√	√	√	√	√	—	—	—	—
F07CBH	CAN RAM ECC syndrome test register	CFDECSYND	00H	8	√	√	√	√	√	—	—	—	—
F07CCH F07CDH	CAN RAM ECC decoder input data replacement test register L	CFDECTEDL	0000H	16	√	√	√	√	√	—	—	—	—
F07CEH F07CFH	CAN RAM ECC decoder input data replacement test register H	CFDECTEDH	0000H	16	√	√	√	√	√	—	—	—	—
F07D0H F07D1H	CAN RAM ECC error address register	CFDECEAD	0000H	16	√	√	√	√	√	—	—	—	—

3. List of Application Accelerator Unit Window Registers for RL78/F23, F24

The table below lists the application accelerator unit (AAU) window registers for RL78/F23, F24 products.

Table 3-1. List of Application Accelerator Unit Window Registers for RL78/F23, F24 (Page.0)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]
F02B0H F02B1H	AAU data register 0	ADTREG0	0000H	16
F02B2H F02B3H	AAU data register 1	ADTREG1	0000H	16
F02B4H F02B5H	AAU data register 2	ADTREG2	0000H	16
F02B6H F02B7H	AAU data register 3	ADTREG3	0000H	16
F02BAH	AAU control register	ACTLREG	00H	1, 8
F02BBH	PI control coefficient range setting register / Current limit duty register	AKRAG / ADUTYMX	00H	8
F02BCH F02BDH	D-axis current reference register / DC/DC channel.1 current reference register	AIDREF / AL1REF	0000H	16
F02BEH F02BFH	Q-axis current reference register / DC/DC channel.2 current reference register	AIQREF / AL2REF	0000H	16

Note AAUWINR.AAUPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Table 3-2. List of Application Accelerator Unit Window Registers for RL78/F23, F24 (Page.1)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]
F02B0H F02B1H	D-axis proposal coefficient register / DC/DC channel.3 current reference register	AKPD / AL3REF	0000H	16
F02B2H F02B3H	D-axis integral coefficient register / DC/DC channel.1 offset current register	AKID / AL1OFS	0000H	16
F02B4H F02B5H	Q-axis proposal coefficient register / DC/DC channel.2 offset current register	AKPQ / AL2OFS	0000H	16
F02B6H F02B7H	Q-axis integral coefficient register / DC/DC channel.3 offset current register	AKIQ / AL3OFS	0000H	16
F02BCH F02BDH	Current limit register / DC/DC proportional coefficient 1 register	AILIM / AKI1	0000H	16
F02BEH F02BFH	PI control limit register / DC/DC proportional coefficient 2 register	APILIM / AKI2	0000H	16

Note AAUWINR.AAUPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Table 3-3. List of Application Accelerator Unit Window Registers for RL78/F23, F24 (Page.2)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]
F02B0H F02B1H	D-axis current buffer register L / DC/DC channel.1 previous duty register	AIDBFL / ADUTYL1	0000H	16
F02B2H F02B3H	D-axis current buffer register H / DC/DC channel.2 previous duty register	AIDBFH / ADUTYL2	0000H	16
F02B4H F02B5H	Q-axis current buffer register L / DC/DC channel.3 previous duty register	AIQBFL / ADUTYL3	0000H	16
F02B6H F02B7H	Q-axis current buffer register H / DC/DC channel.1 previous current register	AIQBFH / AIPL1	0000H	16
F02B8H F02B9H	D-axis limit over current register / DC/DC channel.2 previous current register	ADOVER / AIPL2	0000H	16
F02BAH F02BBH	Q-axis limit over current register / DC/DC channel.3 previous current register	AQOVER / AIPL3	0000H	16

Note AAUWINR.AAUPAGE[1:0] bits are the condition of 10B (page.2 access selection).

4. List of RS-CANFD lite Window Registers for RL78/F24

The table below lists the RS-CANFD lite window registers for RL78/F24 products.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (1/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0420H	Global acceptance filter list ID register 0 L	GAFLID0LL	GAFLID0L	0000H	8, 16
F0421H		GAFLID0LH			
F0422H	Global acceptance filter list ID register 0 H	GAFLID0HL	GAFLID0H	0000H	8, 16
F0423H		GAFLID0HH			
F0424H	Global acceptance filter list mask register 0 L	GAFLM0LL	GAFLM0L	0000H	8, 16
F0425H		GAFLM0LH			
F0426H	Global acceptance filter list mask register 0 H	GAFLM0HL	GAFLM0H	0000H	8, 16
F0427H		GAFLM0HH			
F0428H	Global acceptance filter list pointer 0 register 0 L	GAFLP00LL	GAFLP00L	0000H	8, 16
F0429H		GAFLP00LH			
F042AH	Global acceptance filter list pointer 0 register 0 H	GAFLP00HL	GAFLP00H	0000H	8, 16
F042BH		GAFLP00HH			
F042CH	Global acceptance filter list pointer 1 register 0 L	GAFLP10LL	GAFLP10L	0000H	8, 16
F042DH		GAFLP10LH			
F0430H	Global acceptance filter list ID register 1 L	GAFLID1LL	GAFLID1L	0000H	8, 16
F0431H		GAFLID1LH			
F0432H	Global acceptance filter list ID register 1 H	GAFLID1HL	GAFLID1H	0000H	8, 16
F0433H		GAFLID1HH			
F0434H	Global acceptance filter list mask register 1 L	GAFLM1LL	GAFLM1L	0000H	8, 16
F0435H		GAFLM1LH			
F0436H	Global acceptance filter list mask register 1 H	GAFLM1HL	GAFLM1H	0000H	8, 16
F0437H		GAFLM1HH			
F0438H	Global acceptance filter list pointer 0 register 1 L	GAFLP01LL	GAFLP01L	0000H	8, 16
F0439H		GAFLP01LH			
F043AH	Global acceptance filter list pointer 0 register 1 H	GAFLP01HL	GAFLP01H	0000H	8, 16
F043BH		GAFLP01HH			
F043CH	Global acceptance filter list pointer 1 register 1 L	GAFLP11LL	GAFLP11L	0000H	8, 16
F043DH		GAFLP11LH			
F0440H	Global acceptance filter list ID register 2 L	GAFLID2LL	GAFLID2L	0000H	8, 16
F0441H		GAFLID2LH			
F0442H	Global acceptance filter list ID register 2 H	GAFLID2HL	GAFLID2H	0000H	8, 16
F0443H		GAFLID2HH			
F0444H	Global acceptance filter list mask register 2 L	GAFLM2LL	GAFLM2L	0000H	8, 16
F0445H		GAFLM2LH			
F0446H	Global acceptance filter list mask register 2 H	GAFLM2HL	GAFLM2H	0000H	8, 16
F0447H		GAFLM2HH			
F0448H	Global acceptance filter list pointer 0 register 2 L	GAFLP02LL	GAFLP02L	0000H	8, 16
F0449H		GAFLP02LH			
F044AH	Global acceptance filter list pointer 0 register 2 H	GAFLP02HL	GAFLP02H	0000H	8, 16
F044BH		GAFLP02HH			
F044CH	Global acceptance filter list pointer 1 register 2 L	GAFLP12LL	GAFLP12L	0000H	8, 16
F044DH		GAFLP12LH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (2/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0450H	Global acceptance filter list ID register 3 L	GAFLID3LL	GAFLID3L	0000H	8, 16
F0451H		GAFLID3LH			
F0452H	Global acceptance filter list ID register 3 H	GAFLID3HL	GAFLID3H	0000H	8, 16
F0453H		GAFLID3HH			
F0454H	Global acceptance filter list mask register 3 L	GAFLM3LL	GAFLM3L	0000H	8, 16
F0455H		GAFLM3LH			
F0456H	Global acceptance filter list mask register 3 H	GAFLM3HL	GAFLM3H	0000H	8, 16
F0457H		GAFLM3HH			
F0458H	Global acceptance filter list pointer 0 register 3 L	GAFLP03LL	GAFLP03L	0000H	8, 16
F0459H		GAFLP03LH			
F045AH	Global acceptance filter list pointer 0 register 3 H	GAFLP03HL	GAFLP03H	0000H	8, 16
F045BH		GAFLP03HH			
F045CH	Global acceptance filter list pointer 1 register 3 L	GAFLP13LL	GAFLP13L	0000H	8, 16
F045DH		GAFLP13LH			
F0460H	Global acceptance filter list ID register 4 L	GAFLID4LL	GAFLID4L	0000H	8, 16
F0461H		GAFLID4LH			
F0462H	Global acceptance filter list ID register 4 H	GAFLID4HL	GAFLID4H	0000H	8, 16
F0463H		GAFLID4HH			
F0464H	Global acceptance filter list mask register 4 L	GAFLM4LL	GAFLM4L	0000H	8, 16
F0465H		GAFLM4LH			
F0466H	Global acceptance filter list mask register 4 H	GAFLM4HL	GAFLM4H	0000H	8, 16
F0467H		GAFLM4HH			
F0468H	Global acceptance filter list pointer 0 register 4 L	GAFLP04LL	GAFLP04L	0000H	8, 16
F0469H		GAFLP04LH			
F046AH	Global acceptance filter list pointer 0 register 4 H	GAFLP04HL	GAFLP04H	0000H	8, 16
F046BH		GAFLP04HH			
F046CH	Global acceptance filter list pointer 1 register 4 L	GAFLP14LL	GAFLP14L	0000H	8, 16
F046DH		GAFLP14LH			
F0470H	Global acceptance filter list ID register 5 L	GAFLID5LL	GAFLID5L	0000H	8, 16
F0471H		GAFLID5LH			
F0472H	Global acceptance filter list ID register 5 H	GAFLID5HL	GAFLID5H	0000H	8, 16
F0473H		GAFLID5HH			
F0474H	Global acceptance filter list mask register 5 L	GAFLM5LL	GAFLM5L	0000H	8, 16
F0475H		GAFLM5LH			
F0476H	Global acceptance filter list mask register 5 H	GAFLM5HL	GAFLM5H	0000H	8, 16
F0477H		GAFLM5HH			
F0478H	Global acceptance filter list pointer 0 register 5 L	GAFLP05LL	GAFLP05L	0000H	8, 16
F0479H		GAFLP05LH			
F047AH	Global acceptance filter list pointer 0 register 5 H	GAFLP05HL	GAFLP05H	0000H	8, 16
F047BH		GAFLP05HH			
F047CH	Global acceptance filter list pointer 1 register 5 L	GAFLP15LL	GAFLP15L	0000H	8, 16
F047DH		GAFLP15LH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (3/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0480H	Global acceptance filter list ID register 6 L	GAFLID6LL	GAFLID6L	0000H	8, 16
F0481H		GAFLID6LH			
F0482H	Global acceptance filter list ID register 6 H	GAFLID6HL	GAFLID6H	0000H	8, 16
F0483H		GAFLID6HH			
F0484H	Global acceptance filter list mask register 6 L	GAFLM6LL	GAFLM6L	0000H	8, 16
F0485H		GAFLM6LH			
F0486H	Global acceptance filter list mask register 6 H	GAFLM6HL	GAFLM6H	0000H	8, 16
F0487H		GAFLM6HH			
F0488H	Global acceptance filter list pointer 0 register 6 L	GAFLP06LL	GAFLP06L	0000H	8, 16
F0489H		GAFLP06LH			
F048AH	Global acceptance filter list pointer 0 register 6 H	GAFLP06HL	GAFLP06H	0000H	8, 16
F048BH		GAFLP06HH			
F048CH	Global acceptance filter list pointer 1 register 6 L	GAFLP16LL	GAFLP16L	0000H	8, 16
F048DH		GAFLP16LH			
F0490H	Global acceptance filter list ID register 7 L	GAFLID7LL	GAFLID7L	0000H	8, 16
F0491H		GAFLID7LH			
F0492H	Global acceptance filter list ID register 7 H	GAFLID7HL	GAFLID7H	0000H	8, 16
F0493H		GAFLID7HH			
F0494H	Global acceptance filter list mask register 7 L	GAFLM7LL	GAFLM7L	0000H	8, 16
F0495H		GAFLM7LH			
F0496H	Global acceptance filter list mask register 7 H	GAFLM7HL	GAFLM7H	0000H	8, 16
F0497H		GAFLM7HH			
F0498H	Global acceptance filter list pointer 0 register 7 L	GAFLP07LL	GAFLP07L	0000H	8, 16
F0499H		GAFLP07LH			
F049AH	Global acceptance filter list pointer 0 register 7 H	GAFLP07HL	GAFLP07H	0000H	8, 16
F049BH		GAFLP07HH			
F049CH	Global acceptance filter list pointer 1 register 7 L	GAFLP17LL	GAFLP17L	0000H	8, 16
F049DH		GAFLP17LH			
F04A0H	Global acceptance filter list ID register 8 L	GAFLID8LL	GAFLID8L	0000H	8, 16
F04A1H		GAFLID8LH			
F04A2H	Global acceptance filter list ID register 8 H	GAFLID8HL	GAFLID8H	0000H	8, 16
F04A3H		GAFLID8HH			
F04A4H	Global acceptance filter list mask register 8 L	GAFLM8LL	GAFLM8L	0000H	8, 16
F04A5H		GAFLM8LH			
F04A6H	Global acceptance filter list mask register 8 H	GAFLM8HL	GAFLM8H	0000H	8, 16
F04A7H		GAFLM8HH			
F04A8H	Global acceptance filter list pointer 0 register 8 L	GAFLP08LL	GAFLP08L	0000H	8, 16
F04A9H		GAFLP08LH			
F04AAH	Global acceptance filter list pointer 0 register 8 H	GAFLP08HL	GAFLP08H	0000H	8, 16
F04ABH		GAFLP08HH			
F04ACH	Global acceptance filter list pointer 1 register 8 L	GAFLP18LL	GAFLP18L	0000H	8, 16
F04ADH		GAFLP18LH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (4/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04B0H	Global acceptance filter list ID register 9 L	GAFLID9LL	GAFLID9L	0000H	8, 16
F04B1H		GAFLID9LH			
F04B2H	Global acceptance filter list ID register 9 H	GAFLID9HL	GAFLID9H	0000H	8, 16
F04B3H		GAFLID9HH			
F04B4H	Global acceptance filter list mask register 9 L	GAFLM9LL	GAFLM9L	0000H	8, 16
F04B5H		GAFLM9LH			
F04B6H	Global acceptance filter list mask register 9 H	GAFLM9HL	GAFLM9H	0000H	8, 16
F04B7H		GAFLM9HH			
F04B8H	Global acceptance filter list pointer 0 register 9 L	GAFLP09LL	GAFLP09L	0000H	8, 16
F04B9H		GAFLP09LH			
F04BAH	Global acceptance filter list pointer 0 register 9 H	GAFLP09HL	GAFLP09H	0000H	8, 16
F04BBH		GAFLP09HH			
F04BCH	Global acceptance filter list pointer 1 register 9 L	GAFLP19LL	GAFLP19L	0000H	8, 16
F04BDH		GAFLP19LH			
F04C0H	Global acceptance filter list ID register 10 L	GAFLID10LL	GAFLID10L	0000H	8, 16
F04C1H		GAFLID10LH			
F04C2H	Global acceptance filter list ID register 10 H	GAFLID10HL	GAFLID10H	0000H	8, 16
F04C3H		GAFLID10HH			
F04C4H	Global acceptance filter list mask register 10 L	GAFLM10LL	GAFLM10L	0000H	8, 16
F04C5H		GAFLM10LH			
F04C6H	Global acceptance filter list mask register 10 H	GAFLM10HL	GAFLM10H	0000H	8, 16
F04C7H		GAFLM10HH			
F04C8H	Global acceptance filter list pointer 0 register 10 L	GAFLP010LL	GAFLP010L	0000H	8, 16
F04C9H		GAFLP010LH			
F04CAH	Global acceptance filter list pointer 0 register 10 H	GAFLP010HL	GAFLP010H	0000H	8, 16
F04CBH		GAFLP010HH			
F04CCH	Global acceptance filter list pointer 1 register 10 L	GAFLP110LL	GAFLP110L	0000H	8, 16
F04CDH		GAFLP110LH			
F04D0H	Global acceptance filter list ID register 11 L	GAFLID11LL	GAFLID11L	0000H	8, 16
F04D1H		GAFLID11LH			
F04D2H	Global acceptance filter list ID register 11 H	GAFLID11HL	GAFLID11H	0000H	8, 16
F04D3H		GAFLID11HH			
F04D4H	Global acceptance filter list mask register 11 L	GAFLM11LL	GAFLM11L	0000H	8, 16
F04D5H		GAFLM11LH			
F04D6H	Global acceptance filter list mask register 11 H	GAFLM11HL	GAFLM11H	0000H	8, 16
F04D7H		GAFLM11HH			
F04D8H	Global acceptance filter list pointer 0 register 11 L	GAFLP011LL	GAFLP011L	0000H	8, 16
F04D9H		GAFLP011LH			
F04DAH	Global acceptance filter list pointer 0 register 11 H	GAFLP011HL	GAFLP011H	0000H	8, 16
F04DBH		GAFLP011HH			
F04DCH	Global acceptance filter list pointer 1 register 11 L	GAFLP111LL	GAFLP111L	0000H	8, 16
F04DDH		GAFLP111LH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (5/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04E0H	Global acceptance filter list ID register 12 L	GAFLID12LL	GAFLID12L	0000H	8, 16
F04E1H		GAFLID12LH			
F04E2H	Global acceptance filter list ID register 12 H	GAFLID12HL	GAFLID12H	0000H	8, 16
F04E3H		GAFLID12HH			
F04E4H	Global acceptance filter list mask register 12 L	GAFLM12LL	GAFLM12L	0000H	8, 16
F04E5H		GAFLM12LH			
F04E6H	Global acceptance filter list mask register 12 H	GAFLM12HL	GAFLM12H	0000H	8, 16
F04E7H		GAFLM12HH			
F04E8H	Global acceptance filter list pointer 0 register 12 L	GAFLP012LL	GAFLP012L	0000H	8, 16
F04E9H		GAFLP012LH			
F04EAH	Global acceptance filter list pointer 0 register 12 H	GAFLP012HL	GAFLP012H	0000H	8, 16
F04EBH		GAFLP012HH			
F04ECH	Global acceptance filter list pointer 1 register 12 L	GAFLP112LL	GAFLP112L	0000H	8, 16
F04EDH		GAFLP112LH			
F04F0H	Global acceptance filter list ID register 13 L	GAFLID13LL	GAFLID13L	0000H	8, 16
F04F1H		GAFLID13LH			
F04F2H	Global acceptance filter list ID register 13 H	GAFLID13HL	GAFLID13H	0000H	8, 16
F04F3H		GAFLID13HH			
F04F4H	Global acceptance filter list mask register 13 L	GAFLM13LL	GAFLM13L	0000H	8, 16
F04F5H		GAFLM13LH			
F04F6H	Global acceptance filter list mask register 13 H	GAFLM13HL	GAFLM13H	0000H	8, 16
F04F7H		GAFLM13HH			
F04F8H	Global acceptance filter list pointer 0 register 13 L	GAFLP013LL	GAFLP013L	0000H	8, 16
F04F9H		GAFLP013LH			
F04FAH	Global acceptance filter list pointer 0 register 13 H	GAFLP013HL	GAFLP013H	0000H	8, 16
F04FBH		GAFLP013HH			
F04FCH	Global acceptance filter list pointer 1 register 13 L	GAFLP113LL	GAFLP113L	0000H	8, 16
F04FDH		GAFLP113LH			
F0500H	Global acceptance filter list ID register 14 L	GAFLID14LL	GAFLID14L	0000H	8, 16
F0501H		GAFLID14LH			
F0502H	Global acceptance filter list ID register 14 H	GAFLID14HL	GAFLID14H	0000H	8, 16
F0503H		GAFLID14HH			
F0504H	Global acceptance filter list mask register 14 L	GAFLM14LL	GAFLM14L	0000H	8, 16
F0505H		GAFLM14LH			
F0506H	Global acceptance filter list mask register 14 H	GAFLM14HL	GAFLM14H	0000H	8, 16
F0507H		GAFLM14HH			
F0508H	Global acceptance filter list pointer 0 register 14 L	GAFLP014LL	GAFLP014L	0000H	8, 16
F0509H		GAFLP014LH			
F050AH	Global acceptance filter list pointer 0 register 14 H	GAFLP014HL	GAFLP014H	0000H	8, 16
F050BH		GAFLP014HH			
F050CH	Global acceptance filter list pointer 1 register 14 L	GAFLP114LL	GAFLP114L	0000H	8, 16
F050DH		GAFLP114LH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (6/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0510H	Global acceptance filter list ID register 15 L	GAFLID15LL	GAFLID15L	0000H	8, 16
F0511H		GAFLID15LH			
F0512H	Global acceptance filter list ID register 15 H	GAFLID15HL	GAFLID15H	0000H	8, 16
F0513H		GAFLID15HH			
F0514H	Global acceptance filter list mask register 15 L	GAFLM15LL	GAFLM15L	0000H	8, 16
F0515H		GAFLM15LH			
F0516H	Global acceptance filter list mask register 15 H	GAFLM15HL	GAFLM15H	0000H	8, 16
F0517H		GAFLM15HH			
F0518H	Global acceptance filter list pointer 0 register 15 L	GAFLP015LL	GAFLP015L	0000H	8, 16
F0519H		GAFLP015LH			
F051AH	Global acceptance filter list pointer 0 register 15 H	GAFLP015HL	GAFLP015H	0000H	8, 16
F051BH		GAFLP015HH			
F051CH	Global acceptance filter list pointer 1 register 15 L	GAFLP115LL	GAFLP115L	0000H	8, 16
F051DH		GAFLP115LH			
F0520H	Global pretended network filter list ID register 0 L	GPFLID0LL	GPFLID0L	0000H	8, 16
F0521H		GPFLID0LH			
F0522H	Global pretended network filter list ID register 0 H	GPFLID0HL	GPFLID0H	0000H	8, 16
F0523H		GPFLID0HH			
F0524H	Global pretended network filter list mask register 0 L	GPFLM0LL	GPFLM0L	0000H	8, 16
F0525H		GPFLM0LH			
F0526H	Global pretended network filter list mask register 0 H	GPFLM0HL	GPFLM0H	0000H	8, 16
F0527H		GPFLM0HH			
F0528H	Global pretended network filter list pointer 0 register 0 L	GPFLP00LL	GPFLP00L	0000H	8, 16
F0529H		GPFLP00LH			
F052AH	Global pretended network filter list pointer 0 register 0 H	GPFLP00HL	GPFLP00H	0000H	8, 16
F052BH		GPFLP00HH			
F052CH	Global pretended network filter list pointer 1 register 0 L	GPFLP10LL	GPFLP10L	0000H	8, 16
F052DH		GPFLP10LH			
F0530H	Global pretended network filter list payload type register 0 L	GPFLPT0LL	GPFLPT0L	0000H	8, 16
F0531H		GPFLPT0LH			
F0532H	Global pretended network filter list payload type register 0 H	GPFLPT0HL	GPFLPT0H	0000H	8, 16
F0533H		GPFLPT0HH			
F0534H	Global pretended network filter list payload data 0 register 0 L	GPFLPD00LL	GPFLPD00L	0000H	8, 16
F0535H		GPFLPD00LH			
F0536H	Global pretended network filter list payload data 0 register 0 H	GPFLPD00HL	GPFLPD00H	0000H	8, 16
F0537H		GPFLPD00HH			
F0538H	Global pretended network filter list payload mask 0 register 0 L	GPFLPM00LL	GPFLPM00L	0000H	8, 16
F0539H		GPFLPM00LH			
F053AH	Global pretended network filter list payload mask 0 register 0 H	GPFLPM00HL	GPFLPM00H	0000H	8, 16
F053BH		GPFLPM00HH			
F053CH	Global pretended network filter list payload data 1 register 0 L	GPFLPD10LL	GPFLPD10L	0000H	8, 16
F053DH		GPFLPD10LH			
F053EH	Global pretended network filter list payload data 1 register 0 H	GPFLPD10HL	GPFLPD10H	0000H	8, 16
F053FH		GPFLPD10HH			
F0540H	Global pretended network filter list payload mask 1 register 0 L	GPFLM10LL	GPFLM10L	0000H	8, 16
F0541H		GPFLM10LH			
F0542H	Global pretended network filter list payload mask 1 register 0 H	GPFLM10HL	GPFLM10H	0000H	8, 16
F0543H		GPFLM10HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (7/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0544H	Global pretended network filter list ID register 1 L	GPFLID1LL	GPFLID1L	0000H	8, 16
F0545H		GPFLID1LH			
F0546H	Global pretended network filter list ID register 1 H	GPFLID1HL	GPFLID1H	0000H	8, 16
F0547H		GPFLID1HH			
F0548H	Global pretended network filter list mask register 1 L	GPFLM1LL	GPFLM1L	0000H	8, 16
F0549H		GPFLM1LH			
F054AH	Global pretended network filter list mask register 1 H	GPFLM1HL	GPFLM1H	0000H	8, 16
F054BH		GPFLM1HH			
F054CH	Global pretended network filter list pointer 0 register 1 L	GPFLP01LL	GPFLP01L	0000H	8, 16
F054DH		GPFLP01LH			
F054EH	Global pretended network filter list pointer 0 register 1 H	GPFLP01HL	GPFLP01H	0000H	8, 16
F054FH		GPFLP01HH			
F0550H	Global pretended network filter list pointer 1 register 1 L	GPFLP11LL	GPFLP11L	0000H	8, 16
F0551H		GPFLP11LH			
F0554H	Global pretended network filter list payload type register 1 L	GPFLPT1LL	GPFLPT1L	0000H	8, 16
F0555H		GPFLPT1LH			
F0556H	Global pretended network filter list payload type register 1 H	GPFLPT1HL	GPFLPT1H	0000H	8, 16
F0557H		GPFLPT1HH			
F0558H	Global pretended network filter list payload data 0 register 1 L	GPFLPD01LL	GPFLPD01L	0000H	8, 16
F0559H		GPFLPD01LH			
F055AH	Global pretended network filter list payload data 0 register 1 H	GPFLPD01HL	GPFLPD01H	0000H	8, 16
F055BH		GPFLPD01HH			
F055CH	Global pretended network filter list payload mask 0 register 1 L	GPFLPM01LL	GPFLPM01L	0000H	8, 16
F055DH		GPFLPM01LH			
F055EH	Global pretended network filter list payload mask 0 register 1 H	GPFLPM01HL	GPFLPM01H	0000H	8, 16
F055FH		GPFLPM01HH			
F0560H	Global pretended network filter list payload data 1 register 1 L	GPFLPD11LL	GPFLPD11L	0000H	8, 16
F0561H		GPFLPD11LH			
F0562H	Global pretended network filter list payload data 1 register 1 H	GPFLPD11HL	GPFLPD11H	0000H	8, 16
F0563H		GPFLPD11HH			
F0564H	Global pretended network filter list payload mask 1 register 1 L	GPFLM11LL	GPFLM11L	0000H	8, 16
F0565H		GPFLM11LH			
F0566H	Global pretended network filter list payload mask 1 register 1 H	GPFLM11HL	GPFLM11H	0000H	8, 16
F0567H		GPFLM11HH			
F0580H	RAM test page access register 0 L	RPGACC0LL	RPGACC0L	0000H	8, 16
F0581H		RPGACC0LH			
F0582H	RAM test page access register 0 H	RPGACC0HL	RPGACC0H	0000H	8, 16
F0583H		RPGACC0HH			
F0584H	RAM test page access register 1 L	RPGACC1LL	RPGACC1L	0000H	8, 16
F0585H		RPGACC1LH			
F0586H	RAM test page access register 1 H	RPGACC1HL	RPGACC1H	0000H	8, 16
F0587H		RPGACC1HH			
F0588H	RAM test page access register 2 L	RPGACC2LL	RPGACC2L	0000H	8, 16
F0589H		RPGACC2LH			
F058AH	RAM test page access register 2 H	RPGACC2HL	RPGACC2H	0000H	8, 16
F058BH		RPGACC2HH			
F058CH	RAM test page access register 3 L	RPGACC3LL	RPGACC3L	0000H	8, 16
F058DH		RPGACC3LH			
F058EH	RAM test page access register 3 H	RPGACC3HL	RPGACC3H	0000H	8, 16
F058FH		RPGACC3HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (8/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0590H	RAM test page access register 4 L	RPGACC4LL	RPGACC4L	0000H	8, 16
F0591H		RPGACC4LH			
F0592H	RAM test page access register 4 H	RPGACC4HL	RPGACC4H	0000H	8, 16
F0593H		RPGACC4HH			
F0594H	RAM test page access register 5 L	RPGACC5LL	RPGACC5L	0000H	8, 16
F0595H		RPGACC5LH			
F0596H	RAM test page access register 5 H	RPGACC5HL	RPGACC5H	0000H	8, 16
F0597H		RPGACC5HH			
F0598H	RAM test page access register 6 L	RPGACC6LL	RPGACC6L	0000H	8, 16
F0599H		RPGACC6LH			
F059AH	RAM test page access register 6 H	RPGACC6HL	RPGACC6H	0000H	8, 16
F059BH		RPGACC6HH			
F059CH	RAM test page access register 7 L	RPGACC7LL	RPGACC7L	0000H	8, 16
F059DH		RPGACC7LH			
F059EH	RAM test page access register 7 H	RPGACC7HL	RPGACC7H	0000H	8, 16
F059FH		RPGACC7HH			
F05A0H	RAM test page access register 8 L	RPGACC8LL	RPGACC8L	0000H	8, 16
F05A1H		RPGACC8LH			
F05A2H	RAM test page access register 8 H	RPGACC8HL	RPGACC8H	0000H	8, 16
F05A3H		RPGACC8HH			
F05A4H	RAM test page access register 9 L	RPGACC9LL	RPGACC9L	0000H	8, 16
F05A5H		RPGACC9LH			
F05A6H	RAM test page access register 9 H	RPGACC9HL	RPGACC9H	0000H	8, 16
F05A7H		RPGACC9HH			
F05A8H	RAM test page access register 10 L	RPGACC10LL	RPGACC10L	0000H	8, 16
F05A9H		RPGACC10LH			
F05AAH	RAM test page access register 10 H	RPGACC10HL	RPGACC10H	0000H	8, 16
F05ABH		RPGACC10HH			
F05ACH	RAM test page access register 11 L	RPGACC11LL	RPGACC11L	0000H	8, 16
F05ADH		RPGACC11LH			
F05AEH	RAM test page access register 11 H	RPGACC11HL	RPGACC11H	0000H	8, 16
F05AFH		RPGACC11HH			
F05B0H	RAM test page access register 12 L	RPGACC12LL	RPGACC12L	0000H	8, 16
F05B1H		RPGACC12LH			
F05B2H	RAM test page access register 12 H	RPGACC12HL	RPGACC12H	0000H	8, 16
F05B3H		RPGACC12HH			
F05B4H	RAM test page access register 13 L	RPGACC13LL	RPGACC13L	0000H	8, 16
F05B5H		RPGACC13LH			
F05B6H	RAM test page access register 13 H	RPGACC13HL	RPGACC13H	0000H	8, 16
F05B7H		RPGACC13HH			
F05B8H	RAM test page access register 14 L	RPGACC14LL	RPGACC14L	0000H	8, 16
F05B9H		RPGACC14LH			
F05BAH	RAM test page access register 14 H	RPGACC14HL	RPGACC14H	0000H	8, 16
F05BBH		RPGACC14HH			
F05BCH	RAM test page access register 15 L	RPGACC15LL	RPGACC15L	0000H	8, 16
F05BDH		RPGACC15LH			
F05BEH	RAM test page access register 15 H	RPGACC15HL	RPGACC15H	0000H	8, 16
F05BFH		RPGACC15HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (9/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05C0H	RAM test page access register 16 L	RPGACC16LL	RPGACC16L	0000H	8, 16
F05C1H		RPGACC16LH			
F05C2H	RAM test page access register 16 H	RPGACC16HL	RPGACC16H	0000H	8, 16
F05C3H		RPGACC16HH			
F05C4H	RAM test page access register 17 L	RPGACC17LL	RPGACC17L	0000H	8, 16
F05C5H		RPGACC17LH			
F05C6H	RAM test page access register 17 H	RPGACC17HL	RPGACC17H	0000H	8, 16
F05C7H		RPGACC17HH			
F05C8H	RAM test page access register 18 L	RPGACC18LL	RPGACC18L	0000H	8, 16
F05C9H		RPGACC18LH			
F05CAH	RAM test page access register 18 H	RPGACC18HL	RPGACC18H	0000H	8, 16
F05CBH		RPGACC18HH			
F05CCH	RAM test page access register 19 L	RPGACC19LL	RPGACC19L	0000H	8, 16
F05CDH		RPGACC19LH			
F05CEH	RAM test page access register 19 H	RPGACC19HL	RPGACC19H	0000H	8, 16
F05CFH		RPGACC19HH			
F05D0H	RAM test page access register 20 L	RPGACC20LL	RPGACC20L	0000H	8, 16
F05D1H		RPGACC20LH			
F05D2H	RAM test page access register 20 H	RPGACC20HL	RPGACC20H	0000H	8, 16
F05D3H		RPGACC20HH			
F05D4H	RAM test page access register 21 L	RPGACC21LL	RPGACC21L	0000H	8, 16
F05D5H		RPGACC21LH			
F05D6H	RAM test page access register 21 H	RPGACC21HL	RPGACC21H	0000H	8, 16
F05D7H		RPGACC21HH			
F05D8H	RAM test page access register 22 L	RPGACC22LL	RPGACC22L	0000H	8, 16
F05D9H		RPGACC22LH			
F05DAH	RAM test page access register 22 H	RPGACC22HL	RPGACC22H	0000H	8, 16
F05DBH		RPGACC22HH			
F05DCH	RAM test page access register 23 L	RPGACC23LL	RPGACC23L	0000H	8, 16
F05DDH		RPGACC23LH			
F05DEH	RAM test page access register 23 H	RPGACC23HL	RPGACC23H	0000H	8, 16
F05DFH		RPGACC23HH			
F05E0H	RAM test page access register 24 L	RPGACC24LL	RPGACC24L	0000H	8, 16
F05E1H		RPGACC24LH			
F05E2H	RAM test page access register 24 H	RPGACC24HL	RPGACC24H	0000H	8, 16
F05E3H		RPGACC24HH			
F05E4H	RAM test page access register 25 L	RPGACC25LL	RPGACC25L	0000H	8, 16
F05E5H		RPGACC25LH			
F05E6H	RAM test page access register 25 H	RPGACC25HL	RPGACC25H	0000H	8, 16
F05E7H		RPGACC25HH			
F05E8H	RAM test page access register 26 L	RPGACC26LL	RPGACC26L	0000H	8, 16
F05E9H		RPGACC26LH			
F05EAH	RAM test page access register 26 H	RPGACC26HL	RPGACC26H	0000H	8, 16
F05EBH		RPGACC26HH			
F05ECH	RAM test page access register 27 L	RPGACC27LL	RPGACC27L	0000H	8, 16
F05EDH		RPGACC27LH			
F05EEH	RAM test page access register 27 H	RPGACC27HL	RPGACC27H	0000H	8, 16
F05EFH		RPGACC27HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (10/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05F0H	RAM test page access register 28 L	RPGACC28LL	RPGACC28L	0000H	8, 16
F05F1H		RPGACC28LH			
F05F2H	RAM test page access register 28 H	RPGACC28HL	RPGACC28H	0000H	8, 16
F05F3H		RPGACC28HH			
F05F4H	RAM test page access register 29 L	RPGACC29LL	RPGACC29L	0000H	8, 16
F05F5H		RPGACC29LH			
F05F6H	RAM test page access register 29 H	RPGACC29HL	RPGACC29H	0000H	8, 16
F05F7H		RPGACC29HH			
F05F8H	RAM test page access register 30 L	RPGACC30LL	RPGACC30L	0000H	8, 16
F05F9H		RPGACC30LH			
F05FAH	RAM test page access register 30 H	RPGACC30HL	RPGACC30H	0000H	8, 16
F05FBH		RPGACC30HH			
F05FCH	RAM test page access register 31 L	RPGACC31LL	RPGACC31L	0000H	8, 16
F05FDH		RPGACC31LH			
F05FEH	RAM test page access register 31 H	RPGACC31HL	RPGACC31H	0000H	8, 16
F05FFH		RPGACC31HH			
F0600H	RAM test page access register 32 L	RPGACC32LL	RPGACC32L	0000H	8, 16
F0601H		RPGACC32LH			
F0602H	RAM test page access register 32 H	RPGACC32HL	RPGACC32H	0000H	8, 16
F0603H		RPGACC32HH			
F0604H	RAM test page access register 33 L	RPGACC33LL	RPGACC33L	0000H	8, 16
F0605H		RPGACC33LH			
F0606H	RAM test page access register 33 H	RPGACC33HL	RPGACC33H	0000H	8, 16
F0607H		RPGACC33HH			
F0608H	RAM test page access register 34 L	RPGACC34LL	RPGACC34L	0000H	8, 16
F0609H		RPGACC34LH			
F060AH	RAM test page access register 34 H	RPGACC34HL	RPGACC34H	0000H	8, 16
F060BH		RPGACC34HH			
F060CH	RAM test page access register 35 L	RPGACC35LL	RPGACC35L	0000H	8, 16
F060DH		RPGACC35LH			
F060EH	RAM test page access register 35 H	RPGACC35HL	RPGACC35H	0000H	8, 16
F060FH		RPGACC35HH			
F0610H	RAM test page access register 36 L	RPGACC36LL	RPGACC36L	0000H	8, 16
F0611H		RPGACC36LH			
F0612H	RAM test page access register 36 H	RPGACC36HL	RPGACC36H	0000H	8, 16
F0613H		RPGACC36HH			
F0614H	RAM test page access register 37 L	RPGACC37LL	RPGACC37L	0000H	8, 16
F0615H		RPGACC37LH			
F0616H	RAM test page access register 37 H	RPGACC37HL	RPGACC37H	0000H	8, 16
F0617H		RPGACC37HH			
F0618H	RAM test page access register 38 L	RPGACC38LL	RPGACC38L	0000H	8, 16
F0619H		RPGACC38LH			
F061AH	RAM test page access register 38 H	RPGACC38HL	RPGACC38H	0000H	8, 16
F061BH		RPGACC38HH			
F061CH	RAM test page access register 39 L	RPGACC39LL	RPGACC39L	0000H	8, 16
F061DH		RPGACC39LH			
F061EH	RAM test page access register 39 H	RPGACC39HL	RPGACC39H	0000H	8, 16
F061FH		RPGACC39HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (11/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0620H	RAM test page access register 40 L	RPGACC40LL	RPGACC40L	0000H	8, 16
F0621H		RPGACC40LH			
F0622H	RAM test page access register 40 H	RPGACC40HL	RPGACC40H	0000H	8, 16
F0623H		RPGACC40HH			
F0624H	RAM test page access register 41 L	RPGACC41LL	RPGACC41L	0000H	8, 16
F0625H		RPGACC41LH			
F0626H	RAM test page access register 41 H	RPGACC41HL	RPGACC41H	0000H	8, 16
F0627H		RPGACC41HH			
F0628H	RAM test page access register 42 L	RPGACC42LL	RPGACC42L	0000H	8, 16
F0629H		RPGACC42LH			
F062AH	RAM test page access register 42 H	RPGACC42HL	RPGACC42H	0000H	8, 16
F062BH		RPGACC42HH			
F062CH	RAM test page access register 43 L	RPGACC43LL	RPGACC43L	0000H	8, 16
F062DH		RPGACC43LH			
F062EH	RAM test page access register 43 H	RPGACC43HL	RPGACC43H	0000H	8, 16
F062FH		RPGACC43HH			
F0630H	RAM test page access register 44 L	RPGACC44LL	RPGACC44L	0000H	8, 16
F0631H		RPGACC44LH			
F0632H	RAM test page access register 44 H	RPGACC44HL	RPGACC44H	0000H	8, 16
F0633H		RPGACC44HH			
F0634H	RAM test page access register 45 L	RPGACC45LL	RPGACC45L	0000H	8, 16
F0635H		RPGACC45LH			
F0636H	RAM test page access register 45 H	RPGACC45HL	RPGACC45H	0000H	8, 16
F0637H		RPGACC45HH			
F0638H	RAM test page access register 46 L	RPGACC46LL	RPGACC46L	0000H	8, 16
F0639H		RPGACC46LH			
F063AH	RAM test page access register 46 H	RPGACC46HL	RPGACC46H	0000H	8, 16
F063BH		RPGACC46HH			
F063CH	RAM test page access register 47 L	RPGACC47LL	RPGACC47L	0000H	8, 16
F063DH		RPGACC47LH			
F063EH	RAM test page access register 47 H	RPGACC47HL	RPGACC47H	0000H	8, 16
F063FH		RPGACC47HH			
F0640H	RAM test page access register 48 L	RPGACC48LL	RPGACC48L	0000H	8, 16
F0641H		RPGACC48LH			
F0642H	RAM test page access register 48 H	RPGACC48HL	RPGACC48H	0000H	8, 16
F0643H		RPGACC48HH			
F0644H	RAM test page access register 49 L	RPGACC49LL	RPGACC49L	0000H	8, 16
F0645H		RPGACC49LH			
F0646H	RAM test page access register 49 H	RPGACC49HL	RPGACC49H	0000H	8, 16
F0647H		RPGACC49HH			
F0648H	RAM test page access register 50 L	RPGACC50LL	RPGACC50L	0000H	8, 16
F0649H		RPGACC50LH			
F064AH	RAM test page access register 50 H	RPGACC50HL	RPGACC50H	0000H	8, 16
F064BH		RPGACC50HH			
F064CH	RAM test page access register 51 L	RPGACC51LL	RPGACC51L	0000H	8, 16
F064DH		RPGACC51LH			
F064EH	RAM test page access register 51 H	RPGACC51HL	RPGACC51H	0000H	8, 16
F064FH		RPGACC51HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-1. List of RS-CANFD lite Window Registers for RL78/F24 (Page.0) (12/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0650H	RAM test page access register 52 L	RPGACC52LL	RPGACC52L	0000H	8, 16
F0651H		RPGACC52LH			
F0652H	RAM test page access register 52 H	RPGACC52HL	RPGACC52H	0000H	8, 16
F0653H		RPGACC52HH			
F0654H	RAM test page access register 53 L	RPGACC53LL	RPGACC53L	0000H	8, 16
F0655H		RPGACC53LH			
F0656H	RAM test page access register 53 H	RPGACC53HL	RPGACC53H	0000H	8, 16
F0657H		RPGACC53HH			
F0658H	RAM test page access register 54 L	RPGACC54LL	RPGACC54L	0000H	8, 16
F0659H		RPGACC54LH			
F065AH	RAM test page access register 54 H	RPGACC54HL	RPGACC54H	0000H	8, 16
F065BH		RPGACC54HH			
F065CH	RAM test page access register 55 L	RPGACC55LL	RPGACC55L	0000H	8, 16
F065DH		RPGACC55LH			
F065EH	RAM test page access register 55 H	RPGACC55HL	RPGACC55H	0000H	8, 16
F065FH		RPGACC55HH			
F0660H	RAM test page access register 56 L	RPGACC56LL	RPGACC56L	0000H	8, 16
F0661H		RPGACC56LH			
F0662H	RAM test page access register 56 H	RPGACC56HL	RPGACC56H	0000H	8, 16
F0663H		RPGACC56HH			
F0664H	RAM test page access register 57 L	RPGACC57LL	RPGACC57L	0000H	8, 16
F0665H		RPGACC57LH			
F0666H	RAM test page access register 57 H	RPGACC57HL	RPGACC57H	0000H	8, 16
F0667H		RPGACC57HH			
F0668H	RAM test page access register 58 L	RPGACC58LL	RPGACC58L	0000H	8, 16
F0669H		RPGACC58LH			
F066AH	RAM test page access register 58 H	RPGACC58HL	RPGACC58H	0000H	8, 16
F066BH		RPGACC58HH			
F066CH	RAM test page access register 59 L	RPGACC59LL	RPGACC59L	0000H	8, 16
F066DH		RPGACC59LH			
F066EH	RAM test page access register 59 H	RPGACC59HL	RPGACC59H	0000H	8, 16
F066FH		RPGACC59HH			
F0670H	RAM test page access register 60 L	RPGACC60LL	RPGACC60L	0000H	8, 16
F0671H		RPGACC60LH			
F0672H	RAM test page access register 60 H	RPGACC60HL	RPGACC60H	0000H	8, 16
F0673H		RPGACC60HH			
F0674H	RAM test page access register 61 L	RPGACC61LL	RPGACC61L	0000H	8, 16
F0675H		RPGACC61LH			
F0676H	RAM test page access register 61 H	RPGACC61HL	RPGACC61H	0000H	8, 16
F0677H		RPGACC61HH			
F0678H	RAM test page access register 62 L	RPGACC62LL	RPGACC62L	0000H	8, 16
F0679H		RPGACC62LH			
F067AH	RAM test page access register 62 H	RPGACC62HL	RPGACC62H	0000H	8, 16
F067BH		RPGACC62HH			
F067CH	RAM test page access register 63 L	RPGACC63LL	RPGACC63L	0000H	8, 16
F067DH		RPGACC63LH			
F067EH	RAM test page access register 63 H	RPGACC63HL	RPGACC63H	0000H	8, 16
F067FH		RPGACC63HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 00B (page.0 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (1/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0420H	RX FIFO access ID register 0 L	RFID0LL	RFID0L	0000H	8, 16
F0421H		RFID0LH			
F0422H	RX FIFO access ID register 0 H	RFID0HL	RFID0H	0000H	8, 16
F0423H		RFID0HH			
F0424H	RX FIFO access pointer register 0 L	RFPTR0LL	RFPTR0L	0000H	8, 16
F0425H		RFPTR0LH			
F0426H	RX FIFO access pointer register 0 H	—	RFPTR0H	0000H	8, 16
F0427H		RFPTR0HH			
F0428H	RX FIFO access CAN-FD status register 0 L	RFFDSTS0LL	RFFDSTS0L	0000H	8, 16
F0429H		RFFDSTS0LH			
F042AH	RX FIFO access CAN-FD status register 0 H	RFFDSTS0HL	RFFDSTS0H	0000H	8, 16
F042BH		RFFDSTS0HH			
F042CH	RX FIFO access data field 0 register 0 L	RFDF0_0LL	RFDF0_0L	0000H	8, 16
F042DH		RFDF0_0LH			
F042EH	RX FIFO access data field 0 register 0 H	RFDF0_0HL	RFDF0_0H	0000H	8, 16
F042FH		RFDF0_0HH			
F0430H	RX FIFO access data field 1 register 0 L	RFDF0_1LL	RFDF0_1L	0000H	8, 16
F0431H		RFDF0_1LH			
F0432H	RX FIFO access data field 1 register 0 H	RFDF0_1HL	RFDF0_1H	0000H	8, 16
F0433H		RFDF0_1HH			
F0434H	RX FIFO access data field 2 register 0 L	RFDF0_2LL	RFDF0_2L	0000H	8, 16
F0435H		RFDF0_2LH			
F0436H	RX FIFO access data field 2 register 0 H	RFDF0_2HL	RFDF0_2H	0000H	8, 16
F0437H		RFDF0_2HH			
F0438H	RX FIFO access data field 3 register 0 L	RFDF0_3LL	RFDF0_3L	0000H	8, 16
F0439H		RFDF0_3LH			
F043AH	RX FIFO access data field 3 register 0 H	RFDF0_3HL	RFDF0_3H	0000H	8, 16
F043BH		RFDF0_3HH			
F043CH	RX FIFO access data field 4 register 0 L	RFDF0_4LL	RFDF0_4L	0000H	8, 16
F043DH		RFDF0_4LH			
F043EH	RX FIFO access data field 4 register 0 H	RFDF0_4HL	RFDF0_4H	0000H	8, 16
F043FH		RFDF0_4HH			
F0440H	RX FIFO access data field 5 register 0 L	RFDF0_5LL	RFDF0_5L	0000H	8, 16
F0441H		RFDF0_5LH			
F0442H	RX FIFO access data field 5 register 0 H	RFDF0_5HL	RFDF0_5H	0000H	8, 16
F0443H		RFDF0_5HH			
F0444H	RX FIFO access data field 6 register 0 L	RFDF0_6LL	RFDF0_6L	0000H	8, 16
F0445H		RFDF0_6LH			
F0446H	RX FIFO access data field 6 register 0 H	RFDF0_6HL	RFDF0_6H	0000H	8, 16
F0447H		RFDF0_6HH			
F0448H	RX FIFO access data field 7 register 0 L	RFDF0_7LL	RFDF0_7L	0000H	8, 16
F0449H		RFDF0_7LH			
F044AH	RX FIFO access data field 7 register 0 H	RFDF0_7HL	RFDF0_7H	0000H	8, 16
F044BH		RFDF0_7HH			
F044CH	RX FIFO access data field 8 register 0 L	RFDF0_8LL	RFDF0_8L	0000H	8, 16
F044DH		RFDF0_8LH			
F044EH	RX FIFO access data field 8 register 0 H	RFDF0_8HL	RFDF0_8H	0000H	8, 16
F044FH		RFDF0_8HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (2/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0450H	RX FIFO access data field 9 register 0 L	RFDF0_9LL	RFDF0_9L	0000H	8, 16
F0451H		RFDF0_9LH			
F0452H	RX FIFO access data field 9 register 0 H	RFDF0_9HL	RFDF0_9H	0000H	8, 16
F0453H		RFDF0_9HH			
F0454H	RX FIFO access data field 10 register 0 L	RFDF0_10LL	RFDF0_10L	0000H	8, 16
F0455H		RFDF0_10LH			
F0456H	RX FIFO access data field 10 register 0 H	RFDF0_10HL	RFDF0_10H	0000H	8, 16
F0457H		RFDF0_10HH			
F0458H	RX FIFO access data field 11 register 0 L	RFDF0_11LL	RFDF0_11L	0000H	8, 16
F0459H		RFDF0_11LH			
F045AH	RX FIFO access data field 11 register 0 H	RFDF0_11HL	RFDF0_11H	0000H	8, 16
F045BH		RFDF0_11HH			
F045CH	RX FIFO access data field 12 register 0 L	RFDF0_12LL	RFDF0_12L	0000H	8, 16
F045DH		RFDF0_12LH			
F045EH	RX FIFO access data field 12 register 0 H	RFDF0_12HL	RFDF0_12H	0000H	8, 16
F045FH		RFDF0_12HH			
F0460H	RX FIFO access data field 13 register 0 L	RFDF0_13LL	RFDF0_13L	0000H	8, 16
F0461H		RFDF0_13LH			
F0462H	RX FIFO access data field 13 register 0 H	RFDF0_13HL	RFDF0_13H	0000H	8, 16
F0463H		RFDF0_13HH			
F0464H	RX FIFO access data field 14 register 0 L	RFDF0_14LL	RFDF0_14L	0000H	8, 16
F0465H		RFDF0_14LH			
F0466H	RX FIFO access data field 14 register 0 H	RFDF0_14HL	RFDF0_14H	0000H	8, 16
F0467H		RFDF0_14HH			
F0468H	RX FIFO access data field 15 register 0 L	RFDF0_15LL	RFDF0_15L	0000H	8, 16
F0469H		RFDF0_15LH			
F046AH	RX FIFO access data field 15 register 0 H	RFDF0_15HL	RFDF0_15H	0000H	8, 16
F046BH		RFDF0_15HH			
F046CH	RX FIFO access ID register 1 L	RFID1LL	RFID1L	0000H	8, 16
F046DH		RFID1LH			
F046EH	RX FIFO access ID register 1 H	RFID1HL	RFID1H	0000H	8, 16
F046FH		RFID1HH			
F0470H	RX FIFO access pointer register 1 L	RFPTR1LL	RFPTR1L	0000H	8, 16
F0471H		RFPTR1LH			
F0472H	RX FIFO access pointer register 1 H	—	RFPTR1H	0000H	8, 16
F0473H		RFPTR1HH			
F0474H	RX FIFO access CAN-FD status register 1 L	RFFDSTS1LL	RFFDSTS1L	0000H	8, 16
F0475H		RFFDSTS1LH			
F0476H	RX FIFO access CAN-FD status register 1 H	RFFDSTS1HL	RFFDSTS1H	0000H	8, 16
F0477H		RFFDSTS1H			
F0478H	RX FIFO access data field 0 register 1 L	RFDF1_0LL	RFDF1_0L	0000H	8, 16
F0479H		RFDF1_0LH			
F047AH	RX FIFO access data field 0 register 1 H	RFDF1_0HL	RFDF1_0H	0000H	8, 16
F047BH		RFDF1_0HH			
F047CH	RX FIFO access data field 1 register 1 L	RFDF1_1LL	RFDF1_1L	0000H	8, 16
F047DH		RFDF1_1LH			
F047EH	RX FIFO access data field 1 register 1 H	RFDF1_1HL	RFDF1_1H	0000H	8, 16
F047FH		RFDF1_1HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (3/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0480H	RX FIFO access data field 2 register 1 L	RFDF1_2LL	RFDF1_2L	0000H	8, 16
F0481H		RFDF1_2LH			
F0482H	RX FIFO access data field 2 register 1 H	RFDF1_2HL	RFDF1_2H	0000H	8, 16
F0483H		RFDF1_2HH			
F0484H	RX FIFO access data field 3 register 1 L	RFDF1_3LL	RFDF1_3L	0000H	8, 16
F0485H		RFDF1_3LH			
F0486H	RX FIFO access data field 3 register 1 H	RFDF1_3HL	RFDF1_3H	0000H	8, 16
F0487H		RFDF1_3HH			
F0488H	RX FIFO access data field 4 register 1 L	RFDF1_4LL	RFDF1_4L	0000H	8, 16
F0489H		RFDF1_4LH			
F048AH	RX FIFO access data field 4 register 1 H	RFDF1_4HL	RFDF1_4H	0000H	8, 16
F048BH		RFDF1_4HH			
F048CH	RX FIFO access data field 5 register 1 L	RFDF1_5LL	RFDF1_5L	0000H	8, 16
F048DH		RFDF1_5LH			
F048EH	RX FIFO access data field 5 register 1 H	RFDF1_5HL	RFDF1_5H	0000H	8, 16
F048FH		RFDF1_5HH			
F0490H	RX FIFO access data field 6 register 1 L	RFDF1_6LL	RFDF1_6L	0000H	8, 16
F0491H		RFDF1_6LH			
F0492H	RX FIFO access data field 6 register 1 H	RFDF1_6HL	RFDF1_6H	0000H	8, 16
F0493H		RFDF1_6HH			
F0494H	RX FIFO access data field 7 register 1 L	RFDF1_7LL	RFDF1_7L	0000H	8, 16
F0495H		RFDF1_7LH			
F0496H	RX FIFO access data field 7 register 1 H	RFDF1_7HL	RFDF1_7H	0000H	8, 16
F0497H		RFDF1_7HH			
F0498H	RX FIFO access data field 8 register 1 L	RFDF1_8LL	RFDF1_8L	0000H	8, 16
F0499H		RFDF1_8LH			
F049AH	RX FIFO access data field 8 register 1 H	RFDF1_8HL	RFDF1_8H	0000H	8, 16
F049BH		RFDF1_8HH			
F049CH	RX FIFO access data field 9 register 1 L	RFDF1_9LL	RFDF1_9L	0000H	8, 16
F049DH		RFDF1_9LH			
F049EH	RX FIFO access data field 9 register 1 H	RFDF1_9HL	RFDF1_9H	0000H	8, 16
F049FH		RFDF1_9HH			
F04A0H	RX FIFO access data field 10 register 1 L	RFDF1_10LL	RFDF1_10L	0000H	8, 16
F04A1H		RFDF1_10LH			
F04A2H	RX FIFO access data field 10 register 1 H	RFDF1_10HL	RFDF1_10H	0000H	8, 16
F04A3H		RFDF1_10HH			
F04A4H	RX FIFO access data field 11 register 1 L	RFDF1_11LL	RFDF1_11L	0000H	8, 16
F04A5H		RFDF1_11LH			
F04A6H	RX FIFO access data field 11 register 1 H	RFDF1_11HL	RFDF1_11H	0000H	8, 16
F04A7H		RFDF1_11HH			
F04A8H	RX FIFO access data field 12 register 1 L	RFDF1_12LL	RFDF1_12L	0000H	8, 16
F04A9H		RFDF1_12LH			
F04AAH	RX FIFO access data field 12 register 1 H	RFDF1_12HL	RFDF1_12H	0000H	8, 16
F04ABH		RFDF1_12HH			
F04ACH	RX FIFO access data field 13 register 1 L	RFDF1_13LL	RFDF1_13L	0000H	8, 16
F04ADH		RFDF1_13LH			
F04AEH	RX FIFO access data field 13 register 1 H	RFDF1_13HL	RFDF1_13H	0000H	8, 16
F04AFH		RFDF1_13HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (4/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04B0H	RX FIFO access data field 14 register 1 L	RFDF1_14LL	RFDF1_14L	0000H	8, 16
F04B1H		RFDF1_14LH			
F04B2H	RX FIFO access data field 14 register 1 H	RFDF1_14HL	RFDF1_14H	0000H	8, 16
F04B3H		RFDF1_14HH			
F04B4H	RX FIFO access data field 15 register 1 L	RFDF1_15LL	RFDF1_15L	0000H	8, 16
F04B5H		RFDF1_15LH			
F04B6H	RX FIFO access data field 15 register 1 H	RFDF1_15HL	RFDF1_15H	0000H	8, 16
F04B7H		RFDF1_15HH			
F04B8H	Common FIFO access ID register L	CFIDLL	CFIDL	0000H	8, 16
F04B9H		CFIDLH			
F04BAH	Common FIFO access ID register H	CFIDHL	CFIDH	0000H	8, 16
F04BBH		CFIDHH			
F04BCH	Common FIFO access pointer register L	CFPTRLL	CFPTRL	0000H	8, 16
F04BDH		CFPTRLH			
F04BEH	Common FIFO access pointer register H	—	CFPTRH	0000H	8, 16
F04BFH		CFPTRHH			
F04C0H	Common FIFO access CAN-FD control / status register L	CFFDCSTSLL	CFFDCSTSL	0000H	8, 16
F04C1H		CFFDCSTSLH			
F04C2H	Common FIFO access CAN-FD control / status register H	CFFDCSTSHL	CFFDCSTSH	0000H	8, 16
F04C3H		CFFDCSTSHH			
F04C4H	Common FIFO access data field 0 register L	CFDF0LL	CFDF0L	0000H	8, 16
F04C5H		CFDF0LH			
F04C6H	Common FIFO access data field 0 register H	CFDF0HL	CFDF0H	0000H	8, 16
F04C7H		CFDF0HH			
F04C8H	Common FIFO access data field 1 register L	CFDF1LL	CFDF1L	0000H	8, 16
F04C9H		CFDF1LH			
F04CAH	Common FIFO access data field 1 register H	CFDF1HL	CFDF1H	0000H	8, 16
F04CBH		CFDF1HH			
F04CCH	Common FIFO access data field 2 register L	CFDF2LL	CFDF2L	0000H	8, 16
F04CDH		CFDF2LH			
F04CEH	Common FIFO access data field 2 register H	CFDF2HL	CFDF2H	0000H	8, 16
F04CFH		CFDF2HH			
F04D0H	Common FIFO access data field 3 register L	CFDF3LL	CFDF3L	0000H	8, 16
F04D1H		CFDF3LH			
F04D2H	Common FIFO access data field 3 register H	CFDF3HL	CFDF3H	0000H	8, 16
F04D3H		CFDF3HH			
F04D4H	Common FIFO access data field 4 register L	CFDF4LL	CFDF4L	0000H	8, 16
F04D5H		CFDF4LH			
F04D6H	Common FIFO access data field 4 register H	CFDF4HL	CFDF4H	0000H	8, 16
F04D7H		CFDF4HH			
F04D8H	Common FIFO access data field 5 register L	CFDF5LL	CFDF5L	0000H	8, 16
F04D9H		CFDF5LH			
F04DAH	Common FIFO access data field 5 register H	CFDF5HL	CFDF5H	0000H	8, 16
F04DBH		CFDF5HH			
F04DCH	Common FIFO access data field 6 register L	CFDF6LL	CFDF6L	0000H	8, 16
F04DDH		CFDF6LH			
F04DEH	Common FIFO access data field 6 register H	CFDF6HL	CFDF6H	0000H	8, 16
F04DFH		CFDF6HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (5/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04E0H	Common FIFO access data field 7 register L	CFDF7LL	CFDF7L	0000H	8, 16
F04E1H		CFDF7LH			
F04E2H	Common FIFO access data field 7 register H	CFDF7HL	CFDF7H	0000H	8, 16
F04E3H		CFDF7HH			
F04E4H	Common FIFO access data field 8 register L	CFDF8LL	CFDF8L	0000H	8, 16
F04E5H		CFDF8LH			
F04E6H	Common FIFO access data field 8 register H	CFDF8HL	CFDF8H	0000H	8, 16
F04E7H		CFDF8HH			
F04E8H	Common FIFO access data field 9 register L	CFDF9LL	CFDF9L	0000H	8, 16
F04E9H		CFDF9LH			
F04EAH	Common FIFO access data field 9 register H	CFDF9HL	CFDF9H	0000H	8, 16
F04EBH		CFDF9HH			
F04ECH	Common FIFO access data field 10 register L	CFDF10LL	CFDF10L	0000H	8, 16
F04EDH		CFDF10LH			
F04EEH	Common FIFO access data field 10 register H	CFDF10HL	CFDF10H	0000H	8, 16
F04EFH		CFDF10HH			
F04F0H	Common FIFO access data field 11 register L	CFDF11LL	CFDF11L	0000H	8, 16
F04F1H		CFDF11LH			
F04F2H	Common FIFO access data field 11 register H	CFDF11HL	CFDF11H	0000H	8, 16
F04F3H		CFDF11HH			
F04F4H	Common FIFO access data field 12 register L	CFDF12LL	CFDF12L	0000H	8, 16
F04F5H		CFDF12LH			
F04F6H	Common FIFO access data field 12 register H	CFDF12HL	CFDF12H	0000H	8, 16
F04F7H		CFDF12HH			
F04F8H	Common FIFO access data field 13 register L	CFDF13LL	CFDF13L	0000H	8, 16
F04F9H		CFDF13LH			
F04FAH	Common FIFO access data field 13 register H	CFDF13HL	CFDF13H	0000H	8, 16
F04FBH		CFDF13HH			
F04FCH	Common FIFO access data field 14 register L	CFDF14LL	CFDF14L	0000H	8, 16
F04FDH		CFDF14LH			
F04FEH	Common FIFO access data field 14 register H	CFDF14HL	CFDF14H	0000H	8, 16
F04FFH		CFDF14HH			
F0500H	Common FIFO access data field 15 register L	CFDF15LL	CFDF15L	0000H	8, 16
F0501H		CFDF15LH			
F0502H	Common FIFO access data field 15 register H	CFDF15HL	CFDF15H	0000H	8, 16
F0503H		CFDF15HH			
F0504H	TX message buffer ID register 0 L	TMID0LL	TMID0L	0000H	8, 16
F0505H		TMID0LH			
F0506H	TX message buffer ID register 0 H	TMID0HL	TMID0H	0000H	8, 16
F0507H		TMID0HH			
F050AH	TX message buffer pointer register 0 H	—	TMPTR0H	0000H	8, 16
F050BH		TMPTR0HH			
F050CH	TX message buffer CAN-FD control register 0 L	TMFDCTR0LL	TMFDCTR0L	0000H	8, 16
F050DH		TMFDCTR0LH			
F050EH	TX message buffer CAN-FD control register 0 H	TMFDCTR0HL	TMFDCTR0H	0000H	8, 16
F050FH		TMFDCTR0HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (6/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0510H	TX message buffer data field 0 register 0 L	TMDF0_0LL	TMDF0_0L	0000H	8, 16
F0511H		TMDF0_0LH			
F0512H	TX message buffer data field 0 register 0 H	TMDF0_0HL	TMDF0_0H	0000H	8, 16
F0513H		TMDF0_0HH			
F0514H	TX message buffer data field 1 register 0 L	TMDF0_1LL	TMDF0_1L	0000H	8, 16
F0515H		TMDF0_1LH			
F0516H	TX message buffer data field 1 register 0 H	TMDF0_1HL	TMDF0_1H	0000H	8, 16
F0517H		TMDF0_1HH			
F0518H	TX message buffer data field 2 register 0 L	TMDF0_2LL	TMDF0_2L	0000H	8, 16
F0519H		TMDF0_2LH			
F051AH	TX message buffer data field 2 register 0 H	TMDF0_2HL	TMDF0_2H	0000H	8, 16
F051BH		TMDF0_2HH			
F051CH	TX message buffer data field 3 register 0 L	TMDF0_3LL	TMDF0_3L	0000H	8, 16
F051DH		TMDF0_3LH			
F051EH	TX message buffer data field 3 register 0 H	TMDF0_3HL	TMDF0_3H	0000H	8, 16
F051FH		TMDF0_3HH			
F0520H	TX message buffer data field 4 register 0 L	TMDF0_4LL	TMDF0_4L	0000H	8, 16
F0521H		TMDF0_4LH			
F0522H	TX message buffer data field 4 register 0 H	TMDF0_4HL	TMDF0_4H	0000H	8, 16
F0523H		TMDF0_4HH			
F0524H	TX message buffer data field 5 register 0 L	TMDF0_5LL	TMDF0_5L	0000H	8, 16
F0525H		TMDF0_5LH			
F0526H	TX message buffer data field 5 register 0 H	TMDF0_5HL	TMDF0_5H	0000H	8, 16
F0527H		TMDF0_5HH			
F0528H	TX message buffer data field 6 register 0 L	TMDF0_6LL	TMDF0_6L	0000H	8, 16
F0529H		TMDF0_6LH			
F052AH	TX message buffer data field 6 register 0 H	TMDF0_6HL	TMDF0_6H	0000H	8, 16
F052BH		TMDF0_6HH			
F052CH	TX message buffer data field 7 register 0 L	TMDF0_7LL	TMDF0_7L	0000H	8, 16
F052DH		TMDF0_7LH			
F052EH	TX message buffer data field 7 register 0 H	TMDF0_7HL	TMDF0_7H	0000H	8, 16
F052FH		TMDF0_7HH			
F0530H	TX message buffer data field 8 register 0 L	TMDF0_8LL	TMDF0_8L	0000H	8, 16
F0531H		TMDF0_8LH			
F0532H	TX message buffer data field 8 register 0 H	TMDF0_8HL	TMDF0_8H	0000H	8, 16
F0533H		TMDF0_8HH			
F0534H	TX message buffer data field 9 register 0 L	TMDF0_9LL	TMDF0_9L	0000H	8, 16
F0535H		TMDF0_9LH			
F0536H	TX message buffer data field 9 register 0 H	TMDF0_9HL	TMDF0_9H	0000H	8, 16
F0537H		TMDF0_9HH			
F0538H	TX message buffer data field 10 register 0 L	TMDF0_10LL	TMDF0_10L	0000H	8, 16
F0539H		TMDF0_10LH			
F053AH	TX message buffer data field 10 register 0 H	TMDF0_10HL	TMDF0_10H	0000H	8, 16
F053BH		TMDF0_10HH			
F053CH	TX message buffer data field 11 register 0 L	TMDF0_11LL	TMDF0_11L	0000H	8, 16
F053DH		TMDF0_11LH			
F053EH	TX message buffer data field 11 register 0 H	TMDF0_11HL	TMDF0_11H	0000H	8, 16
F053FH		TMDF0_11HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (7/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0540H	TX message buffer data field 12 register 0 L	TMDF0_12LL	TMDF0_12L	0000H	8, 16
F0541H		TMDF0_12LH			
F0542H	TX message buffer data field 12 register 0 H	TMDF0_12HL	TMDF0_12H	0000H	8, 16
F0543H		TMDF0_12HH			
F0544H	TX message buffer data field 13 register 0 L	TMDF0_13LL	TMDF0_13L	0000H	8, 16
F0545H		TMDF0_13LH			
F0546H	TX message buffer data field 13 register 0 H	TMDF0_13HL	TMDF0_13H	0000H	8, 16
F0547H		TMDF0_13HH			
F0548H	TX message buffer data field 14 register 0 L	TMDF0_14LL	TMDF0_14L	0000H	8, 16
F0549H		TMDF0_14LH			
F054AH	TX message buffer data field 14 register 0 H	TMDF0_14HL	TMDF0_14H	0000H	8, 16
F054BH		TMDF0_14HH			
F054CH	TX message buffer data field 15 register 0 L	TMDF0_15LL	TMDF0_15L	0000H	8, 16
F054DH		TMDF0_15LH			
F054EH	TX message buffer data field 15 register 0 H	TMDF0_15HL	TMDF0_15H	0000H	8, 16
F054FH		TMDF0_15HH			
F0550H	TX message buffer ID register 1 L	TMID1LL	TMID1L	0000H	8, 16
F0551H		TMID1LH			
F0552H	TX message buffer ID register 1 H	TMID1HL	TMID1H	0000H	8, 16
F0553H		TMID1HH			
F0556H	TX message buffer pointer register 1 H	—	TMPTR1H	0000H	8, 16
F0557H		TMPTR1HH			
F0558H	TX message buffer CAN-FD control register 1 L	TMFDCTR1LL	TMFDCTR1L	0000H	8, 16
F0559H		TMFDCTR1LH			
F055AH	TX message buffer CAN-FD control register 1 H	TMFDCTR1HL	TMFDCTR1H	0000H	8, 16
F055BH		TMFDCTR1HH			
F055CH	TX message buffer data field 0 register 1 L	TMDF1_0LL	TMDF1_0L	0000H	8, 16
F055DH		TMDF1_0LH			
F055EH	TX message buffer data field 0 register 1 H	TMDF1_0HL	TMDF1_0H	0000H	8, 16
F055FH		TMDF1_0HH			
F0560H	TX message buffer data field 1 register 1 L	TMDF1_1LL	TMDF1_1L	0000H	8, 16
F0561H		TMDF1_1LH			
F0562H	TX message buffer data field 1 register 1 H	TMDF1_1HL	TMDF1_1H	0000H	8, 16
F0563H		TMDF1_1HH			
F0564H	TX message buffer data field 2 register 1 L	TMDF1_2LL	TMDF1_2L	0000H	8, 16
F0565H		TMDF1_2LH			
F0566H	TX message buffer data field 2 register 1 H	TMDF1_2HL	TMDF1_2H	0000H	8, 16
F0567H		TMDF1_2HH			
F0568H	TX message buffer data field 3 register 1 L	TMDF1_3LL	TMDF1_3L	0000H	8, 16
F0569H		TMDF1_3LH			
F056AH	TX message buffer data field 3 register 1 H	TMDF1_3HL	TMDF1_3H	0000H	8, 16
F056BH		TMDF1_3HH			
F056CH	TX message buffer data field 4 register 1 L	TMDF1_4LL	TMDF1_4L	0000H	8, 16
F056DH		TMDF1_4LH			
F056EH	TX message buffer data field 4 register 1 H	TMDF1_4HL	TMDF1_4H	0000H	8, 16
F056FH		TMDF1_4HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (8/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0570H	TX message buffer data field 5 register 1 L	TMDF1_5LL	TMDF1_5L	0000H	8, 16
F0571H		TMDF1_5LH			
F0572H	TX message buffer data field 5 register 1 H	TMDF1_5HL	TMDF1_5H	0000H	8, 16
F0573H		TMDF1_5HH			
F0574H	TX message buffer data field 6 register 1 L	TMDF1_6LL	TMDF1_6L	0000H	8, 16
F0575H		TMDF1_6LH			
F0576H	TX message buffer data field 6 register 1 H	TMDF1_6HL	TMDF1_6H	0000H	8, 16
F0577H		TMDF1_6HH			
F0578H	TX message buffer data field 7 register 1 L	TMDF1_7LL	TMDF1_7L	0000H	8, 16
F0579H		TMDF1_7LH			
F057AH	TX message buffer data field 7 register 1 H	TMDF1_7HL	TMDF1_7H	0000H	8, 16
F057BH		TMDF1_7HH			
F057CH	TX message buffer data field 8 register 1 L	TMDF1_8LL	TMDF1_8L	0000H	8, 16
F057DH		TMDF1_8LH			
F057EH	TX message buffer data field 8 register 1 H	TMDF1_8HL	TMDF1_8H	0000H	8, 16
F057FH		TMDF1_8HH			
F0580H	TX message buffer data field 9 register 1 L	TMDF1_9LL	TMDF1_9L	0000H	8, 16
F0581H		TMDF1_9LH			
F0582H	TX message buffer data field 9 register 1 H	TMDF1_9HL	TMDF1_9H	0000H	8, 16
F0583H		TMDF1_9HH			
F0584H	TX message buffer data field 10 register 1 L	TMDF1_10LL	TMDF1_10L	0000H	8, 16
F0585H		TMDF1_10LH			
F0586H	TX message buffer data field 10 register 1 H	TMDF1_10HL	TMDF1_10H	0000H	8, 16
F0587H		TMDF1_10HH			
F0588H	TX message buffer data field 11 register 1 L	TMDF1_11LL	TMDF1_11L	0000H	8, 16
F0589H		TMDF1_11LH			
F058AH	TX message buffer data field 11 register 1 H	TMDF1_11HL	TMDF1_11H	0000H	8, 16
F058BH		TMDF1_11HH			
F058CH	TX message buffer data field 12 register 1 L	TMDF1_12LL	TMDF1_12L	0000H	8, 16
F058DH		TMDF1_12LH			
F058EH	TX message buffer data field 12 register 1 H	TMDF1_12HL	TMDF1_12H	0000H	8, 16
F058FH		TMDF1_12HH			
F0590H	TX message buffer data field 13 register 1 L	TMDF1_13LL	TMDF1_13L	0000H	8, 16
F0591H		TMDF1_13LH			
F0592H	TX message buffer data field 13 register 1 H	TMDF1_13HL	TMDF1_13H	0000H	8, 16
F0593H		TMDF1_13HH			
F0594H	TX message buffer data field 14 register 1 L	TMDF1_14LL	TMDF1_14L	0000H	8, 16
F0595H		TMDF1_14LH			
F0596H	TX message buffer data field 14 register 1 H	TMDF1_14HL	TMDF1_14H	0000H	8, 16
F0597H		TMDF1_14HH			
F0598H	TX message buffer data field 15 register 1 L	TMDF1_15LL	TMDF1_15L	0000H	8, 16
F0599H		TMDF1_15LH			
F059AH	TX message buffer data field 15 register 1 H	TMDF1_15HL	TMDF1_15H	0000H	8, 16
F059BH		TMDF1_15HH			
F059CH	TX message buffer ID register 2 L	TMID2LL	TMID2L	0000H	8, 16
F059DH		TMID2LH			
F059EH	TX message buffer ID register 2 H	TMID2HL	TMID2H	0000H	8, 16
F059FH		TMID2HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (9/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05A2H	TX message buffer pointer register 2 H	—	TMPTR2H	0000H	8, 16
F05A3H		TMPTR2HH			
F05A4H	TX message buffer CAN-FD control register 2 L	TMFDCTR2LL	TMFDCTR2L	0000H	8, 16
F05A5H		TMFDCTR2LH			
F05A6H	TX message buffer CAN-FD control register 2 H	TMFDCTR2HL	TMFDCTR2H	0000H	8, 16
F05A7H		TMFDCTR2HH			
F05A8H	TX message buffer data field 0 register 2 L	TMDF2_0LL	TMDF2_0L	0000H	8, 16
F05A9H		TMDF2_0LH			
F05AAH	TX message buffer data field 0 register 2 H	TMDF2_0HL	TMDF2_0H	0000H	8, 16
F05ABH		TMDF2_0HH			
F05ACH	TX message buffer data field 1 register 2 L	TMDF2_1LL	TMDF2_1L	0000H	8, 16
F05ADH		TMDF2_1LH			
F05AEH	TX message buffer data field 1 register 2 H	TMDF2_1HL	TMDF2_1H	0000H	8, 16
F05AFH		TMDF2_1HH			
F05B0H	TX message buffer data field 2 register 2 L	TMDF2_2LL	TMDF2_2L	0000H	8, 16
F05B1H		TMDF2_2LH			
F05B2H	TX message buffer data field 2 register 2 H	TMDF2_2HL	TMDF2_2H	0000H	8, 16
F05B3H		TMDF2_2HH			
F05B4H	TX message buffer data field 3 register 2 L	TMDF2_3LL	TMDF2_3L	0000H	8, 16
F05B5H		TMDF2_3LH			
F05B6H	TX message buffer data field 3 register 2 H	TMDF2_3HL	TMDF2_3H	0000H	8, 16
F05B7H		TMDF2_3HH			
F05B8H	TX message buffer data field 4 register 2 L	TMDF2_4LL	TMDF2_4L	0000H	8, 16
F05B9H		TMDF2_4LH			
F05BAH	TX message buffer data field 4 register 2 H	TMDF2_4HL	TMDF2_4H	0000H	8, 16
F05BBH		TMDF2_4HH			
F05BCH	TX message buffer data field 5 register 2 L	TMDF2_5LL	TMDF2_5L	0000H	8, 16
F05BDH		TMDF2_5LH			
F05BEH	TX message buffer data field 5 register 2 H	TMDF2_5HL	TMDF2_5H	0000H	8, 16
F05BFH		TMDF2_5HH			
F05C0H	TX message buffer data field 6 register 2 L	TMDF2_6LL	TMDF2_6L	0000H	8, 16
F05C1H		TMDF2_6LH			
F05C2H	TX message buffer data field 6 register 2 H	TMDF2_6HL	TMDF2_6H	0000H	8, 16
F05C3H		TMDF2_6HH			
F05C4H	TX message buffer data field 7 register 2 L	TMDF2_7LL	TMDF2_7L	0000H	8, 16
F05C5H		TMDF2_7LH			
F05C6H	TX message buffer data field 7 register 2 H	TMDF2_7HL	TMDF2_7H	0000H	8, 16
F05C7H		TMDF2_7HH			
F05C8H	TX message buffer data field 8 register 2 L	TMDF2_8LL	TMDF2_8L	0000H	8, 16
F05C9H		TMDF2_8LH			
F05CAH	TX message buffer data field 8 register 2 H	TMDF2_8HL	TMDF2_8H	0000H	8, 16
F05CBH		TMDF2_8HH			
F05CCH	TX message buffer data field 9 register 2 L	TMDF2_9LL	TMDF2_9L	0000H	8, 16
F05CDH		TMDF2_9LH			
F05CEH	TX message buffer data field 9 register 2 H	TMDF2_9HL	TMDF2_9H	0000H	8, 16
F05CFH		TMDF2_9HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (10/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05D0H	TX message buffer data field 10 register 2 L	TMDF2_10LL	TMDF2_10L	0000H	8, 16
F05D1H		TMDF2_10LH			
F05D2H	TX message buffer data field 10 register 2 H	TMDF2_10HL	TMDF2_10H	0000H	8, 16
F05D3H		TMDF2_10HH			
F05D4H	TX message buffer data field 11 register 2 L	TMDF2_11LL	TMDF2_11L	0000H	8, 16
F05D5H		TMDF2_11LH			
F05D6H	TX message buffer data field 11 register 2 H	TMDF2_11HL	TMDF2_11H	0000H	8, 16
F05D7H		TMDF2_11HH			
F05D8H	TX message buffer data field 12 register 2 L	TMDF2_12LL	TMDF2_12L	0000H	8, 16
F05D9H		TMDF2_12LH			
F05DAH	TX message buffer data field 12 register 2 H	TMDF2_12HL	TMDF2_12H	0000H	8, 16
F05DBH		TMDF2_12HH			
F05DCH	TX message buffer data field 13 register 2 L	TMDF2_13LL	TMDF2_13L	0000H	8, 16
F05DDH		TMDF2_13LH			
F05DEH	TX message buffer data field 13 register 2 H	TMDF2_13HL	TMDF2_13H	0000H	8, 16
F05DFH		TMDF2_13HH			
F05E0H	TX message buffer data field 14 register 2 L	TMDF2_14LL	TMDF2_14L	0000H	8, 16
F05E1H		TMDF2_14LH			
F05E2H	TX message buffer data field 14 register 2 H	TMDF2_14HL	TMDF2_14H	0000H	8, 16
F05E3H		TMDF2_14HH			
F05E4H	TX message buffer data field 15 register 2 L	TMDF2_15LL	TMDF2_15L	0000H	8, 16
F05E5H		TMDF2_15LH			
F05E6H	TX message buffer data field 15 register 2 H	TMDF2_15HL	TMDF2_15H	0000H	8, 16
F05E7H		TMDF2_15HH			
F05E8H	TX message buffer ID register 3 L	TMID3LL	TMID3L	0000H	8, 16
F05E9H		TMID3LH			
F05EAH	TX message buffer ID register 3 H	TMID3HL	TMID3H	0000H	8, 16
F05EBH		TMID3HH			
F05EEH	TX message buffer pointer register 3 H	—	TMPTR3H	0000H	8, 16
F05EFH		TMPTR3HH			
F05F0H	TX message buffer CAN-FD control register 3 L	TMFDCTR3LL	TMFDCTR3L	0000H	8, 16
F05F1H		TMFDCTR3LH			
F05F2H	TX message buffer CAN-FD control register 3 H	TMFDCTR3HL	TMFDCTR3H	0000H	8, 16
F05F3H		TMFDCTR3HH			
F05F4H	TX message buffer data field 0 register 3 L	TMDF3_0LL	TMDF3_0L	0000H	8, 16
F05F5H		TMDF3_0LH			
F05F6H	TX message buffer data field 0 register 3 H	TMDF3_0HL	TMDF3_0H	0000H	8, 16
F05F7H		TMDF3_0HH			
F05F8H	TX message buffer data field 1 register 3 L	TMDF3_1LL	TMDF3_1L	0000H	8, 16
F05F9H		TMDF3_1LH			
F05FAH	TX message buffer data field 1 register 3 H	TMDF3_1HL	TMDF3_1H	0000H	8, 16
F05FBH		TMDF3_1HH			
F05FCH	TX message buffer data field 2 register 3 L	TMDF3_2LL	TMDF3_2L	0000H	8, 16
F05FDH		TMDF3_2LH			
F05FEH	TX message buffer data field 2 register 3 H	TMDF3_2HL	TMDF3_2H	0000H	8, 16
F05FFH		TMDF3_2HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (11/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0600H	TX message buffer data field 3 register 3 L	TMDF3_3LL	TMDF3_3L	0000H	8, 16
F0601H		TMDF3_3LH			
F0602H	TX message buffer data field 3 register 3 H	TMDF3_3HL	TMDF3_3H	0000H	8, 16
F0603H		TMDF3_3HH			
F0604H	TX message buffer data field 4 register 3 L	TMDF3_4LL	TMDF3_4L	0000H	8, 16
F0605H		TMDF3_4LH			
F0606H	TX message buffer data field 4 register 3 H	TMDF3_4HL	TMDF3_4H	0000H	8, 16
F0607H		TMDF3_4HH			
F0608H	TX message buffer data field 5 register 3 L	TMDF3_5LL	TMDF3_5L	0000H	8, 16
F0609H		TMDF3_5LH			
F060AH	TX message buffer data field 5 register 3 H	TMDF3_5HL	TMDF3_5H	0000H	8, 16
F060BH		TMDF3_5HH			
F060CH	TX message buffer data field 6 register 3 L	TMDF3_6LL	TMDF3_6L	0000H	8, 16
F060DH		TMDF3_6LH			
F060EH	TX message buffer data field 6 register 3 H	TMDF3_6HL	TMDF3_6H	0000H	8, 16
F060FH		TMDF3_6HH			
F0610H	TX message buffer data field 7 register 3 L	TMDF3_7LL	TMDF3_7L	0000H	8, 16
F0611H		TMDF3_7LH			
F0612H	TX message buffer data field 7 register 3 H	TMDF3_7HL	TMDF3_7H	0000H	8, 16
F0613H		TMDF3_7HH			
F0614H	TX message buffer data field 8 register 3 L	TMDF3_8LL	TMDF3_8L	0000H	8, 16
F0615H		TMDF3_8LH			
F0616H	TX message buffer data field 8 register 3 H	TMDF3_8HL	TMDF3_8H	0000H	8, 16
F0617H		TMDF3_8HH			
F0618H	TX message buffer data field 9 register 3 L	TMDF3_9LL	TMDF3_9L	0000H	8, 16
F0619H		TMDF3_9LH			
F061AH	TX message buffer data field 9 register 3 H	TMDF3_9HL	TMDF3_9H	0000H	8, 16
F061BH		TMDF3_9HH			
F061CH	TX message buffer data field 10 register 3 L	TMDF3_10LL	TMDF3_10L	0000H	8, 16
F061DH		TMDF3_10LH			
F061EH	TX message buffer data field 10 register 3 H	TMDF3_10HL	TMDF3_10H	0000H	8, 16
F061FH		TMDF3_10HH			
F0620H	TX message buffer data field 11 register 3 L	TMDF3_11LL	TMDF3_11L	0000H	8, 16
F0621H		TMDF3_11LH			
F0622H	TX message buffer data field 11 register 3 H	TMDF3_11HL	TMDF3_11H	0000H	8, 16
F0623H		TMDF3_11HH			
F0624H	TX message buffer data field 12 register 3 L	TMDF3_12LL	TMDF3_12L	0000H	8, 16
F0625H		TMDF3_12LH			
F0626H	TX message buffer data field 12 register 3 H	TMDF3_12HL	TMDF3_12H	0000H	8, 16
F0627H		TMDF3_12HH			
F0628H	TX message buffer data field 13 register 3 L	TMDF3_13LL	TMDF3_13L	0000H	8, 16
F0629H		TMDF3_13LH			
F062AH	TX message buffer data field 13 register 3 H	TMDF3_13HL	TMDF3_13H	0000H	8, 16
F062BH		TMDF3_13HH			
F062CH	TX message buffer data field 14 register 3 L	TMDF3_14LL	TMDF3_14L	0000H	8, 16
F062DH		TMDF3_14LH			
F062EH	TX message buffer data field 14 register 3 H	TMDF3_14HL	TMDF3_14H	0000H	8, 16
F062FH		TMDF3_14HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-2. List of RS-CANFD lite Window Registers for RL78/F24 (Page.1) (12/12)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0630H	TX message buffer data field 15 register 3 L	TMDF3_15LL	TMDF3_15L	0000H	8, 16
F0631H		TMDF3_15LH			
F0632H	TX message buffer data field 15 register 3 H	TMDF3_15HL	TMDF3_15H	0000H	8, 16
F0633H		TMDF3_15HH			
F0640H	TX history list access register 0 L	THLACC0LL	THLACC0L	0000H	8, 16
F0641H		—			
F0642H	TX history list access register 0 H	THLACC0HL	THLACC0H	0000H	8, 16
F0643H		THLACC0HH			
F0644H	TX history list access register 1 L	THLACC1LL	THLACC1L	0000H	8, 16
F0645H		THLACC1LH			
F0646H	TX history list access register 1 H	THLACC1HL	THLACC1H	0000H	8, 16
F0647H		—			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 01B (page.1 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (1/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0420H	RX message buffer ID register 0 L	RMID0LL	RMID0L	0000H	8, 16
F0421H		RMID0LH			
F0422H	RX message buffer ID register 0 H	RMID0HL	RMID0H	0000H	8, 16
F0423H		RMID0HH			
F0424H	RX message buffer pointer register 0 L	RMPTR0LL	RMPTR0L	0000H	8, 16
F0425H		RMPTR0LH			
F0426H	RX message buffer pointer register 0 H	—	RMPTR0H	0000H	8, 16
F0427H		RMPTR0HH			
F0428H	RX message buffer CAN-FD status register 0 L	RMFDSTS0LL	RMFDSTS0L	0000H	8, 16
F0429H		RMFDSTS0LH			
F042AH	RX message buffer CAN-FD status register 0 H	RMFDSTS0HL	RMFDSTS0H	0000H	8, 16
F042BH		RMFDSTS0HH			
F042CH	RX message buffer data field 0 register 0 L	RMDF0_0LL	RMDF0_0L	0000H	8, 16
F042DH		RMDF0_0LH			
F042EH	RX message buffer data field 0 register 0 H	RMDF0_0HL	RMDF0_0H	0000H	8, 16
F042FH		RMDF0_0HH			
F0430H	RX message buffer data field 1 register 0 L	RMDF0_1LL	RMDF0_1L	0000H	8, 16
F0431H		RMDF0_1LH			
F0432H	RX message buffer data field 1 register 0 H	RMDF0_1HL	RMDF0_1H	0000H	8, 16
F0433H		RMDF0_1HH			
F0434H	RX message buffer data field 2 register 0 L	RMDF0_2LL	RMDF0_2L	0000H	8, 16
F0435H		RMDF0_2LH			
F0436H	RX message buffer data field 2 register 0 H	RMDF0_2HL	RMDF0_2H	0000H	8, 16
F0437H		RMDF0_2HH			
F0438H	RX message buffer data field 3 register 0 L	RMDF0_3LL	RMDF0_3L	0000H	8, 16
F0439H		RMDF0_3LH			
F043AH	RX message buffer data field 3 register 0 H	RMDF0_3HL	RMDF0_3H	0000H	8, 16
F043BH		RMDF0_3HH			
F043CH	RX message buffer data field 4 register 0 L	RMDF0_4LL	RMDF0_4L	0000H	8, 16
F043DH		RMDF0_4LH			
F043EH	RX message buffer data field 4 register 0 H	RMDF0_4HL	RMDF0_4H	0000H	8, 16
F043FH		RMDF0_4HH			
F0440H	RX message buffer data field 5 register 0 L	RMDF0_5LL	RMDF0_5L	0000H	8, 16
F0441H		RMDF0_5LH			
F0442H	RX message buffer data field 5 register 0 H	RMDF0_5HL	RMDF0_5H	0000H	8, 16
F0443H		RMDF0_5HH			
F0444H	RX message buffer data field 6 register 0 L	RMDF0_6LL	RMDF0_6L	0000H	8, 16
F0445H		RMDF0_6LH			
F0446H	RX message buffer data field 6 register 0 H	RMDF0_6HL	RMDF0_6H	0000H	8, 16
F0447H		RMDF0_6HH			
F0448H	RX message buffer data field 7 register 0 L	RMDF0_7LL	RMDF0_7L	0000H	8, 16
F0449H		RMDF0_7LH			
F044AH	RX message buffer data field 7 register 0 H	RMDF0_7HL	RMDF0_7H	0000H	8, 16
F044BH		RMDF0_7HH			
F044CH	RX message buffer data field 8 register 0 L	RMDF0_8LL	RMDF0_8L	0000H	8, 16
F044DH		RMDF0_8LH			
F044EH	RX message buffer data field 8 register 0 H	RMDF0_8HL	RMDF0_8H	0000H	8, 16
F044FH		RMDF0_8HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (2/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0450H	RX message buffer data field 9 register 0 L	RMDF0_9LL	RMDF0_9L	0000H	8, 16
F0451H		RMDF0_9LH			
F0452H	RX message buffer data field 9 register 0 H	RMDF0_9HL	RMDF0_9H	0000H	8, 16
F0453H		RMDF0_9HH			
F0454H	RX message buffer data field 10 register 0 L	RMDF0_10LL	RMDF0_10L	0000H	8, 16
F0455H		RMDF0_10LH			
F0456H	RX message buffer data field 10 register 0 H	RMDF0_10HL	RMDF0_10H	0000H	8, 16
F0457H		RMDF0_10HH			
F0458H	RX message buffer data field 11 register 0 L	RMDF0_11LL	RMDF0_11L	0000H	8, 16
F0459H		RMDF0_11LH			
F045AH	RX message buffer data field 11 register 0 H	RMDF0_11HL	RMDF0_11H	0000H	8, 16
F045BH		RMDF0_11HH			
F045CH	RX message buffer data field 12 register 0 L	RMDF0_12LL	RMDF0_12L	0000H	8, 16
F045DH		RMDF0_12LH			
F045EH	RX message buffer data field 12 register 0 H	RMDF0_12HL	RMDF0_12H	0000H	8, 16
F045FH		RMDF0_12HH			
F0460H	RX message buffer data field 13 register 0 L	RMDF0_13LL	RMDF0_13L	0000H	8, 16
F0461H		RMDF0_13LH			
F0462H	RX message buffer data field 13 register 0 H	RMDF0_13HL	RMDF0_13H	0000H	8, 16
F0463H		RMDF0_13HH			
F0464H	RX message buffer data field 14 register 0 L	RMDF0_14LL	RMDF0_14L	0000H	8, 16
F0465H		RMDF0_14LH			
F0466H	RX message buffer data field 14 register 0 H	RMDF0_14HL	RMDF0_14H	0000H	8, 16
F0467H		RMDF0_14HH			
F0468H	RX message buffer data field 15 register 0 L	RMDF0_15LL	RMDF0_15L	0000H	8, 16
F0469H		RMDF0_15LH			
F046AH	RX message buffer data field 15 register 0 H	RMDF0_15HL	RMDF0_15H	0000H	8, 16
F046BH		RMDF0_15HH			
F046CH	RX message buffer ID register 1 L	RMID1LL	RMID1L	0000H	8, 16
F046DH		RMID1LH			
F046EH	RX message buffer ID register 1 H	RMID1HL	RMID1H	0000H	8, 16
F046FH		RMID1HH			
F0470H	RX message buffer pointer register 1 L	RMPTR1LL	RMPTR1L	0000H	8, 16
F0471H		RMPTR1LH			
F0472H	RX message buffer pointer register 1 H	—	RMPTR1H	0000H	8, 16
F0473H		RMPTR1HH			
F0474H	RX message buffer CAN-FD status register 1 L	RMFDSTS1LL	RMFDSTS1L	0000H	8, 16
F0475H		RMFDSTS1LH			
F0476H	RX message buffer CAN-FD status register 1 H	RMFDSTS1HL	RMFDSTS1H	0000H	8, 16
F0477H		RMFDSTS1HH			
F0478H	RX message buffer data field 0 register 1 L	RMDF1_0LL	RMDF1_0L	0000H	8, 16
F0479H		RMDF1_0LH			
F047AH	RX message buffer data field 0 register 1 H	RMDF1_0HL	RMDF1_0H	0000H	8, 16
F047BH		RMDF1_0HH			
F047CH	RX message buffer data field 1 register 1 L	RMDF1_1LL	RMDF1_1L	0000H	8, 16
F047DH		RMDF1_1LH			
F047EH	RX message buffer data field 1 register 1 H	RMDF1_1HL	RMDF1_1H	0000H	8, 16
F047FH		RMDF1_1HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (3/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0480H	RX message buffer data field 2 register 1 L	RMDF1_2LL	RMDF1_2L	0000H	8, 16
F0481H		RMDF1_2LH			
F0482H	RX message buffer data field 2 register 1 H	RMDF1_2HL	RMDF1_2H	0000H	8, 16
F0483H		RMDF1_2HH			
F0484H	RX message buffer data field 3 register 1 L	RMDF1_3LL	RMDF1_3L	0000H	8, 16
F0485H		RMDF1_3LH			
F0486H	RX message buffer data field 3 register 1 H	RMDF1_3HL	RMDF1_3H	0000H	8, 16
F0487H		RMDF1_3HH			
F0488H	RX message buffer data field 4 register 1 L	RMDF1_4LL	RMDF1_4L	0000H	8, 16
F0489H		RMDF1_4LH			
F048AH	RX message buffer data field 4 register 1 H	RMDF1_4HL	RMDF1_4H	0000H	8, 16
F048BH		RMDF1_4HH			
F048CH	RX message buffer data field 5 register 1 L	RMDF1_5LL	RMDF1_5L	0000H	8, 16
F048DH		RMDF1_5LH			
F048EH	RX message buffer data field 5 register 1 H	RMDF1_5HL	RMDF1_5H	0000H	8, 16
F048FH		RMDF1_5HH			
F0490H	RX message buffer data field 6 register 1 L	RMDF1_6LL	RMDF1_6L	0000H	8, 16
F0491H		RMDF1_6LH			
F0492H	RX message buffer data field 6 register 1 H	RMDF1_6HL	RMDF1_6H	0000H	8, 16
F0493H		RMDF1_6HH			
F0494H	RX message buffer data field 7 register 1 L	RMDF1_7LL	RMDF1_7L	0000H	8, 16
F0495H		RMDF1_7LH			
F0496H	RX message buffer data field 7 register 1 H	RMDF1_7HL	RMDF1_7H	0000H	8, 16
F0497H		RMDF1_7HH			
F0498H	RX message buffer data field 8 register 1 L	RMDF1_8LL	RMDF1_8L	0000H	8, 16
F0499H		RMDF1_8LH			
F049AH	RX message buffer data field 8 register 1 H	RMDF1_8HL	RMDF1_8H	0000H	8, 16
F049BH		RMDF1_8HH			
F049CH	RX message buffer data field 9 register 1 L	RMDF1_9LL	RMDF1_9L	0000H	8, 16
F049DH		RMDF1_9LH			
F049EH	RX message buffer data field 9 register 1 H	RMDF1_9HL	RMDF1_9H	0000H	8, 16
F049FH		RMDF1_9HH			
F04A0H	RX message buffer data field 10 register 1 L	RMDF1_10LL	RMDF1_10L	0000H	8, 16
F04A1H		RMDF1_10LH			
F04A2H	RX message buffer data field 10 register 1 H	RMDF1_10HL	RMDF1_10H	0000H	8, 16
F04A3H		RMDF1_10HH			
F04A4H	RX message buffer data field 11 register 1 L	RMDF1_11LL	RMDF1_11L	0000H	8, 16
F04A5H		RMDF1_11LH			
F04A6H	RX message buffer data field 11 register 1 H	RMDF1_11HL	RMDF1_11H	0000H	8, 16
F04A7H		RMDF1_11HH			
F04A8H	RX message buffer data field 12 register 1 L	RMDF1_12LL	RMDF1_12L	0000H	8, 16
F04A9H		RMDF1_12LH			
F04AAH	RX message buffer data field 12 register 1 H	RMDF1_12HL	RMDF1_12H	0000H	8, 16
F04ABH		RMDF1_12HH			
F04ACH	RX message buffer data field 13 register 1 L	RMDF1_13LL	RMDF1_13L	0000H	8, 16
F04ADH		RMDF1_13LH			
F04AEH	RX message buffer data field 13 register 1 H	RMDF1_13HL	RMDF1_13H	0000H	8, 16
F04AFH		RMDF1_13HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (4/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04B0H	RX message buffer data field 14 register 1 L	RMDF1_14LL	RMDF1_14L	0000H	8, 16
F04B1H		RMDF1_14LH			
F04B2H	RX message buffer data field 14 register 1 H	RMDF1_14HL	RMDF1_14H	0000H	8, 16
F04B3H		RMDF1_14HH			
F04B4H	RX message buffer data field 15 register 1 L	RMDF1_15LL	RMDF1_15L	0000H	8, 16
F04B5H		RMDF1_15LH			
F04B6H	RX message buffer data field 15 register 1 H	RMDF1_15HL	RMDF1_15H	0000H	8, 16
F04B7H		RMDF1_15HH			
F04B8H	RX message buffer ID register 2 L	RMID2LL	RMID2L	0000H	8, 16
F04B9H		RMID2LH			
F04BAH	RX message buffer ID register 2 H	RMID2HL	RMID2H	0000H	8, 16
F04BBH		RMID2HH			
F04BCH	RX message buffer pointer register 2 L	RMPTR2LL	RMPTR2L	0000H	8, 16
F04BDH		RMPTR2LH			
F04BEH	RX message buffer pointer register 2 H	—	RMPTR2H	0000H	8, 16
F04BFH		RMPTR2HH			
F04C0H	RX message buffer CAN-FD status register 2 L	RMFDSTS2LL	RMFDSTS2L	0000H	8, 16
F04C1H		RMFDSTS2LH			
F04C2H	RX message buffer CAN-FD status register 2 H	RMFDSTS2HL	RMFDSTS2H	0000H	8, 16
F04C3H		RMFDSTS2HH			
F04C4H	RX message buffer data field 0 register 2 L	RMDF2_0LL	RMDF2_0L	0000H	8, 16
F04C5H		RMDF2_0LH			
F04C6H	RX message buffer data field 0 register 2 H	RMDF2_0HL	RMDF2_0H	0000H	8, 16
F04C7H		RMDF2_0HH			
F04C8H	RX message buffer data field 1 register 2 L	RMDF2_1LL	RMDF2_1L	0000H	8, 16
F04C9H		RMDF2_1LH			
F04CAH	RX message buffer data field 1 register 2 H	RMDF2_1HL	RMDF2_1H	0000H	8, 16
F04CBH		RMDF2_1HH			
F04CCH	RX message buffer data field 2 register 2 L	RMDF2_2LL	RMDF2_2L	0000H	8, 16
F04CDH		RMDF2_2LH			
F04CEH	RX message buffer data field 2 register 2 H	RMDF2_2HL	RMDF2_2H	0000H	8, 16
F04CFH		RMDF2_2HH			
F04D0H	RX message buffer data field 3 register 2 L	RMDF2_3LL	RMDF2_3L	0000H	8, 16
F04D1H		RMDF2_3LH			
F04D2H	RX message buffer data field 3 register 2 H	RMDF2_3HL	RMDF2_3H	0000H	8, 16
F04D3H		RMDF2_3HH			
F04D4H	RX message buffer data field 4 register 2 L	RMDF2_4LL	RMDF2_4L	0000H	8, 16
F04D5H		RMDF2_4LH			
F04D6H	RX message buffer data field 4 register 2 H	RMDF2_4HL	RMDF2_4H	0000H	8, 16
F04D7H		RMDF2_4HH			
F04D8H	RX message buffer data field 5 register 2 L	RMDF2_5LL	RMDF2_5L	0000H	8, 16
F04D9H		RMDF2_5LH			
F04DAH	RX message buffer data field 5 register 2 H	RMDF2_5HL	RMDF2_5H	0000H	8, 16
F04DBH		RMDF2_5HH			
F04DCH	RX message buffer data field 6 register 2 L	RMDF2_6LL	RMDF2_6L	0000H	8, 16
F04DDH		RMDF2_6LH			
F04DEH	RX message buffer data field 6 register 2 H	RMDF2_6HL	RMDF2_6H	0000H	8, 16
F04DFH		RMDF2_6HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (5/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04E0H	RX message buffer data field 7 register 2 L	RMDF2_7LL	RMDF2_7L	0000H	8, 16
F04E1H		RMDF2_7LH			
F04E2H	RX message buffer data field 7 register 2 H	RMDF2_7HL	RMDF2_7H	0000H	8, 16
F04E3H		RMDF2_7HH			
F04E4H	RX message buffer data field 8 register 2 L	RMDF2_8LL	RMDF2_8L	0000H	8, 16
F04E5H		RMDF2_8LH			
F04E6H	RX message buffer data field 8 register 2 H	RMDF2_8HL	RMDF2_8H	0000H	8, 16
F04E7H		RMDF2_8HH			
F04E8H	RX message buffer data field 9 register 2 L	RMDF2_9LL	RMDF2_9L	0000H	8, 16
F04E9H		RMDF2_9LH			
F04EAH	RX message buffer data field 9 register 2 H	RMDF2_9HL	RMDF2_9H	0000H	8, 16
F04EBH		RMDF2_9HH			
F04ECH	RX message buffer data field 10 register 2 L	RMDF2_10LL	RMDF2_10L	0000H	8, 16
F04EDH		RMDF2_10LH			
F04EEH	RX message buffer data field 10 register 2 H	RMDF2_10HL	RMDF2_10H	0000H	8, 16
F04EFH		RMDF2_10HH			
F04F0H	RX message buffer data field 11 register 2 L	RMDF2_11LL	RMDF2_11L	0000H	8, 16
F04F1H		RMDF2_11LH			
F04F2H	RX message buffer data field 11 register 2 H	RMDF2_11HL	RMDF2_11H	0000H	8, 16
F04F3H		RMDF2_11HH			
F04F4H	RX message buffer data field 12 register 2 L	RMDF2_12LL	RMDF2_12L	0000H	8, 16
F04F5H		RMDF2_12LH			
F04F6H	RX message buffer data field 12 register 2 H	RMDF2_12HL	RMDF2_12H	0000H	8, 16
F04F7H		RMDF2_12HH			
F04F8H	RX message buffer data field 13 register 2 L	RMDF2_13LL	RMDF2_13L	0000H	8, 16
F04F9H		RMDF2_13LH			
F04FAH	RX message buffer data field 13 register 2 H	RMDF2_13HL	RMDF2_13H	0000H	8, 16
F04FBH		RMDF2_13HH			
F04FCH	RX message buffer data field 14 register 2 L	RMDF2_14LL	RMDF2_14L	0000H	8, 16
F04FDH		RMDF2_14LH			
F04FEH	RX message buffer data field 14 register 2 H	RMDF2_14HL	RMDF2_14H	0000H	8, 16
F04FFH		RMDF2_14HH			
F0500H	RX message buffer data field 15 register 2 L	RMDF2_15LL	RMDF2_15L	0000H	8, 16
F0501H		RMDF2_15LH			
F0502H	RX message buffer data field 15 register 2 H	RMDF2_15HL	RMDF2_15H	0000H	8, 16
F0503H		RMDF2_15HH			
F0504H	RX message buffer ID register 3 L	RMID3LL	RMID3L	0000H	8, 16
F0505H		RMID3LH			
F0506H	RX message buffer ID register 3 H	RMID3HL	RMID3H	0000H	8, 16
F0507H		RMID3HH			
F0508H	RX message buffer pointer register 3 L	RMPTR3LL	RMPTR3L	0000H	8, 16
F0509H		RMPTR3LH			
F050AH	RX message buffer pointer register 3 H	—	RMPTR3H	0000H	8, 16
F050BH		RMPTR3HH			
F050CH	RX message buffer CAN-FD status register 3 L	RMFDSTS3LL	RMFDSTS3L	0000H	8, 16
F050DH		RMFDSTS3LH			
F050EH	RX message buffer CAN-FD status register 3 H	RMFDSTS3HL	RMFDSTS3H	0000H	8, 16
F050FH		RMFDSTS3HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (6/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0510H	RX message buffer data field 0 register 3 L	RMDF3_0LL	RMDF3_0L	0000H	8, 16
F0511H		RMDF3_0LH			
F0512H	RX message buffer data field 0 register 3 H	RMDF3_0HL	RMDF3_0H	0000H	8, 16
F0513H		RMDF3_0HH			
F0514H	RX message buffer data field 1 register 3 L	RMDF3_1LL	RMDF3_1L	0000H	8, 16
F0515H		RMDF3_1LH			
F0516H	RX message buffer data field 1 register 3 H	RMDF3_1HL	RMDF3_1H	0000H	8, 16
F0517H		RMDF3_1HH			
F0518H	RX message buffer data field 2 register 3 L	RMDF3_2LL	RMDF3_2L	0000H	8, 16
F0519H		RMDF3_2LH			
F051AH	RX message buffer data field 2 register 3 H	RMDF3_2HL	RMDF3_2H	0000H	8, 16
F051BH		RMDF3_2HH			
F051CH	RX message buffer data field 3 register 3 L	RMDF3_3LL	RMDF3_3L	0000H	8, 16
F051DH		RMDF3_3LH			
F051EH	RX message buffer data field 3 register 3 H	RMDF3_3HL	RMDF3_3H	0000H	8, 16
F051FH		RMDF3_3HH			
F0520H	RX message buffer data field 4 register 3 L	RMDF3_4LL	RMDF3_4L	0000H	8, 16
F0521H		RMDF3_4LH			
F0522H	RX message buffer data field 4 register 3 H	RMDF3_4HL	RMDF3_4H	0000H	8, 16
F0523H		RMDF3_4HH			
F0524H	RX message buffer data field 5 register 3 L	RMDF3_5LL	RMDF3_5L	0000H	8, 16
F0525H		RMDF3_5LH			
F0526H	RX message buffer data field 5 register 3 H	RMDF3_5HL	RMDF3_5H	0000H	8, 16
F0527H		RMDF3_5HH			
F0528H	RX message buffer data field 6 register 3 L	RMDF3_6LL	RMDF3_6L	0000H	8, 16
F0529H		RMDF3_6LH			
F052AH	RX message buffer data field 6 register 3 H	RMDF3_6HL	RMDF3_6H	0000H	8, 16
F052BH		RMDF3_6HH			
F052CH	RX message buffer data field 7 register 3 L	RMDF3_7LL	RMDF3_7L	0000H	8, 16
F052DH		RMDF3_7LH			
F052EH	RX message buffer data field 7 register 3 H	RMDF3_7HL	RMDF3_7H	0000H	8, 16
F052FH		RMDF3_7HH			
F0530H	RX message buffer data field 8 register 3 L	RMDF3_8LL	RMDF3_8L	0000H	8, 16
F0531H		RMDF3_8LH			
F0532H	RX message buffer data field 8 register 3 H	RMDF3_8HL	RMDF3_8H	0000H	8, 16
F0533H		RMDF3_8HH			
F0534H	RX message buffer data field 9 register 3 L	RMDF3_9LL	RMDF3_9L	0000H	8, 16
F0535H		RMDF3_9LH			
F0536H	RX message buffer data field 9 register 3 H	RMDF3_9HL	RMDF3_9H	0000H	8, 16
F0537H		RMDF3_9HH			
F0538H	RX message buffer data field 10 register 3 L	RMDF3_10LL	RMDF3_10L	0000H	8, 16
F0539H		RMDF3_10LH			
F053AH	RX message buffer data field 10 register 3 H	RMDF3_10HL	RMDF3_10H	0000H	8, 16
F053BH		RMDF3_10HH			
F053CH	RX message buffer data field 11 register 3 L	RMDF3_11LL	RMDF3_11L	0000H	8, 16
F053DH		RMDF3_11LH			
F053EH	RX message buffer data field 11 register 3 H	RMDF3_11HL	RMDF3_11H	0000H	8, 16
F053FH		RMDF3_11HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (7/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0540H	RX message buffer data field 12 register 3 L	RMDF3_12LL	RMDF3_12L	0000H	8, 16
F0541H		RMDF3_12LH			
F0542H	RX message buffer data field 12 register 3 H	RMDF3_12HL	RMDF3_12H	0000H	8, 16
F0543H		RMDF3_12HH			
F0544H	RX message buffer data field 13 register 3 L	RMDF3_13LL	RMDF3_13L	0000H	8, 16
F0545H		RMDF3_13LH			
F0546H	RX message buffer data field 13 register 3 H	RMDF3_13HL	RMDF3_13H	0000H	8, 16
F0547H		RMDF3_13HH			
F0548H	RX message buffer data field 14 register 3 L	RMDF3_14LL	RMDF3_14L	0000H	8, 16
F0549H		RMDF3_14LH			
F054AH	RX message buffer data field 14 register 3 H	RMDF3_14HL	RMDF3_14H	0000H	8, 16
F054BH		RMDF3_14HH			
F054CH	RX message buffer data field 15 register 3 L	RMDF3_15LL	RMDF3_15L	0000H	8, 16
F054DH		RMDF3_15LH			
F054EH	RX message buffer data field 15 register 3 H	RMDF3_15HL	RMDF3_15H	0000H	8, 16
F054FH		RMDF3_15HH			
F0550H	RX message buffer ID register 4 L	RMID4LL	RMID4L	0000H	8, 16
F0551H		RMID4LH			
F0552H	RX message buffer ID register 4 H	RMID4HL	RMID4H	0000H	8, 16
F0553H		RMID4HH			
F0554H	RX message buffer pointer register 4 L	RMPTR4LL	RMPTR4L	0000H	8, 16
F0555H		RMPTR4LH			
F0556H	RX message buffer pointer register 4 H	—	RMPTR4H	0000H	8, 16
F0557H		RMPTR4HH			
F0558H	RX message buffer CAN-FD status register 4 L	RMFDSTS4LL	RMFDSTS4L	0000H	8, 16
F0559H		RMFDSTS4LH			
F055AH	RX message buffer CAN-FD status register 4 H	RMFDSTS4HL	RMFDSTS4H	0000H	8, 16
F055BH		RMFDSTS4HH			
F055CH	RX message buffer data field 0 register 4 L	RMDF4_0LL	RMDF4_0L	0000H	8, 16
F055DH		RMDF4_0LH			
F055EH	RX message buffer data field 0 register 4 H	RMDF4_0HL	RMDF4_0H	0000H	8, 16
F055FH		RMDF4_0HH			
F0560H	RX message buffer data field 1 register 4 L	RMDF4_1LL	RMDF4_1L	0000H	8, 16
F0561H		RMDF4_1LH			
F0562H	RX message buffer data field 1 register 4 H	RMDF4_1HL	RMDF4_1H	0000H	8, 16
F0563H		RMDF4_1HH			
F0564H	RX message buffer data field 2 register 4 L	RMDF4_2LL	RMDF4_2L	0000H	8, 16
F0565H		RMDF4_2LH			
F0566H	RX message buffer data field 2 register 4 H	RMDF4_2HL	RMDF4_2H	0000H	8, 16
F0567H		RMDF4_2HH			
F0568H	RX message buffer data field 3 register 4 L	RMDF4_3LL	RMDF4_3L	0000H	8, 16
F0569H		RMDF4_3LH			
F056AH	RX message buffer data field 3 register 4 H	RMDF4_3HL	RMDF4_3H	0000H	8, 16
F056BH		RMDF4_3HH			
F056CH	RX message buffer data field 4 register 4 L	RMDF4_4LL	RMDF4_4L	0000H	8, 16
F056DH		RMDF4_4LH			
F056EH	RX message buffer data field 4 register 4 H	RMDF4_4HL	RMDF4_4H	0000H	8, 16
F056FH		RMDF4_4HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (8/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0570H	RX message buffer data field 5 register 4 L	RMDF4_5LL	RMDF4_5L	0000H	8, 16
F0571H		RMDF4_5LH			
F0572H	RX message buffer data field 5 register 4 H	RMDF4_5HL	RMDF4_5H	0000H	8, 16
F0573H		RMDF4_5HH			
F0574H	RX message buffer data field 6 register 4 L	RMDF4_6LL	RMDF4_6L	0000H	8, 16
F0575H		RMDF4_6LH			
F0576H	RX message buffer data field 6 register 4 H	RMDF4_6HL	RMDF4_6H	0000H	8, 16
F0577H		RMDF4_6HH			
F0578H	RX message buffer data field 7 register 4 L	RMDF4_7LL	RMDF4_7L	0000H	8, 16
F0579H		RMDF4_7LH			
F057AH	RX message buffer data field 7 register 4 H	RMDF4_7HL	RMDF4_7H	0000H	8, 16
F057BH		RMDF4_7HH			
F057CH	RX message buffer data field 8 register 4 L	RMDF4_8LL	RMDF4_8L	0000H	8, 16
F057DH		RMDF4_8LH			
F057EH	RX message buffer data field 8 register 4 H	RMDF4_8HL	RMDF4_8H	0000H	8, 16
F057FH		RMDF4_8HH			
F0580H	RX message buffer data field 9 register 4 L	RMDF4_9LL	RMDF4_9L	0000H	8, 16
F0581H		RMDF4_9LH			
F0582H	RX message buffer data field 9 register 4 H	RMDF4_9HL	RMDF4_9H	0000H	8, 16
F0583H		RMDF4_9HH			
F0584H	RX message buffer data field 10 register 4 L	RMDF4_10LL	RMDF4_10L	0000H	8, 16
F0585H		RMDF4_10LH			
F0586H	RX message buffer data field 10 register 4 H	RMDF4_10HL	RMDF4_10H	0000H	8, 16
F0587H		RMDF4_10HH			
F0588H	RX message buffer data field 11 register 4 L	RMDF4_11LL	RMDF4_11L	0000H	8, 16
F0589H		RMDF4_11LH			
F058AH	RX message buffer data field 11 register 4 H	RMDF4_11HL	RMDF4_11H	0000H	8, 16
F058BH		RMDF4_11HH			
F058CH	RX message buffer data field 12 register 4 L	RMDF4_12LL	RMDF4_12L	0000H	8, 16
F058DH		RMDF4_12LH			
F058EH	RX message buffer data field 12 register 4 H	RMDF4_12HL	RMDF4_12H	0000H	8, 16
F058FH		RMDF4_12HH			
F0590H	RX message buffer data field 13 register 4 L	RMDF4_13LL	RMDF4_13L	0000H	8, 16
F0591H		RMDF4_13LH			
F0592H	RX message buffer data field 13 register 4 H	RMDF4_13HL	RMDF4_13H	0000H	8, 16
F0593H		RMDF4_13HH			
F0594H	RX message buffer data field 14 register 4 L	RMDF4_14LL	RMDF4_14L	0000H	8, 16
F0595H		RMDF4_14LH			
F0596H	RX message buffer data field 14 register 4 H	RMDF4_14HL	RMDF4_14H	0000H	8, 16
F0597H		RMDF4_14HH			
F0598H	RX message buffer data field 15 register 4 L	RMDF4_15LL	RMDF4_15L	0000H	8, 16
F0599H		RMDF4_15LH			
F059AH	RX message buffer data field 15 register 4 H	RMDF4_15HL	RMDF4_15H	0000H	8, 16
F059BH		RMDF4_15HH			
F059CH	RX message buffer ID register 5 L	RMID5LL	RMID5L	0000H	8, 16
F059DH		RMID5LH			
F059EH	RX message buffer ID register 5 H	RMID5HL	RMID5H	0000H	8, 16
F059FH		RMID5HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (9/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05A0H	RX message buffer pointer register 5 L	RMPTR5LL	RMPTR5L	0000H	8, 16
F05A1H		RMPTR5LH			
F05A2H	RX message buffer pointer register 5 H	—	RMPTR5H	0000H	8, 16
F05A3H		RMPTR5HH			
F05A4H	RX message buffer CAN-FD status register 5 L	RMFDSTS5LL	RMFDSTS5L	0000H	8, 16
F05A5H		RMFDSTS5LH			
F05A6H	RX message buffer CAN-FD status register 5 H	RMFDSTS5HL	RMFDSTS5H	0000H	8, 16
F05A7H		RMFDSTS5HH			
F05A8H	RX message buffer data field 0 register 5 L	RMDF5_0LL	RMDF5_0L	0000H	8, 16
F05A9H		RMDF5_0LH			
F05AAH	RX message buffer data field 0 register 5 H	RMDF5_0HL	RMDF5_0H	0000H	8, 16
F05ABH		RMDF5_0HH			
F05ACH	RX message buffer data field 1 register 5 L	RMDF5_1LL	RMDF5_1L	0000H	8, 16
F05ADH		RMDF5_1LH			
F05AEH	RX message buffer data field 1 register 5 H	RMDF5_1HL	RMDF5_1H	0000H	8, 16
F05AFH		RMDF5_1HH			
F05B0H	RX message buffer data field 2 register 5 L	RMDF5_2LL	RMDF5_2L	0000H	8, 16
F05B1H		RMDF5_2LH			
F05B2H	RX message buffer data field 2 register 5 H	RMDF5_2HL	RMDF5_2H	0000H	8, 16
F05B3H		RMDF5_2HH			
F05B4H	RX message buffer data field 3 register 5 L	RMDF5_3LL	RMDF5_3L	0000H	8, 16
F05B5H		RMDF5_3LH			
F05B6H	RX message buffer data field 3 register 5 H	RMDF5_3HL	RMDF5_3H	0000H	8, 16
F05B7H		RMDF5_3HH			
F05B8H	RX message buffer data field 4 register 5 L	RMDF5_4LL	RMDF5_4L	0000H	8, 16
F05B9H		RMDF5_4LH			
F05BAH	RX message buffer data field 4 register 5 H	RMDF5_4HL	RMDF5_4H	0000H	8, 16
F05BBH		RMDF5_4HH			
F05BCH	RX message buffer data field 5 register 5 L	RMDF5_5LL	RMDF5_5L	0000H	8, 16
F05BDH		RMDF5_5LH			
F05BEH	RX message buffer data field 5 register 5 H	RMDF5_5HL	RMDF5_5H	0000H	8, 16
F05BFH		RMDF5_5HH			
F05C0H	RX message buffer data field 6 register 5 L	RMDF5_6LL	RMDF5_6L	0000H	8, 16
F05C1H		RMDF5_6LH			
F05C2H	RX message buffer data field 6 register 5 H	RMDF5_6HL	RMDF5_6H	0000H	8, 16
F05C3H		RMDF5_6HH			
F05C4H	RX message buffer data field 7 register 5 L	RMDF5_7LL	RMDF5_7L	0000H	8, 16
F05C5H		RMDF5_7LH			
F05C6H	RX message buffer data field 7 register 5 H	RMDF5_7HL	RMDF5_7H	0000H	8, 16
F05C7H		RMDF5_7HH			
F05C8H	RX message buffer data field 8 register 5 L	RMDF5_8LL	RMDF5_8L	0000H	8, 16
F05C9H		RMDF5_8LH			
F05CAH	RX message buffer data field 8 register 5 H	RMDF5_8HL	RMDF5_8H	0000H	8, 16
F05CBH		RMDF5_8HH			
F05CCH	RX message buffer data field 9 register 5 L	RMDF5_9LL	RMDF5_9L	0000H	8, 16
F05CDH		RMDF5_9LH			
F05CEH	RX message buffer data field 9 register 5 H	RMDF5_9HL	RMDF5_9H	0000H	8, 16
F05CFH		RMDF5_9HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (10/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05D0H	RX message buffer data field 10 register 5 L	RMDF5_10LL	RMDF5_10L	0000H	8, 16
F05D1H		RMDF5_10LH			
F05D2H	RX message buffer data field 10 register 5 H	RMDF5_10HL	RMDF5_10H	0000H	8, 16
F05D3H		RMDF5_10HH			
F05D4H	RX message buffer data field 11 register 5 L	RMDF5_11LL	RMDF5_11L	0000H	8, 16
F05D5H		RMDF5_11LH			
F05D6H	RX message buffer data field 11 register 5 H	RMDF5_11HL	RMDF5_11H	0000H	8, 16
F05D7H		RMDF5_11HH			
F05D8H	RX message buffer data field 12 register 5 L	RMDF5_12LL	RMDF5_12L	0000H	8, 16
F05D9H		RMDF5_12LH			
F05DAH	RX message buffer data field 12 register 5 H	RMDF5_12HL	RMDF5_12H	0000H	8, 16
F05DBH		RMDF5_12HH			
F05DCH	RX message buffer data field 13 register 5 L	RMDF5_13LL	RMDF5_13L	0000H	8, 16
F05DDH		RMDF5_13LH			
F05DEH	RX message buffer data field 13 register 5 H	RMDF5_13HL	RMDF5_13H	0000H	8, 16
F05DFH		RMDF5_13HH			
F05E0H	RX message buffer data field 14 register 5 L	RMDF5_14LL	RMDF5_14L	0000H	8, 16
F05E1H		RMDF5_14LH			
F05E2H	RX message buffer data field 14 register 5 H	RMDF5_14HL	RMDF5_14H	0000H	8, 16
F05E3H		RMDF5_14HH			
F05E4H	RX message buffer data field 15 register 5 L	RMDF5_15LL	RMDF5_15L	0000H	8, 16
F05E5H		RMDF5_15LH			
F05E6H	RX message buffer data field 15 register 5 H	RMDF5_15HL	RMDF5_15H	0000H	8, 16
F05E7H		RMDF5_15HH			
F05E8H	RX message buffer ID register 6 L	RMID6LL	RMID6L	0000H	8, 16
F05E9H		RMID6LH			
F05EAH	RX message buffer ID register 6 H	RMID6HL	RMID6H	0000H	8, 16
F05EBH		RMID6HH			
F05ECH	RX message buffer pointer register 6 L	RMPTR6LL	RMPTR6L	0000H	8, 16
F05EDH		RMPTR6LH			
F05EEH	RX message buffer pointer register 6 H	—	RMPTR6H	0000H	8, 16
F05EFH		RMPTR6HH			
F05F0H	RX message buffer CAN-FD status register 6 L	RMFDSTS6LL	RMFDSTS6L	0000H	8, 16
F05F1H		RMFDSTS6LH			
F05F2H	RX message buffer CAN-FD status register 6 H	RMFDSTS6HL	RMFDSTS6H	0000H	8, 16
F05F3H		RMFDSTS6HH			
F05F4H	RX message buffer data field 0 register 6 L	RMDF6_0LL	RMDF6_0L	0000H	8, 16
F05F5H		RMDF6_0LH			
F05F6H	RX message buffer data field 0 register 6 H	RMDF6_0HL	RMDF6_0H	0000H	8, 16
F05F7H		RMDF6_0HH			
F05F8H	RX message buffer data field 1 register 6 L	RMDF6_1LL	RMDF6_1L	0000H	8, 16
F05F9H		RMDF6_1LH			
F05FAH	RX message buffer data field 1 register 6 H	RMDF6_1HL	RMDF6_1H	0000H	8, 16
F05FBH		RMDF6_1HH			
F05FCH	RX message buffer data field 2 register 6 L	RMDF6_2LL	RMDF6_2L	0000H	8, 16
F05FDH		RMDF6_2LH			
F05FEH	RX message buffer data field 2 register 6 H	RMDF6_2HL	RMDF6_2H	0000H	8, 16
F05FFH		RMDF6_2HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (11/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0600H	RX message buffer data field 3 register 6 L	RMDF6_3LL	RMDF6_3L	0000H	8, 16
F0601H		RMDF6_3LH			
F0602H	RX message buffer data field 3 register 6 H	RMDF6_3HL	RMDF6_3H	0000H	8, 16
F0603H		RMDF6_3HH			
F0604H	RX message buffer data field 4 register 6 L	RMDF6_4LL	RMDF6_4L	0000H	8, 16
F0605H		RMDF6_4LH			
F0606H	RX message buffer data field 4 register 6 H	RMDF6_4HL	RMDF6_4H	0000H	8, 16
F0607H		RMDF6_4HH			
F0608H	RX message buffer data field 5 register 6 L	RMDF6_5LL	RMDF6_5L	0000H	8, 16
F0609H		RMDF6_5LH			
F060AH	RX message buffer data field 5 register 6 H	RMDF6_5HL	RMDF6_5H	0000H	8, 16
F060BH		RMDF6_5HH			
F060CH	RX message buffer data field 6 register 6 L	RMDF6_6LL	RMDF6_6L	0000H	8, 16
F060DH		RMDF6_6LH			
F060EH	RX message buffer data field 6 register 6 H	RMDF6_6HL	RMDF6_6H	0000H	8, 16
F060FH		RMDF6_6HH			
F0610H	RX message buffer data field 7 register 6 L	RMDF6_7LL	RMDF6_7L	0000H	8, 16
F0611H		RMDF6_7LH			
F0612H	RX message buffer data field 7 register 6 H	RMDF6_7HL	RMDF6_7H	0000H	8, 16
F0613H		RMDF6_7HH			
F0614H	RX message buffer data field 8 register 6 L	RMDF6_8LL	RMDF6_8L	0000H	8, 16
F0615H		RMDF6_8LH			
F0616H	RX message buffer data field 8 register 6 H	RMDF6_8HL	RMDF6_8H	0000H	8, 16
F0617H		RMDF6_8HH			
F0618H	RX message buffer data field 9 register 6 L	RMDF6_9LL	RMDF6_9L	0000H	8, 16
F0619H		RMDF6_9LH			
F061AH	RX message buffer data field 9 register 6 H	RMDF6_9HL	RMDF6_9H	0000H	8, 16
F061BH		RMDF6_9HH			
F061CH	RX message buffer data field 10 register 6 L	RMDF6_10LL	RMDF6_10L	0000H	8, 16
F061DH		RMDF6_10LH			
F061EH	RX message buffer data field 10 register 6 H	RMDF6_10HL	RMDF6_10H	0000H	8, 16
F061FH		RMDF6_10HH			
F0620H	RX message buffer data field 11 register 6 L	RMDF6_11LL	RMDF6_11L	0000H	8, 16
F0621H		RMDF6_11LH			
F0622H	RX message buffer data field 11 register 6 H	RMDF6_11HL	RMDF6_11H	0000H	8, 16
F0623H		RMDF6_11HH			
F0624H	RX message buffer data field 12 register 6 L	RMDF6_12LL	RMDF6_12L	0000H	8, 16
F0625H		RMDF6_12LH			
F0626H	RX message buffer data field 12 register 6 H	RMDF6_12HL	RMDF6_12H	0000H	8, 16
F0627H		RMDF6_12HH			
F0628H	RX message buffer data field 13 register 6 L	RMDF6_13LL	RMDF6_13L	0000H	8, 16
F0629H		RMDF6_13LH			
F062AH	RX message buffer data field 13 register 6 H	RMDF6_13HL	RMDF6_13H	0000H	8, 16
F062BH		RMDF6_13HH			
F062CH	RX message buffer data field 14 register 6 L	RMDF6_14LL	RMDF6_14L	0000H	8, 16
F062DH		RMDF6_14LH			
F062EH	RX message buffer data field 14 register 6 H	RMDF6_14HL	RMDF6_14H	0000H	8, 16
F062FH		RMDF6_14HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (12/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0630H	RX message buffer data field 15 register 6 L	RMDF6_15LL	RMDF6_15L	0000H	8, 16
F0631H		RMDF6_15LH			
F0632H	RX message buffer data field 15 register 6 H	RMDF6_15HL	RMDF6_15H	0000H	8, 16
F0633H		RMDF6_15HH			
F0634H	RX message buffer ID register 7 L	RMID7LL	RMID7L	0000H	8, 16
F0635H		RMID7LH			
F0636H	RX message buffer ID register 7 H	RMID7HL	RMID7H	0000H	8, 16
F0637H		RMID7HH			
F0638H	RX message buffer pointer register 7 L	RMPTR7LL	RMPTR7L	0000H	8, 16
F0639H		RMPTR7LH			
F063AH	RX message buffer pointer register 7 H	—	RMPTR7H	0000H	8, 16
F063BH		RMPTR7HH			
F063CH	RX message buffer CAN-FD status register 7 L	RMFDSTS7LL	RMFDSTS7L	0000H	8, 16
F063DH		RMFDSTS7LH			
F063EH	RX message buffer CAN-FD status register 7 H	RMFDSTS7HL	RMFDSTS7H	0000H	8, 16
F063FH		RMFDSTS7HH			
F0640H	RX message buffer data field 0 register 7 L	RMDF7_0LL	RMDF7_0L	0000H	8, 16
F0641H		RMDF7_0LH			
F0642H	RX message buffer data field 0 register 7 H	RMDF7_0HL	RMDF7_0H	0000H	8, 16
F0643H		RMDF7_0HH			
F0644H	RX message buffer data field 1 register 7 L	RMDF7_1LL	RMDF7_1L	0000H	8, 16
F0645H		RMDF7_1LH			
F0646H	RX message buffer data field 1 register 7 H	RMDF7_1HL	RMDF7_1H	0000H	8, 16
F0647H		RMDF7_1HH			
F0648H	RX message buffer data field 2 register 7 L	RMDF7_2LL	RMDF7_2L	0000H	8, 16
F0649H		RMDF7_2LH			
F064AH	RX message buffer data field 2 register 7 H	RMDF7_2HL	RMDF7_2H	0000H	8, 16
F064BH		RMDF7_2HH			
F064CH	RX message buffer data field 3 register 7 L	RMDF7_3LL	RMDF7_3L	0000H	8, 16
F064DH		RMDF7_3LH			
F064EH	RX message buffer data field 3 register 7 H	RMDF7_3HL	RMDF7_3H	0000H	8, 16
F064FH		RMDF7_3HH			
F0650H	RX message buffer data field 4 register 7 L	RMDF7_4LL	RMDF7_4L	0000H	8, 16
F0651H		RMDF7_4LH			
F0652H	RX message buffer data field 4 register 7 H	RMDF7_4HL	RMDF7_4H	0000H	8, 16
F0653H		RMDF7_4HH			
F0654H	RX message buffer data field 5 register 7 L	RMDF7_5LL	RMDF7_5L	0000H	8, 16
F0655H		RMDF7_5LH			
F0656H	RX message buffer data field 5 register 7 H	RMDF7_5HL	RMDF7_5H	0000H	8, 16
F0657H		RMDF7_5HH			
F0658H	RX message buffer data field 6 register 7 L	RMDF7_6LL	RMDF7_6L	0000H	8, 16
F0659H		RMDF7_6LH			
F065AH	RX message buffer data field 6 register 7 H	RMDF7_6HL	RMDF7_6H	0000H	8, 16
F065BH		RMDF7_6HH			
F065CH	RX message buffer data field 7 register 7 L	RMDF7_7LL	RMDF7_7L	0000H	8, 16
F065DH		RMDF7_7LH			
F065EH	RX message buffer data field 7 register 7 H	RMDF7_7HL	RMDF7_7H	0000H	8, 16
F065FH		RMDF7_7HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-3. List of RS-CANFD lite Window Registers for RL78/F24 (Page.2) (13/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0660H	RX message buffer data field 8 register 7 L	RMDF7_8LL	RMDF7_8L	0000H	8, 16
F0661H		RMDF7_8LH			
F0662H	RX message buffer data field 8 register 7 H	RMDF7_8HL	RMDF7_8H	0000H	8, 16
F0663H		RMDF7_8HH			
F0664H	RX message buffer data field 9 register 7 L	RMDF7_9LL	RMDF7_9L	0000H	8, 16
F0665H		RMDF7_9LH			
F0666H	RX message buffer data field 9 register 7 H	RMDF7_9HL	RMDF7_9H	0000H	8, 16
F0667H		RMDF7_9HH			
F0668H	RX message buffer data field 10 register 7 L	RMDF7_10LL	RMDF7_10L	0000H	8, 16
F0669H		RMDF7_10LH			
F066AH	RX message buffer data field 10 register 7 H	RMDF7_10HL	RMDF7_10H	0000H	8, 16
F066BH		RMDF7_10HH			
F066CH	RX message buffer data field 11 register 7 L	RMDF7_11LL	RMDF7_11L	0000H	8, 16
F066DH		RMDF7_11LH			
F066EH	RX message buffer data field 11 register 7 H	RMDF7_11HL	RMDF7_11H	0000H	8, 16
F066FH		RMDF7_11HH			
F0670H	RX message buffer data field 12 register 7 L	RMDF7_12LL	RMDF7_12L	0000H	8, 16
F0671H		RMDF7_12LH			
F0672H	RX message buffer data field 12 register 7 H	RMDF7_12HL	RMDF7_12H	0000H	8, 16
F0673H		RMDF7_12HH			
F0674H	RX message buffer data field 13 register 7 L	RMDF7_13LL	RMDF7_13L	0000H	8, 16
F0675H		RMDF7_13LH			
F0676H	RX message buffer data field 13 register 7 H	RMDF7_13HL	RMDF7_13H	0000H	8, 16
F0677H		RMDF7_13HH			
F0678H	RX message buffer data field 14 register 7 L	RMDF7_14LL	RMDF7_14L	0000H	8, 16
F0679H		RMDF7_14LH			
F067AH	RX message buffer data field 14 register 7 H	RMDF7_14HL	RMDF7_14H	0000H	8, 16
F067BH		RMDF7_14HH			
F067CH	RX message buffer data field 15 register 7 L	RMDF7_15LL	RMDF7_15L	0000H	8, 16
F067DH		RMDF7_15LH			
F067EH	RX message buffer data field 15 register 7 H	RMDF7_15HL	RMDF7_15H	0000H	8, 16
F067FH		RMDF7_15HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 10B (page.2 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (1/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0420H	RX message buffer ID register 8 L	RMID8LL	RMID8L	0000H	8, 16
F0421H		RMID8LH			
F0422H	RX message buffer ID register 8 H	RMID8HL	RMID8H	0000H	8, 16
F0423H		RMID8HH			
F0424H	RX message buffer pointer register 8 L	RMPTR8LL	RMPTR8L	0000H	8, 16
F0425H		RMPTR8LH			
F0426H	RX message buffer pointer register 8 H	—	RMPTR8H	0000H	8, 16
F0427H		RMPTR8HH			
F0428H	RX message buffer CAN-FD status register 8 L	RMFDSTS8LL	RMFDSTS8L	0000H	8, 16
F0429H		RMFDSTS8LH			
F042AH	RX message buffer CAN-FD status register 8 H	RMFDSTS8HL	RMFDSTS8H	0000H	8, 16
F042BH		RMFDSTS8HH			
F042CH	RX message buffer data field 0 register 8 L	RMDF8_0LL	RMDF8_0L	0000H	8, 16
F042DH		RMDF8_0LH			
F042EH	RX message buffer data field 0 register 8 H	RMDF8_0HL	RMDF8_0H	0000H	8, 16
F042FH		RMDF8_0HH			
F0430H	RX message buffer data field 1 register 8 L	RMDF8_1LL	RMDF8_1L	0000H	8, 16
F0431H		RMDF8_1LH			
F0432H	RX message buffer data field 1 register 8 H	RMDF8_1HL	RMDF8_1H	0000H	8, 16
F0433H		RMDF8_1HH			
F0434H	RX message buffer data field 2 register 8 L	RMDF8_2LL	RMDF8_2L	0000H	8, 16
F0435H		RMDF8_2LH			
F0436H	RX message buffer data field 2 register 8 H	RMDF8_2HL	RMDF8_2H	0000H	8, 16
F0437H		RMDF8_2HH			
F0438H	RX message buffer data field 3 register 8 L	RMDF8_3LL	RMDF8_3L	0000H	8, 16
F0439H		RMDF8_3LH			
F043AH	RX message buffer data field 3 register 8 H	RMDF8_3HL	RMDF8_3H	0000H	8, 16
F043BH		RMDF8_3HH			
F043CH	RX message buffer data field 4 register 8 L	RMDF8_4LL	RMDF8_4L	0000H	8, 16
F043DH		RMDF8_4LH			
F043EH	RX message buffer data field 4 register 8 H	RMDF8_4HL	RMDF8_4H	0000H	8, 16
F043FH		RMDF8_4HH			
F0440H	RX message buffer data field 5 register 8 L	RMDF8_5LL	RMDF8_5L	0000H	8, 16
F0441H		RMDF8_5LH			
F0442H	RX message buffer data field 5 register 8 H	RMDF8_5HL	RMDF8_5H	0000H	8, 16
F0443H		RMDF8_5HH			
F0444H	RX message buffer data field 6 register 8 L	RMDF8_6LL	RMDF8_6L	0000H	8, 16
F0445H		RMDF8_6LH			
F0446H	RX message buffer data field 6 register 8 H	RMDF8_6HL	RMDF8_6H	0000H	8, 16
F0447H		RMDF8_6HH			
F0448H	RX message buffer data field 7 register 8 L	RMDF8_7LL	RMDF8_7L	0000H	8, 16
F0449H		RMDF8_7LH			
F044AH	RX message buffer data field 7 register 8 H	RMDF8_7HL	RMDF8_7H	0000H	8, 16
F044BH		RMDF8_7HH			
F044CH	RX message buffer data field 8 register 8 L	RMDF8_8LL	RMDF8_8L	0000H	8, 16
F044DH		RMDF8_8LH			
F044EH	RX message buffer data field 8 register 8 H	RMDF8_8HL	RMDF8_8H	0000H	8, 16
F044FH		RMDF8_8HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (2/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0450H	RX message buffer data field 9 register 8 L	RMDF8_9LL	RMDF8_9L	0000H	8, 16
F0451H		RMDF8_9LH			
F0452H	RX message buffer data field 9 register 8 H	RMDF8_9HL	RMDF8_9H	0000H	8, 16
F0453H		RMDF8_9HH			
F0454H	RX message buffer data field 10 register 8 L	RMDF8_10LL	RMDF8_10L	0000H	8, 16
F0455H		RMDF8_10LH			
F0456H	RX message buffer data field 10 register 8 H	RMDF8_10HL	RMDF8_10H	0000H	8, 16
F0457H		RMDF8_10HH			
F0458H	RX message buffer data field 11 register 8 L	RMDF8_11LL	RMDF8_11L	0000H	8, 16
F0459H		RMDF8_11LH			
F045AH	RX message buffer data field 11 register 8 H	RMDF8_11HL	RMDF8_11H	0000H	8, 16
F045BH		RMDF8_11HH			
F045CH	RX message buffer data field 12 register 8 L	RMDF8_12LL	RMDF8_12L	0000H	8, 16
F045DH		RMDF8_12LH			
F045EH	RX message buffer data field 12 register 8 H	RMDF8_12HL	RMDF8_12H	0000H	8, 16
F045FH		RMDF8_12HH			
F0460H	RX message buffer data field 13 register 8 L	RMDF8_13LL	RMDF8_13L	0000H	8, 16
F0461H		RMDF8_13LH			
F0462H	RX message buffer data field 13 register 8 H	RMDF8_13HL	RMDF8_13H	0000H	8, 16
F0463H		RMDF8_13HH			
F0464H	RX message buffer data field 14 register 8 L	RMDF8_14LL	RMDF8_14L	0000H	8, 16
F0465H		RMDF8_14LH			
F0466H	RX message buffer data field 14 register 8 H	RMDF8_14HL	RMDF8_14H	0000H	8, 16
F0467H		RMDF8_14HH			
F0468H	RX message buffer data field 15 register 8 L	RMDF8_15LL	RMDF8_15L	0000H	8, 16
F0469H		RMDF8_15LH			
F046AH	RX message buffer data field 15 register 8 H	RMDF8_15HL	RMDF8_15H	0000H	8, 16
F046BH		RMDF8_15HH			
F046CH	RX message buffer ID register 9 L	RMID9LL	RMID9L	0000H	8, 16
F046DH		RMID9LH			
F046EH	RX message buffer ID register 9 H	RMID9HL	RMID9H	0000H	8, 16
F046FH		RMID9HH			
F0470H	RX message buffer pointer register 9 L	RMPTR9LL	RMPTR9L	0000H	8, 16
F0471H		RMPTR9LH			
F0472H	RX message buffer pointer register 9 H	—	RMPTR9H	0000H	8, 16
F0473H		RMPTR9HH			
F0474H	RX message buffer CAN-FD status register 9 L	RMFDSTS9LL	RMFDSTS9L	0000H	8, 16
F0475H		RMFDSTS9LH			
F0476H	RX message buffer CAN-FD status register 9 H	RMFDSTS9HL	RMFDSTS9H	0000H	8, 16
F0477H		RMFDSTS9HH			
F0478H	RX message buffer data field 0 register 9 L	RMDF9_0LL	RMDF9_0L	0000H	8, 16
F0479H		RMDF9_0LH			
F047AH	RX message buffer data field 0 register 9 H	RMDF9_0HL	RMDF9_0H	0000H	8, 16
F047BH		RMDF9_0HH			
F047CH	RX message buffer data field 1 register 9 L	RMDF9_1LL	RMDF9_1L	0000H	8, 16
F047DH		RMDF9_1LH			
F047EH	RX message buffer data field 1 register 9 H	RMDF9_1HL	RMDF9_1H	0000H	8, 16
F047FH		RMDF9_1HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (3/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0480H	RX message buffer data field 2 register 9 L	RMDF9_2LL	RMDF9_2L	0000H	8, 16
F0481H		RMDF9_2LH			
F0482H	RX message buffer data field 2 register 9 H	RMDF9_2HL	RMDF9_2H	0000H	8, 16
F0483H		RMDF9_2HH			
F0484H	RX message buffer data field 3 register 9 L	RMDF9_3LL	RMDF9_3L	0000H	8, 16
F0485H		RMDF9_3LH			
F0486H	RX message buffer data field 3 register 9 H	RMDF9_3HL	RMDF9_3H	0000H	8, 16
F0487H		RMDF9_3HH			
F0488H	RX message buffer data field 4 register 9 L	RMDF9_4LL	RMDF9_4L	0000H	8, 16
F0489H		RMDF9_4LH			
F048AH	RX message buffer data field 4 register 9 H	RMDF9_4HL	RMDF9_4H	0000H	8, 16
F048BH		RMDF9_4HH			
F048CH	RX message buffer data field 5 register 9 L	RMDF9_5LL	RMDF9_5L	0000H	8, 16
F048DH		RMDF9_5LH			
F048EH	RX message buffer data field 5 register 9 H	RMDF9_5HL	RMDF9_5H	0000H	8, 16
F048FH		RMDF9_5HH			
F0490H	RX message buffer data field 6 register 9 L	RMDF9_6LL	RMDF9_6L	0000H	8, 16
F0491H		RMDF9_6LH			
F0492H	RX message buffer data field 6 register 9 H	RMDF9_6HL	RMDF9_6H	0000H	8, 16
F0493H		RMDF9_6HH			
F0494H	RX message buffer data field 7 register 9 L	RMDF9_7LL	RMDF9_7L	0000H	8, 16
F0495H		RMDF9_7LH			
F0496H	RX message buffer data field 7 register 9 H	RMDF9_7HL	RMDF9_7H	0000H	8, 16
F0497H		RMDF9_7HH			
F0498H	RX message buffer data field 8 register 9 L	RMDF9_8LL	RMDF9_8L	0000H	8, 16
F0499H		RMDF9_8LH			
F049AH	RX message buffer data field 8 register 9 H	RMDF9_8HL	RMDF9_8H	0000H	8, 16
F049BH		RMDF9_8HH			
F049CH	RX message buffer data field 9 register 9 L	RMDF9_9LL	RMDF9_9L	0000H	8, 16
F049DH		RMDF9_9LH			
F049EH	RX message buffer data field 9 register 9 H	RMDF9_9HL	RMDF9_9H	0000H	8, 16
F049FH		RMDF9_9HH			
F04A0H	RX message buffer data field 10 register 9 L	RMDF9_10LL	RMDF9_10L	0000H	8, 16
F04A1H		RMDF9_10LH			
F04A2H	RX message buffer data field 10 register 9 H	RMDF9_10HL	RMDF9_10H	0000H	8, 16
F04A3H		RMDF9_10HH			
F04A4H	RX message buffer data field 11 register 9 L	RMDF9_11LL	RMDF9_11L	0000H	8, 16
F04A5H		RMDF9_11LH			
F04A6H	RX message buffer data field 11 register 9 H	RMDF9_11HL	RMDF9_11H	0000H	8, 16
F04A7H		RMDF9_11HH			
F04A8H	RX message buffer data field 12 register 9 L	RMDF9_12LL	RMDF9_12L	0000H	8, 16
F04A9H		RMDF9_12LH			
F04AAH	RX message buffer data field 12 register 9 H	RMDF9_12HL	RMDF9_12H	0000H	8, 16
F04ABH		RMDF9_12HH			
F04ACH	RX message buffer data field 13 register 9 L	RMDF9_13LL	RMDF9_13L	0000H	8, 16
F04ADH		RMDF9_13LH			
F04AEH	RX message buffer data field 13 register 9 H	RMDF9_13HL	RMDF9_13H	0000H	8, 16
F04AFH		RMDF9_13HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (4/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04B0H	RX message buffer data field 14 register 9 L	RMDF9_14LL	RMDF9_14L	0000H	8, 16
F04B1H		RMDF9_14LH			
F04B2H	RX message buffer data field 14 register 9 H	RMDF9_14HL	RMDF9_14H	0000H	8, 16
F04B3H		RMDF9_14HH			
F04B4H	RX message buffer data field 15 register 9 L	RMDF9_15LL	RMDF9_15L	0000H	8, 16
F04B5H		RMDF9_15LH			
F04B6H	RX message buffer data field 15 register 9 H	RMDF9_15HL	RMDF9_15H	0000H	8, 16
F04B7H		RMDF9_15HH			
F04B8H	RX message buffer ID register 10 L	RMID10LL	RMID10L	0000H	8, 16
F04B9H		RMID10LH			
F04BAH	RX message buffer ID register 10 H	RMID10HL	RMID10H	0000H	8, 16
F04BBH		RMID10HH			
F04BCH	RX message buffer pointer register 10 L	RMPTR10LL	RMPTR10L	0000H	8, 16
F04BDH		RMPTR10LH			
F04BEH	RX message buffer pointer register 10 H	—	RMPTR10H	0000H	8, 16
F04BFH		RMPTR10HH			
F04C0H	RX message buffer CAN-FD status register 10 L	RMFDSTS10LL	RMFDSTS10L	0000H	8, 16
F04C1H		RMFDSTS10LH			
F04C2H	RX message buffer CAN-FD status register 10 H	RMFDSTS10HL	RMFDSTS10H	0000H	8, 16
F04C3H		RMFDSTS10HH			
F04C4H	RX message buffer data field 0 register 10 L	RMDF10_0LL	RMDF10_0L	0000H	8, 16
F04C5H		RMDF10_0LH			
F04C6H	RX message buffer data field 0 register 10 H	RMDF10_0HL	RMDF10_0H	0000H	8, 16
F04C7H		RMDF10_0HH			
F04C8H	RX message buffer data field 1 register 10 L	RMDF10_1LL	RMDF10_1L	0000H	8, 16
F04C9H		RMDF10_1LH			
F04CAH	RX message buffer data field 1 register 10 H	RMDF10_1HL	RMDF10_1H	0000H	8, 16
F04CBH		RMDF10_1HH			
F04CCH	RX message buffer data field 2 register 10 L	RMDF10_2LL	RMDF10_2L	0000H	8, 16
F04CDH		RMDF10_2LH			
F04CEH	RX message buffer data field 2 register 10 H	RMDF10_2HL	RMDF10_2H	0000H	8, 16
F04CFH		RMDF10_2HH			
F04D0H	RX message buffer data field 3 register 10 L	RMDF10_3LL	RMDF10_3L	0000H	8, 16
F04D1H		RMDF10_3LH			
F04D2H	RX message buffer data field 3 register 10 H	RMDF10_3HL	RMDF10_3H	0000H	8, 16
F04D3H		RMDF10_3HH			
F04D4H	RX message buffer data field 4 register 10 L	RMDF10_4LL	RMDF10_4L	0000H	8, 16
F04D5H		RMDF10_4LH			
F04D6H	RX message buffer data field 4 register 10 H	RMDF10_4HL	RMDF10_4H	0000H	8, 16
F04D7H		RMDF10_4HH			
F04D8H	RX message buffer data field 5 register 10 L	RMDF10_5LL	RMDF10_5L	0000H	8, 16
F04D9H		RMDF10_5LH			
F04DAH	RX message buffer data field 5 register 10 H	RMDF10_5HL	RMDF10_5H	0000H	8, 16
F04DBH		RMDF10_5HH			
F04DCH	RX message buffer data field 6 register 10 L	RMDF10_6LL	RMDF10_6L	0000H	8, 16
F04DDH		RMDF10_6LH			
F04DEH	RX message buffer data field 6 register 10 H	RMDF10_6HL	RMDF10_6H	0000H	8, 16
F04DFH		RMDF10_6HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (5/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F04E0H	RX message buffer data field 7 register 10 L	RMDF10_7LL	RMDF10_7L	0000H	8, 16
F04E1H		RMDF10_7LH			
F04E2H	RX message buffer data field 7 register 10 H	RMDF10_7HL	RMDF10_7H	0000H	8, 16
F04E3H		RMDF10_7HH			
F04E4H	RX message buffer data field 8 register 10 L	RMDF10_8LL	RMDF10_8L	0000H	8, 16
F04E5H		RMDF10_8LH			
F04E6H	RX message buffer data field 8 register 10 H	RMDF10_8HL	RMDF10_8H	0000H	8, 16
F04E7H		RMDF10_8HH			
F04E8H	RX message buffer data field 9 register 10 L	RMDF10_9LL	RMDF10_9L	0000H	8, 16
F04E9H		RMDF10_9LH			
F04EAH	RX message buffer data field 9 register 10 H	RMDF10_9HL	RMDF10_9H	0000H	8, 16
F04EBH		RMDF10_9HH			
F04ECH	RX message buffer data field 10 register 10 L	RMDF10_10LL	RMDF10_10L	0000H	8, 16
F04EDH		RMDF10_10LH			
F04EEH	RX message buffer data field 10 register 10 H	RMDF10_10HL	RMDF10_10H	0000H	8, 16
F04EFH		RMDF10_10HH			
F04F0H	RX message buffer data field 11 register 10 L	RMDF10_11LL	RMDF10_11L	0000H	8, 16
F04F1H		RMDF10_11LH			
F04F2H	RX message buffer data field 11 register 10 H	RMDF10_11HL	RMDF10_11H	0000H	8, 16
F04F3H		RMDF10_11HH			
F04F4H	RX message buffer data field 12 register 10 L	RMDF10_12LL	RMDF10_12L	0000H	8, 16
F04F5H		RMDF10_12LH			
F04F6H	RX message buffer data field 12 register 10 H	RMDF10_12HL	RMDF10_12H	0000H	8, 16
F04F7H		RMDF10_12HH			
F04F8H	RX message buffer data field 13 register 10 L	RMDF10_13LL	RMDF10_13L	0000H	8, 16
F04F9H		RMDF10_13LH			
F04FAH	RX message buffer data field 13 register 10 H	RMDF10_13HL	RMDF10_13H	0000H	8, 16
F04FBH		RMDF10_13HH			
F04FCH	RX message buffer data field 14 register 10 L	RMDF10_14LL	RMDF10_14L	0000H	8, 16
F04FDH		RMDF10_14LH			
F04FEH	RX message buffer data field 14 register 10 H	RMDF10_14HL	RMDF10_14H	0000H	8, 16
F04FFH		RMDF10_14HH			
F0500H	RX message buffer data field 15 register 10 L	RMDF10_15LL	RMDF10_15L	0000H	8, 16
F0501H		RMDF10_15LH			
F0502H	RX message buffer data field 15 register 10 H	RMDF10_15HL	RMDF10_15H	0000H	8, 16
F0503H		RMDF10_15HH			
F0504H	RX message buffer ID register 11 L	RMID11LL	RMID11L	0000H	8, 16
F0505H		RMID11LH			
F0506H	RX message buffer ID register 11 H	RMID11HL	RMID11H	0000H	8, 16
F0507H		RMID11HH			
F0508H	RX message buffer pointer register 11 L	RMPTR11LL	RMPTR11L	0000H	8, 16
F0509H		RMPTR11LH			
F050AH	RX message buffer pointer register 11 H	—	RMPTR11H	0000H	8, 16
F050BH		RMPTR11HH			
F050CH	RX message buffer CAN-FD status register 11 L	RMFDSTS11LL	RMFDSTS11L	0000H	8, 16
F050DH		RMFDSTS11LH			
F050EH	RX message buffer CAN-FD status register 11 H	RMFDSTS11HL	RMFDSTS11H	0000H	8, 16
F050FH		RMFDSTS11HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (6/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0510H	RX message buffer data field 0 register 11 L	RMDF11_0LL	RMDF11_0L	0000H	8, 16
F0511H		RMDF11_0LH			
F0512H	RX message buffer data field 0 register 11 H	RMDF11_0HL	RMDF11_0H	0000H	8, 16
F0513H		RMDF11_0HH			
F0514H	RX message buffer data field 1 register 11 L	RMDF11_1LL	RMDF11_1L	0000H	8, 16
F0515H		RMDF11_1LH			
F0516H	RX message buffer data field 1 register 11 H	RMDF11_1HL	RMDF11_1H	0000H	8, 16
F0517H		RMDF11_1HH			
F0518H	RX message buffer data field 2 register 11 L	RMDF11_2LL	RMDF11_2L	0000H	8, 16
F0519H		RMDF11_2LH			
F051AH	RX message buffer data field 2 register 11 H	RMDF11_2HL	RMDF11_2H	0000H	8, 16
F051BH		RMDF11_2HH			
F051CH	RX message buffer data field 3 register 11 L	RMDF11_3LL	RMDF11_3L	0000H	8, 16
F051DH		RMDF11_3LH			
F051EH	RX message buffer data field 3 register 11 H	RMDF11_3HL	RMDF11_3H	0000H	8, 16
F051FH		RMDF11_3HH			
F0520H	RX message buffer data field 4 register 11 L	RMDF11_4LL	RMDF11_4L	0000H	8, 16
F0521H		RMDF11_4LH			
F0522H	RX message buffer data field 4 register 11 H	RMDF11_4HL	RMDF11_4H	0000H	8, 16
F0523H		RMDF11_4HH			
F0524H	RX message buffer data field 5 register 11 L	RMDF11_5LL	RMDF11_5L	0000H	8, 16
F0525H		RMDF11_5LH			
F0526H	RX message buffer data field 5 register 11 H	RMDF11_5HL	RMDF11_5H	0000H	8, 16
F0527H		RMDF11_5HH			
F0528H	RX message buffer data field 6 register 11 L	RMDF11_6LL	RMDF11_6L	0000H	8, 16
F0529H		RMDF11_6LH			
F052AH	RX message buffer data field 6 register 11 H	RMDF11_6HL	RMDF11_6H	0000H	8, 16
F052BH		RMDF11_6HH			
F052CH	RX message buffer data field 7 register 11 L	RMDF11_7LL	RMDF11_7L	0000H	8, 16
F052DH		RMDF11_7LH			
F052EH	RX message buffer data field 7 register 11 H	RMDF11_7HL	RMDF11_7H	0000H	8, 16
F052FH		RMDF11_7HH			
F0530H	RX message buffer data field 8 register 11 L	RMDF11_8LL	RMDF11_8L	0000H	8, 16
F0531H		RMDF11_8LH			
F0532H	RX message buffer data field 8 register 11 H	RMDF11_8HL	RMDF11_8H	0000H	8, 16
F0533H		RMDF11_8HH			
F0534H	RX message buffer data field 9 register 11 L	RMDF11_9LL	RMDF11_9L	0000H	8, 16
F0535H		RMDF11_9LH			
F0536H	RX message buffer data field 9 register 11 H	RMDF11_9HL	RMDF11_9H	0000H	8, 16
F0537H		RMDF11_9HH			
F0538H	RX message buffer data field 10 register 11 L	RMDF11_10LL	RMDF11_10L	0000H	8, 16
F0539H		RMDF11_10LH			
F053AH	RX message buffer data field 10 register 11 H	RMDF11_10HL	RMDF11_10H	0000H	8, 16
F053BH		RMDF11_10HH			
F053CH	RX message buffer data field 11 register 11 L	RMDF11_11LL	RMDF11_11L	0000H	8, 16
F053DH		RMDF11_11LH			
F053EH	RX message buffer data field 11 register 11 H	RMDF11_11HL	RMDF11_11H	0000H	8, 16
F053FH		RMDF11_11HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (7/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0540H	RX message buffer data field 12 register 11 L	RMDF11_12LL	RMDF11_12L	0000H	8, 16
F0541H		RMDF11_12LH			
F0542H	RX message buffer data field 12 register 11 H	RMDF11_12HL	RMDF11_12H	0000H	8, 16
F0543H		RMDF11_12HH			
F0544H	RX message buffer data field 13 register 11 L	RMDF11_13LL	RMDF11_13L	0000H	8, 16
F0545H		RMDF11_13LH			
F0546H	RX message buffer data field 13 register 11 H	RMDF11_13HL	RMDF11_13H	0000H	8, 16
F0547H		RMDF11_13HH			
F0548H	RX message buffer data field 14 register 11 L	RMDF11_14LL	RMDF11_14L	0000H	8, 16
F0549H		RMDF11_14LH			
F054AH	RX message buffer data field 14 register 11 H	RMDF11_14HL	RMDF11_14H	0000H	8, 16
F054BH		RMDF11_14HH			
F054CH	RX message buffer data field 15 register 11 L	RMDF11_15LL	RMDF11_15L	0000H	8, 16
F054DH		RMDF11_15LH			
F054EH	RX message buffer data field 15 register 11 H	RMDF11_15HL	RMDF11_15H	0000H	8, 16
F054FH		RMDF11_15HH			
F0550H	RX message buffer ID register 12 L	RMID12LL	RMID12L	0000H	8, 16
F0551H		RMID12LH			
F0552H	RX message buffer ID register 12 H	RMID12HL	RMID12H	0000H	8, 16
F0553H		RMID12HH			
F0554H	RX message buffer pointer register 12 L	RMPTR12LL	RMPTR12L	0000H	8, 16
F0555H		RMPTR12LH			
F0556H	RX message buffer pointer register 12 H	—	RMPTR12H	0000H	8, 16
F0557H		RMPTR12HH			
F0558H	RX message buffer CAN-FD status register 12 L	RMFDSTS12LL	RMFDSTS12L	0000H	8, 16
F0559H		RMFDSTS12LH			
F055AH	RX message buffer CAN-FD status register 12 H	RMFDSTS12HL	RMFDSTS12H	0000H	8, 16
F055BH		RMFDSTS12HH			
F055CH	RX message buffer data field 0 register 12 L	RMDF12_0LL	RMDF12_0L	0000H	8, 16
F055DH		RMDF12_0LH			
F055EH	RX message buffer data field 0 register 12 H	RMDF12_0HL	RMDF12_0H	0000H	8, 16
F055FH		RMDF12_0HH			
F0560H	RX message buffer data field 1 register 12 L	RMDF12_1LL	RMDF12_1L	0000H	8, 16
F0561H		RMDF12_1LH			
F0562H	RX message buffer data field 1 register 12 H	RMDF12_1HL	RMDF12_1H	0000H	8, 16
F0563H		RMDF12_1HH			
F0564H	RX message buffer data field 2 register 12 L	RMDF12_2LL	RMDF12_2L	0000H	8, 16
F0565H		RMDF12_2LH			
F0566H	RX message buffer data field 2 register 12 H	RMDF12_2HL	RMDF12_2H	0000H	8, 16
F0567H		RMDF12_2HH			
F0568H	RX message buffer data field 3 register 12 L	RMDF12_3LL	RMDF12_3L	0000H	8, 16
F0569H		RMDF12_3LH			
F056AH	RX message buffer data field 3 register 12 H	RMDF12_3HL	RMDF12_3H	0000H	8, 16
F056BH		RMDF12_3HH			
F056CH	RX message buffer data field 4 register 12 L	RMDF12_4LL	RMDF12_4L	0000H	8, 16
F056DH		RMDF12_4LH			
F056EH	RX message buffer data field 4 register 12 H	RMDF12_4HL	RMDF12_4H	0000H	8, 16
F056FH		RMDF12_4HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (8/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0570H	RX message buffer data field 5 register 12 L	RMDF12_5LL	RMDF12_5L	0000H	8, 16
F0571H		RMDF12_5LH			
F0572H	RX message buffer data field 5 register 12 H	RMDF12_5HL	RMDF12_5H	0000H	8, 16
F0573H		RMDF12_5HH			
F0574H	RX message buffer data field 6 register 12 L	RMDF12_6LL	RMDF12_6L	0000H	8, 16
F0575H		RMDF12_6LH			
F0576H	RX message buffer data field 6 register 12 H	RMDF12_6HL	RMDF12_6H	0000H	8, 16
F0577H		RMDF12_6HH			
F0578H	RX message buffer data field 7 register 12 L	RMDF12_7LL	RMDF12_7L	0000H	8, 16
F0579H		RMDF12_7LH			
F057AH	RX message buffer data field 7 register 12 H	RMDF12_7HL	RMDF12_7H	0000H	8, 16
F057BH		RMDF12_7HH			
F057CH	RX message buffer data field 8 register 12 L	RMDF12_8LL	RMDF12_8L	0000H	8, 16
F057DH		RMDF12_8LH			
F057EH	RX message buffer data field 8 register 12 H	RMDF12_8HL	RMDF12_8H	0000H	8, 16
F057FH		RMDF12_8HH			
F0580H	RX message buffer data field 9 register 12 L	RMDF12_9LL	RMDF12_9L	0000H	8, 16
F0581H		RMDF12_9LH			
F0582H	RX message buffer data field 9 register 12 H	RMDF12_9HL	RMDF12_9H	0000H	8, 16
F0583H		RMDF12_9HH			
F0584H	RX message buffer data field 10 register 12 L	RMDF12_10LL	RMDF12_10L	0000H	8, 16
F0585H		RMDF12_10LH			
F0586H	RX message buffer data field 10 register 12 H	RMDF12_10HL	RMDF12_10H	0000H	8, 16
F0587H		RMDF12_10HH			
F0588H	RX message buffer data field 11 register 12 L	RMDF12_11LL	RMDF12_11L	0000H	8, 16
F0589H		RMDF12_11LH			
F058AH	RX message buffer data field 11 register 12 H	RMDF12_11HL	RMDF12_11H	0000H	8, 16
F058BH		RMDF12_11HH			
F058CH	RX message buffer data field 12 register 12 L	RMDF12_12LL	RMDF12_12L	0000H	8, 16
F058DH		RMDF12_12LH			
F058EH	RX message buffer data field 12 register 12 H	RMDF12_12HL	RMDF12_12H	0000H	8, 16
F058FH		RMDF12_12HH			
F0590H	RX message buffer data field 13 register 12 L	RMDF12_13LL	RMDF12_13L	0000H	8, 16
F0591H		RMDF12_13LH			
F0592H	RX message buffer data field 13 register 12 H	RMDF12_13HL	RMDF12_13H	0000H	8, 16
F0593H		RMDF12_13HH			
F0594H	RX message buffer data field 14 register 12 L	RMDF12_14LL	RMDF12_14L	0000H	8, 16
F0595H		RMDF12_14LH			
F0596H	RX message buffer data field 14 register 12 H	RMDF12_14HL	RMDF12_14H	0000H	8, 16
F0597H		RMDF12_14HH			
F0598H	RX message buffer data field 15 register 12 L	RMDF12_15LL	RMDF12_15L	0000H	8, 16
F0599H		RMDF12_15LH			
F059AH	RX message buffer data field 15 register 12 H	RMDF12_15HL	RMDF12_15H	0000H	8, 16
F059BH		RMDF12_15HH			
F059CH	RX message buffer ID register 13 L	RMID13LL	RMID13L	0000H	8, 16
F059DH		RMID13LH			
F059EH	RX message buffer ID register 13 H	RMID13HL	RMID13H	0000H	8, 16
F059FH		RMID13HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (9/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05A0H	RX message buffer pointer register 13 L	RMPTR13LL	RMPTR13L	0000H	8, 16
F05A1H		RMPTR13LH			
F05A2H	RX message buffer pointer register 13 H	—	RMPTR13H	0000H	8, 16
F05A3H		RMPTR13HH			
F05A4H	RX message buffer CAN-FD status register 13 L	RMFDSTS13LL	RMFDSTS13L	0000H	8, 16
F05A5H		RMFDSTS13LH			
F05A6H	RX message buffer CAN-FD status register 13 H	RMFDSTS13HL	RMFDSTS13H	0000H	8, 16
F05A7H		RMFDSTS13HH			
F05A8H	RX message buffer data field 0 register 13 L	RMDF13_0LL	RMDF13_0L	0000H	8, 16
F05A9H		RMDF13_0LH			
F05AAH	RX message buffer data field 0 register 13 H	RMDF13_0HL	RMDF13_0H	0000H	8, 16
F05ABH		RMDF13_0HH			
F05ACH	RX message buffer data field 1 register 13 L	RMDF13_1LL	RMDF13_1L	0000H	8, 16
F05ADH		RMDF13_1LH			
F05AEH	RX message buffer data field 1 register 13 H	RMDF13_1HL	RMDF13_1H	0000H	8, 16
F05AFH		RMDF13_1HH			
F05B0H	RX message buffer data field 2 register 13 L	RMDF13_2LL	RMDF13_2L	0000H	8, 16
F05B1H		RMDF13_2LH			
F05B2H	RX message buffer data field 2 register 13 H	RMDF13_2HL	RMDF13_2H	0000H	8, 16
F05B3H		RMDF13_2HH			
F05B4H	RX message buffer data field 3 register 13 L	RMDF13_3LL	RMDF13_3L	0000H	8, 16
F05B5H		RMDF13_3LH			
F05B6H	RX message buffer data field 3 register 13 H	RMDF13_3HL	RMDF13_3H	0000H	8, 16
F05B7H		RMDF13_3HH			
F05B8H	RX message buffer data field 4 register 13 L	RMDF13_4LL	RMDF13_4L	0000H	8, 16
F05B9H		RMDF13_4LH			
F05BAH	RX message buffer data field 4 register 13 H	RMDF13_4HL	RMDF13_4H	0000H	8, 16
F05BBH		RMDF13_4HH			
F05BCH	RX message buffer data field 5 register 13 L	RMDF13_5LL	RMDF13_5L	0000H	8, 16
F05BDH		RMDF13_5LH			
F05BEH	RX message buffer data field 5 register 13 H	RMDF13_5HL	RMDF13_5H	0000H	8, 16
F05BFH		RMDF13_5HH			
F05C0H	RX message buffer data field 6 register 13 L	RMDF13_6LL	RMDF13_6L	0000H	8, 16
F05C1H		RMDF13_6LH			
F05C2H	RX message buffer data field 6 register 13 H	RMDF13_6HL	RMDF13_6H	0000H	8, 16
F05C3H		RMDF13_6HH			
F05C4H	RX message buffer data field 7 register 13 L	RMDF13_7LL	RMDF13_7L	0000H	8, 16
F05C5H		RMDF13_7LH			
F05C6H	RX message buffer data field 7 register 13 H	RMDF13_7HL	RMDF13_7H	0000H	8, 16
F05C7H		RMDF13_7HH			
F05C8H	RX message buffer data field 8 register 13 L	RMDF13_8LL	RMDF13_8L	0000H	8, 16
F05C9H		RMDF13_8LH			
F05CAH	RX message buffer data field 8 register 13 H	RMDF13_8HL	RMDF13_8H	0000H	8, 16
F05CBH		RMDF13_8HH			
F05CCH	RX message buffer data field 9 register 13 L	RMDF13_9LL	RMDF13_9L	0000H	8, 16
F05CDH		RMDF13_9LH			
F05CEH	RX message buffer data field 9 register 13 H	RMDF13_9HL	RMDF13_9H	0000H	8, 16
F05CFH		RMDF13_9HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (10/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F05D0H	RX message buffer data field 10 register 13 L	RMDF13_10LL	RMDF13_10L	0000H	8, 16
F05D1H		RMDF13_10LH			
F05D2H	RX message buffer data field 10 register 13 H	RMDF13_10HL	RMDF13_10H	0000H	8, 16
F05D3H		RMDF13_10HH			
F05D4H	RX message buffer data field 11 register 13 L	RMDF13_11LL	RMDF13_11L	0000H	8, 16
F05D5H		RMDF13_11LH			
F05D6H	RX message buffer data field 11 register 13 H	RMDF13_11HL	RMDF13_11H	0000H	8, 16
F05D7H		RMDF13_11HH			
F05D8H	RX message buffer data field 12 register 13 L	RMDF13_12LL	RMDF13_12L	0000H	8, 16
F05D9H		RMDF13_12LH			
F05DAH	RX message buffer data field 12 register 13 H	RMDF13_12HL	RMDF13_12H	0000H	8, 16
F05DBH		RMDF13_12HH			
F05DCH	RX message buffer data field 13 register 13 L	RMDF13_13LL	RMDF13_13L	0000H	8, 16
F05DDH		RMDF13_13LH			
F05DEH	RX message buffer data field 13 register 13 H	RMDF13_13HL	RMDF13_13H	0000H	8, 16
F05DFH		RMDF13_13HH			
F05E0H	RX message buffer data field 14 register 13 L	RMDF13_14LL	RMDF13_14L	0000H	8, 16
F05E1H		RMDF13_14LH			
F05E2H	RX message buffer data field 14 register 13 H	RMDF13_14HL	RMDF13_14H	0000H	8, 16
F05E3H		RMDF13_14HH			
F05E4H	RX message buffer data field 15 register 13 L	RMDF13_15LL	RMDF13_15L	0000H	8, 16
F05E5H		RMDF13_15LH			
F05E6H	RX message buffer data field 15 register 13 H	RMDF13_15HL	RMDF13_15H	0000H	8, 16
F05E7H		RMDF13_15HH			
F05E8H	RX message buffer ID register 14 L	RMID14LL	RMID14L	0000H	8, 16
F05E9H		RMID14LH			
F05EAH	RX message buffer ID register 14 H	RMID14HL	RMID14H	0000H	8, 16
F05EBH		RMID14HH			
F05ECH	RX message buffer pointer register 14 L	RMPTR14LL	RMPTR14L	0000H	8, 16
F05EDH		RMPTR14LH			
F05EEH	RX message buffer pointer register 14 H	—	RMPTR14H	0000H	8, 16
F05EFH		RMPTR14HH			
F05F0H	RX message buffer CAN-FD status register 14 L	RMFDSTS14LL	RMFDSTS14L	0000H	8, 16
F05F1H		RMFDSTS14LH			
F05F2H	RX message buffer CAN-FD status register 14 H	RMFDSTS14HL	RMFDSTS14H	0000H	8, 16
F05F3H		RMFDSTS14HH			
F05F4H	RX message buffer data field 0 register 14 L	RMDF14_0LL	RMDF14_0L	0000H	8, 16
F05F5H		RMDF14_0LH			
F05F6H	RX message buffer data field 0 register 14 H	RMDF14_0HL	RMDF14_0H	0000H	8, 16
F05F7H		RMDF14_0HH			
F05F8H	RX message buffer data field 1 register 14 L	RMDF14_1LL	RMDF14_1L	0000H	8, 16
F05F9H		RMDF14_1LH			
F05FAH	RX message buffer data field 1 register 14 H	RMDF14_1HL	RMDF14_1H	0000H	8, 16
F05FBH		RMDF14_1HH			
F05FCH	RX message buffer data field 2 register 14 L	RMDF14_2LL	RMDF14_2L	0000H	8, 16
F05FDH		RMDF14_2LH			
F05FEH	RX message buffer data field 2 register 14 H	RMDF14_2HL	RMDF14_2H	0000H	8, 16
F05FFH		RMDF14_2HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (11/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0600H	RX message buffer data field 3 register 14 L	RMDF14_3LL	RMDF14_3L	0000H	8, 16
F0601H		RMDF14_3LH			
F0602H	RX message buffer data field 3 register 14 H	RMDF14_3HL	RMDF14_3H	0000H	8, 16
F0603H		RMDF14_3HH			
F0604H	RX message buffer data field 4 register 14 L	RMDF14_4LL	RMDF14_4L	0000H	8, 16
F0605H		RMDF14_4LH			
F0606H	RX message buffer data field 4 register 14 H	RMDF14_4HL	RMDF14_4H	0000H	8, 16
F0607H		RMDF14_4HH			
F0608H	RX message buffer data field 5 register 14 L	RMDF14_5LL	RMDF14_5L	0000H	8, 16
F0609H		RMDF14_5LH			
F060AH	RX message buffer data field 5 register 14 H	RMDF14_5HL	RMDF14_5H	0000H	8, 16
F060BH		RMDF14_5HH			
F060CH	RX message buffer data field 6 register 14 L	RMDF14_6LL	RMDF14_6L	0000H	8, 16
F060DH		RMDF14_6LH			
F060EH	RX message buffer data field 6 register 14 H	RMDF14_6HL	RMDF14_6H	0000H	8, 16
F060FH		RMDF14_6HH			
F0610H	RX message buffer data field 7 register 14 L	RMDF14_7LL	RMDF14_7L	0000H	8, 16
F0611H		RMDF14_7LH			
F0612H	RX message buffer data field 7 register 14 H	RMDF14_7HL	RMDF14_7H	0000H	8, 16
F0613H		RMDF14_7HH			
F0614H	RX message buffer data field 8 register 14 L	RMDF14_8LL	RMDF14_8L	0000H	8, 16
F0615H		RMDF14_8LH			
F0616H	RX message buffer data field 8 register 14 H	RMDF14_8HL	RMDF14_8H	0000H	8, 16
F0617H		RMDF14_8HH			
F0618H	RX message buffer data field 9 register 14 L	RMDF14_9LL	RMDF14_9L	0000H	8, 16
F0619H		RMDF14_9LH			
F061AH	RX message buffer data field 9 register 14 H	RMDF14_9HL	RMDF14_9H	0000H	8, 16
F061BH		RMDF14_9HH			
F061CH	RX message buffer data field 10 register 14 L	RMDF14_10LL	RMDF14_10L	0000H	8, 16
F061DH		RMDF14_10LH			
F061EH	RX message buffer data field 10 register 14 H	RMDF14_10HL	RMDF14_10H	0000H	8, 16
F061FH		RMDF14_10HH			
F0620H	RX message buffer data field 11 register 14 L	RMDF14_11LL	RMDF14_11L	0000H	8, 16
F0621H		RMDF14_11LH			
F0622H	RX message buffer data field 11 register 14 H	RMDF14_11HL	RMDF14_11H	0000H	8, 16
F0623H		RMDF14_11HH			
F0624H	RX message buffer data field 12 register 14 L	RMDF14_12LL	RMDF14_12L	0000H	8, 16
F0625H		RMDF14_12LH			
F0626H	RX message buffer data field 12 register 14 H	RMDF14_12HL	RMDF14_12H	0000H	8, 16
F0627H		RMDF14_12HH			
F0628H	RX message buffer data field 13 register 14 L	RMDF14_13LL	RMDF14_13L	0000H	8, 16
F0629H		RMDF14_13LH			
F062AH	RX message buffer data field 13 register 14 H	RMDF14_13HL	RMDF14_13H	0000H	8, 16
F062BH		RMDF14_13HH			
F062CH	RX message buffer data field 14 register 14 L	RMDF14_14LL	RMDF14_14L	0000H	8, 16
F062DH		RMDF14_14LH			
F062EH	RX message buffer data field 14 register 14 H	RMDF14_14HL	RMDF14_14H	0000H	8, 16
F062FH		RMDF14_14HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (12/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0630H	RX message buffer data field 15 register 14 L	RMDF14_15LL	RMDF14_15L	0000H	8, 16
F0631H		RMDF14_15LH			
F0632H	RX message buffer data field 15 register 14 H	RMDF14_15HL	RMDF14_15H	0000H	8, 16
F0633H		RMDF14_15HH			
F0634H	RX message buffer ID register 15 L	RMID15LL	RMID15L	0000H	8, 16
F0635H		RMID15LH			
F0636H	RX message buffer ID register 15 H	RMID15HL	RMID15H	0000H	8, 16
F0637H		RMID15HH			
F0638H	RX message buffer pointer register 15 L	RMPTR15LL	RMPTR15L	0000H	8, 16
F0639H		RMPTR15LH			
F063AH	RX message buffer pointer register 15 H	—	RMPTR15H	0000H	8, 16
F063BH		RMPTR15HH			
F063CH	RX message buffer CAN-FD status register 15 L	RMFDSTS15LL	RMFDSTS15L	0000H	8, 16
F063DH		RMFDSTS15LH			
F063EH	RX message buffer CAN-FD status register 15 H	RMFDSTS15HL	RMFDSTS15H	0000H	8, 16
F063FH		RMFDSTS15HH			
F0640H	RX message buffer data field 0 register 15 L	RMDF15_0LL	RMDF15_0L	0000H	8, 16
F0641H		RMDF15_0LH			
F0642H	RX message buffer data field 0 register 15 H	RMDF15_0HL	RMDF15_0H	0000H	8, 16
F0643H		RMDF15_0HH			
F0644H	RX message buffer data field 1 register 15 L	RMDF15_1LL	RMDF15_1L	0000H	8, 16
F0645H		RMDF15_1LH			
F0646H	RX message buffer data field 1 register 15 H	RMDF15_1HL	RMDF15_1H	0000H	8, 16
F0647H		RMDF15_1HH			
F0648H	RX message buffer data field 2 register 15 L	RMDF15_2LL	RMDF15_2L	0000H	8, 16
F0649H		RMDF15_2LH			
F064AH	RX message buffer data field 2 register 15 H	RMDF15_2HL	RMDF15_2H	0000H	8, 16
F064BH		RMDF15_2HH			
F064CH	RX message buffer data field 3 register 15 L	RMDF15_3LL	RMDF15_3L	0000H	8, 16
F064DH		RMDF15_3LH			
F064EH	RX message buffer data field 3 register 15 H	RMDF15_3HL	RMDF15_3H	0000H	8, 16
F064FH		RMDF15_3HH			
F0650H	RX message buffer data field 4 register 15 L	RMDF15_4LL	RMDF15_4L	0000H	8, 16
F0651H		RMDF15_4LH			
F0652H	RX message buffer data field 4 register 15 H	RMDF15_4HL	RMDF15_4H	0000H	8, 16
F0653H		RMDF15_4HH			
F0654H	RX message buffer data field 5 register 15 L	RMDF15_5LL	RMDF15_5L	0000H	8, 16
F0655H		RMDF15_5LH			
F0656H	RX message buffer data field 5 register 15 H	RMDF15_5HL	RMDF15_5H	0000H	8, 16
F0657H		RMDF15_5HH			
F0658H	RX message buffer data field 6 register 15 L	RMDF15_6LL	RMDF15_6L	0000H	8, 16
F0659H		RMDF15_6LH			
F065AH	RX message buffer data field 6 register 15 H	RMDF15_6HL	RMDF15_6H	0000H	8, 16
F065BH		RMDF15_6HH			
F065CH	RX message buffer data field 7 register 15 L	RMDF15_7LL	RMDF15_7L	0000H	8, 16
F065DH		RMDF15_7LH			
F065EH	RX message buffer data field 7 register 15 H	RMDF15_7HL	RMDF15_7H	0000H	8, 16
F065FH		RMDF15_7HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

Table 4-4. List of RS-CANFD lite Window Registers for RL78/F24 (Page.3) (13/13)

Address	Register Name	Register Symbol		After Reset	Access Size [unit: bit]
F0660H	RX message buffer data field 8 register 15 L	RMDF15_8LL	RMDF15_8L	0000H	8, 16
F0661H		RMDF15_8LH			
F0662H	RX message buffer data field 8 register 15 H	RMDF15_8HL	RMDF15_8H	0000H	8, 16
F0663H		RMDF15_8HH			
F0664H	RX message buffer data field 9 register 15 L	RMDF15_9LL	RMDF15_9L	0000H	8, 16
F0665H		RMDF15_9LH			
F0666H	RX message buffer data field 9 register 15 H	RMDF15_9HL	RMDF15_9H	0000H	8, 16
F0667H		RMDF15_9HH			
F0668H	RX message buffer data field 10 register 15 L	RMDF15_10LL	RMDF15_10L	0000H	8, 16
F0669H		RMDF15_10LH			
F066AH	RX message buffer data field 10 register 15 H	RMDF15_10HL	RMDF15_10H	0000H	8, 16
F066BH		RMDF15_10HH			
F066CH	RX message buffer data field 11 register 15 L	RMDF15_11LL	RMDF15_11L	0000H	8, 16
F066DH		RMDF15_11LH			
F066EH	RX message buffer data field 11 register 15 H	RMDF15_11HL	RMDF15_11H	0000H	8, 16
F066FH		RMDF15_11HH			
F0670H	RX message buffer data field 12 register 15 L	RMDF15_12LL	RMDF15_12L	0000H	8, 16
F0671H		RMDF15_12LH			
F0672H	RX message buffer data field 12 register 15 H	RMDF15_12HL	RMDF15_12H	0000H	8, 16
F0673H		RMDF15_12HH			
F0674H	RX message buffer data field 13 register 15 L	RMDF15_13LL	RMDF15_13L	0000H	8, 16
F0675H		RMDF15_13LH			
F0676H	RX message buffer data field 13 register 15 H	RMDF15_13HL	RMDF15_13H	0000H	8, 16
F0677H		RMDF15_13HH			
F0678H	RX message buffer data field 14 register 15 L	RMDF15_14LL	RMDF15_14L	0000H	8, 16
F0679H		RMDF15_14LH			
F067AH	RX message buffer data field 14 register 15 H	RMDF15_14HL	RMDF15_14H	0000H	8, 16
F067BH		RMDF15_14HH			
F067CH	RX message buffer data field 15 register 15 L	RMDF15_15LL	RMDF15_15L	0000H	8, 16
F067DH		RMDF15_15LH			
F067EH	RX message buffer data field 15 register 15 H	RMDF15_15HL	RMDF15_15H	0000H	8, 16
F067FH		RMDF15_15HH			

Note CFDGRWC.RPAGE[1:0] bits are the condition of 11B (page.3 access selection).

Caution When the CAN0EN bit in the PER2 register is 0 or CAN RAM initialization has not been performed, the read value is undefined. When the CAN0EN bit is 1 and the initialization of the CAN RAM area is completed, the read value is the initial value listed above.

5. List of A/D Converter Window Registers for RL78/F23, F24

The table below lists the 12-bit A/D converter window registers for RL78/F23, F24 products.

Table 5-1. List of A/D Converter Window Registers for RL78/F23, F24 (Page.0)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D control register	ADCSR	0000H	16	√	√	√	√	√	√	√	√	√
F06B4H F06B5H	A/D channel select register A0	ADANSA0	0000H	16	√	√	√	√	√	√	√	√	√
F06B6H F06B7H	A/D channel select register A1	ADANSA1	0000H	16	√	√	√	√	√	√	√	√	√
F06B8H F06B9H	Addition/average function channel select register 0	ADADS0	0000H	16	√	√	√	√	√	√	√	√	√
F06BAH F06BBH	Addition/average function channel select register 1	ADADS1	0000H	16	√	√	√	√	√	√	√	√	√
F06BCH	Addition/average counter select register	ADADC	00H	1, 8	√	√	√	√	√	√	√	√	√
F06BEH F06BFH	A/D control expansion register	ADCER	0000H	16	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 0000B (page.0 access selection).

Table 5-2. List of A/D Converter Window Registers for RL78/F23, F24 (Page.1)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D start trigger select register	ADSTRGR	0000H	16	√	√	√	√	√	√	√	√	√
F06B2H F06B3H	A/D expansion input control register	ADEXICR	0000H	16	√	√	√	√	√	√	√	√	√
F06B4H F06B5H	A/D channel select register B0	ADANSB0	0000H	16	√	√	√	√	√	√	√	√	√
F06B6H F06B7H	A/D channel select register B1	ADANSB1	0000H	16	√	√	√	√	√	√	√	√	√
F06BCH F06BDH	A/D internal reference voltage data register	ADOCDR	0000H	16	√	√	√	√	√	√	√	√	√
F06BEH F06BFH	A/D self-test mode data register	ADRD	0000H	16	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 0001B (page.1 access selection).

Table 5-3. List of A/D Converter Window Registers for RL78/F23, F24 (Page.2)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D data register 0	ADDR0	0000H	16	√	√	√	√	√	√	√	√	√
F06B2H F06B3H	A/D data register 1	ADDR1	0000H	16	√	√	√	√	√	√	√	√	√
F06B4H F06B5H	A/D data register 2	ADDR2	0000H	16	√	√	√	√	√	√	√	√	√
F06B6H F06B7H	A/D data register 3	ADDR3	0000H	16	√	√	√	√	√	√	√	√	√
F06B8H F06B9H	A/D data register 4	ADDR4	0000H	16	√	√	√	√	√	√	√	√	√
F06BAH F06BBH	A/D data register 5	ADDR5	0000H	16	√	√	√	√	√	√	√	√	√
F06BCH F06BDH	A/D data register 6	ADDR6	0000H	16	√	√	√	√	√	√	√	√	√
F06BEH F06BFH	A/D data register 7	ADDR7	0000H	16	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 0010B (page.2 access selection).

Table 5-4. List of A/D Converter Window Registers for RL78/F23, F24 (Page.3)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D data register 8	ADDR8	0000H	16	√	√	√	√	—	√	√	√	—
F06B2H F06B3H	A/D data register 9	ADDR9	0000H	16	√	√	√	√	—	√	√	√	—
F06B4H F06B5H	A/D data register 10	ADDR10	0000H	16	√	√	√	√	—	√	√	√	—
F06B6H F06B7H	A/D data register 11	ADDR11	0000H	16	√	√	√	√	—	√	√	√	—
F06B8H F06B9H	A/D data register 12	ADDR12	0000H	16	√	√	√	√	—	√	√	√	—
F06BAH F06BBH	A/D data register 13	ADDR13	0000H	16	√	√	√	—	—	√	√	—	—
F06BCH F06BDH	A/D data register 14	ADDR14	0000H	16	√	√	√	—	—	√	√	—	—
F06BEH F06BFH	A/D data register 15	ADDR15	0000H	16	√	√	√	—	—	√	√	—	—

Note ADWINR.ADPAGE[3:0] bits are the condition of 0011B (page.3 access selection).

Table 5-5. List of A/D Converter Window Registers for RL78/F23, F24 (Page.4)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D data register 16	ADDR16	0000H	16	√	√	√	—	—	√	√	—	—
F06B2H F06B3H	A/D data register 17	ADDR17	0000H	16	√	√	—	—	—	√	—	—	—
F06B4H F06B5H	A/D data register 18	ADDR18	0000H	16	√	—	—	—	—	—	—	—	—
F06B6H F06B7H	A/D data register 19	ADDR19	0000H	16	√	—	—	—	—	—	—	—	—
F06B8H F06B9H	A/D data register 20	ADDR20	0000H	16	√	—	—	—	—	—	—	—	—
F06BAH F06BBH	A/D data register 21	ADDR21	0000H	16	√	—	—	—	—	—	—	—	—
F06BCH F06BDH	A/D data register 22	ADDR22	0000H	16	√	—	—	—	—	—	—	—	—
F06BEH F06BFH	A/D data register 23	ADDR23	0000H	16	√	—	—	—	—	—	—	—	—

Note ADWINR.ADPAGE[3:0] bits are the condition of 0100B (page.4 access selection).

Table 5-6. List of A/D Converter Window Registers for RL78/F23, F24 (Page.5)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D data register 24	ADDR24	0000H	16	√	√	√	√	√	√	√	√	√
F06B2H F06B3H	A/D data register 25	ADDR25	0000H	16	√	√	√	√	√	√	√	√	√
F06B4H F06B5H	A/D data register 26	ADDR26	0000H	16	√	√	√	√	—	√	√	√	—
F06B6H F06B7H	A/D data register 27	ADDR27	0000H	16	√	√	√	√	—	√	√	√	—
F06B8H F06B9H	A/D data register 28	ADDR28	0000H	16	√	√	√	√	—	√	√	√	—
F06BAH F06BBH	A/D data register 29	ADDR29	0000H	16	√	√	√	√	—	√	√	√	—
F06BCH F06BDH	A/D data register 30	ADDR30	0000H	16	√	√	√	—	—	√	√	—	—

Note ADWINR.ADPAGE[3:0] bits are the condition of 0101B (page.5 access selection).

Table 5-7. List of A/D Converter Window Registers for RL78/F23, F24 (Page.6)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B6H F06B7H	A/D sample-and-hold circuit control register	ADSHCR	001AH	16	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 0110B (page.6 access selection).

Table 5-8. List of A/D Converter Window Registers for RL78/F23, F24 (Page.7)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06BAH	A/D disconnection detection control register	ADDISCR	00H	8	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 0111B (page.7 access selection).

Table 5-9. List of A/D Converter Window Registers for RL78/F23, F24 (Page.8)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H F06B1H	A/D group scan priority control register	ADGSPCR	0000H	16	√	√	√	√	√	√	√	√	√
F06BAH	A/D high-/low-potential reference voltage control register	ADHVREFCNT	00H	1, 8	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 1000B (page.8 access selection).

Table 5-10. List of A/D Converter Window Registers for RL78/F23, F24 (Page.13)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06BDH	A/D sampling state register L (ANI16 to ANI30)	ADSSTRL	0DH	8	√	√	√	√	√	√	√	√	√
F06BFH	A/D sampling state register O (V_{BGR})	ADSSTRO	0DH	8	√	√	√	√	√	√	√	√	√

Note ADWINR.ADPAGE[3:0] bits are the condition of 1101B (page.13 access selection).

Table 5-11. List of A/D Converter Window Registers for RL78/F23, F24 (Page.14)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06B0H	A/D sampling state register 0	ADSSTR0	0DH	8	√	√	√	√	√	√	√	√	√
F06B1H	A/D sampling state register 1	ADSSTR1	0DH	8	√	√	√	√	√	√	√	√	√
F06B2H	A/D sampling state register 2	ADSSTR2	0DH	8	√	√	√	√	√	√	√	√	√
F06B3H	A/D sampling state register 3	ADSSTR3	0DH	8	√	√	√	√	√	√	√	√	√
F06B4H	A/D sampling state register 4	ADSSTR4	0DH	8	√	√	√	√	√	√	√	√	√
F06B5H	A/D sampling state register 5	ADSSTR5	0DH	8	√	√	√	√	√	√	√	√	√
F06B6H	A/D sampling state register 6	ADSSTR6	0DH	8	√	√	√	√	√	√	√	√	√
F06B7H	A/D sampling state register 7	ADSSTR7	0DH	8	√	√	√	√	√	√	√	√	√
F06B8H	A/D sampling state register 8	ADSSTR8	0DH	8	√	√	√	√	—	√	√	√	—
F06B9H	A/D sampling state register 9	ADSSTR9	0DH	8	√	√	√	√	—	√	√	√	—
F06BAH	A/D sampling state register 10	ADSSTR10	0DH	8	√	√	√	√	—	√	√	√	—
F06BBH	A/D sampling state register 11	ADSSTR11	0DH	8	√	√	√	√	—	√	√	√	—
F06BCH	A/D sampling state register 12	ADSSTR12	0DH	8	√	√	√	√	—	√	√	√	—
F06BDH	A/D sampling state register 13	ADSSTR13	0DH	8	√	√	√	—	—	√	√	—	—
F06BEH	A/D sampling state register 14	ADSSTR14	0DH	8	√	√	√	—	—	√	√	—	—
F06BFH	A/D sampling state register 15	ADSSTR15	0DH	8	√	√	√	—	—	√	√	—	—

Note ADWINR.ADPAGE[3:0] bits are the condition of 1110B (page.14 access selection).

6. List of LIN/UART Module Window Registers for RL78/F23, F24

The table below lists the LIN/UART module (RLIN3) window registers for RL78/F23, F24 products.

Table 6-1. List of LIN/UART Module Window Registers for RL78/F23, F24 (channel.0)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06C1H	LIN0 wake-up baud rate select register	LWBR0	00H	8	√	√	√	√	√	√	√	√	√
F06C2H	LIN/UART0 baud rate prescaler register	LBRP0	0000H	16	√	√	√	√	√	√	√	√	√
	LIN/UART0 baud rate prescaler 0 register	LBRP00		8									
F06C3H	LIN/UART0 baud rate prescaler 1 register	LBRP01		8									
F06C4H	LIN0 self-test control register	LSTC0	00H	8	√	√	√	√	√	√	√	√	√
F06C5H	UART0 stand-by control register	LUSC0	00H	8	√	√	√	√	√	√	√	√	√
F06C8H	LIN/UART0 mode register	LMD0	00H	8	√	√	√	√	√	√	√	√	√
F06C9H	LIN0 break field configuration register / UART0 configuration register	LBFC0	00H	8	√	√	√	√	√	√	√	√	√
F06CAH	LIN/UART0 space configuration register	LSC0	00H	8	√	√	√	√	√	√	√	√	√
F06CBH	LIN0 wake-up configuration register	LWUP0	00H	8	√	√	√	√	√	√	√	√	√
F06CCH	LIN0 interrupt enable register	LIE0	00H	8	√	√	√	√	√	√	√	√	√
F06CDH	LIN/UART0 error detection enable register	LEDE0	00H	8	√	√	√	√	√	√	√	√	√
F06CEH	LIN/UART0 control register	LCUC0	00H	8	√	√	√	√	√	√	√	√	√
F06D0H	LIN/UART0 transmission control register	LTRC0	00H	8	√	√	√	√	√	√	√	√	√
F06D1H	LIN/UART0 mode status register	LMST0	00H	8	√	√	√	√	√	√	√	√	√
F06D2H	LIN/UART0 status register	LST0	00H	8	√	√	√	√	√	√	√	—	—
F06D3H	LIN/UART0 error status register	LEST0	00H	8	√	√	√	√	√	√	√	√	√
F06D4H	LIN/UART0 data field configuration register	LDFC0	00H	8	√	√	√	√	√	√	√	√	√
F06D5H	LIN/UART0 ID buffer register	LIDB0	00H	8	√	√	√	√	√	√	√	√	√
F06D6H	LIN0 checksum buffer register	LCBR0	00H	8	√	√	√	√	√	√	√	√	√
F06D7H	UART0 data buffer 0 register	LUDB00	00H	8	√	√	√	√	√	√	√	√	√
F06D8H	LIN/UART0 data buffer 1 register	LDB01	00H	8	√	√	√	√	√	√	√	√	√
F06D9H	LIN/UART0 data buffer 2 register	LDB02	00H	8	√	√	√	√	√	√	√	√	√
F06DAH	LIN/UART0 data buffer 3 register	LDB03	00H	8	√	√	√	√	√	√	√	√	√
F06DBH	LIN/UART0 data buffer 4 register	LDB04	00H	8	√	√	√	√	√	√	√	√	√
F06DCH	LIN/UART0 data buffer 5 register	LDB05	00H	8	√	√	√	√	√	√	√	√	√
F06DDH	LIN/UART0 data buffer 6 register	LDB06	00H	8	√	√	√	√	√	√	√	√	√
F06DEH	LIN/UART0 data buffer 7 register	LDB07	00H	8	√	√	√	√	√	√	√	√	√
F06DFH	LIN/UART0 data buffer 8 register	LDB08	00H	8	√	√	√	√	√	√	√	√	√
F06E0H	UART0 operation enable register	LUOER0	00H	8	√	√	√	√	√	√	√	√	√
F06E1H	UART0 option register 1	LUOR01	00H	8	√	√	√	√	√	√	√	√	√
F06E4H	UART0 transmission data register	LUTDR0	0000H	16	√	√	√	√	√	√	√	√	√
		LUTDR0L		8									
F06E5H		LUTDR0H		8									
F06E6H	UART0 reception data register	LURDR0	0000H	16	√	√	√	√	√	√	√	√	√
		LURDR0L		8									
F06E7H		LURDR0H		8									
F06E8H	UART0 wait transmission data register	LUWTDR0	0000H	16	√	√	√	√	√	√	√	√	√
		LUWTDR0L		8									
F06E9H		LUWTDR0H		8									
F06ECH	LIN0 break and sync field detection status register	LBSS0	00H	8	√	√	√	√	√	√	√	√	√
F06EEH	LIN0 response space dominant signal detection status register	LRSS0	00H	8	√	√	√	√	√	√	√	√	√

Note LCHSEL.LSEL0 bit is the condition of 0 (channel.0 access selection).

Table 6-2. List of LIN/UART Module Window Registers for RL78/F24 (channel.1)

Address	Register Name	Register Symbol	After Reset	Access Size [unit: bit]	RL78/F24					RL78/F23			
					100-pin	80-pin	64-pin	48-pin	32-pin	80-pin	64-pin	48-pin	32-pin
F06C1H	LIN1 wake-up baud rate select register	LWBR1	00H	8	√	√	√	√	√	—	—	—	—
F06C2H	LIN/UART1 baud rate prescaler register	LBRP1	0000H	16	√	√	√	√	√	—	—	—	—
	LIN/UART1 baud rate prescaler 0 register	LBRP10		8									
F06C3H	LIN/UART1 baud rate prescaler 1 register	LBRP11		8									
F06C4H	LIN1 self-test control register	LSTC1	00H	8	√	√	√	√	√	—	—	—	—
F06C5H	UART1 stand-by control register	LUSC1	00H	8	√	√	√	√	√	—	—	—	—
F06C8H	LIN/UART1 mode register	LMD1	00H	8	√	√	√	√	√	—	—	—	—
F06C9H	LIN1 break field configuration register / UART1 configuration register	LBFC1	00H	8	√	√	√	√	√	—	—	—	—
F06CAH	LIN/UART1 space configuration register	LSC1	00H	8	√	√	√	√	√	—	—	—	—
F06CBH	LIN1 wake-up configuration register	LWUP1	00H	8	√	√	√	√	√	—	—	—	—
F06CCH	LIN1 interrupt enable register	LIE1	00H	8	√	√	√	√	√	—	—	—	—
F06CDH	LIN/UART1 error detection enable register	LEDE1	00H	8	√	√	√	√	√	—	—	—	—
F06CEH	LIN/UART1 control register	LCUC1	00H	8	√	√	√	√	√	—	—	—	—
F06D0H	LIN/UART1 transmission control register	LTRC1	00H	8	√	√	√	√	√	—	—	—	—
F06D1H	LIN/UART1 mode status register	LMST1	00H	8	√	√	√	√	√	—	—	—	—
F06D2H	LIN/UART1 status register	LST1	00H	8	√	√	√	√	√	—	—	—	—
F06D3H	LIN/UART1 error status register	LEST1	00H	8	√	√	√	√	√	—	—	—	—
F06D4H	LIN/UART1 data field configuration register	LDFC1	00H	8	√	√	√	√	√	—	—	—	—
F06D5H	LIN/UART1 ID buffer register	LIDB1	00H	8	√	√	√	√	√	—	—	—	—
F06D6H	LIN1 checksum buffer register	LCBR1	00H	8	√	√	√	√	√	—	—	—	—
F06D7H	UART1 data buffer 0 register	LUDB10	00H	8	√	√	√	√	√	—	—	—	—
F06D8H	LIN/UART1 data buffer 1 register	LDB11	00H	8	√	√	√	√	√	—	—	—	—
F06D9H	LIN/UART1 data buffer 2 register	LDB12	00H	8	√	√	√	√	√	—	—	—	—
F06DAH	LIN/UART1 data buffer 3 register	LDB13	00H	8	√	√	√	√	√	—	—	—	—
F06DBH	LIN/UART1 data buffer 4 register	LDB14	00H	8	√	√	√	√	√	—	—	—	—
F06DCH	LIN/UART1 data buffer 5 register	LDB15	00H	8	√	√	√	√	√	—	—	—	—
F06DDH	LIN/UART1 data buffer 6 register	LDB16	00H	8	√	√	√	√	√	—	—	—	—
F06DEH	LIN/UART1 data buffer 7 register	LDB17	00H	8	√	√	√	√	√	—	—	—	—
F06DFH	LIN/UART1 data buffer 8 register	LDB18	00H	8	√	√	√	√	√	—	—	—	—
F06E0H	UART1 operation enable register	LUOER1	00H	8	√	√	√	√	√	—	—	—	—
F06E1H	UART1 option register 1	LUOR11	00H	8	√	√	√	√	√	—	—	—	—
F06E4H	UART1 transmission data register	LUTDR1	0000H	16	√	√	√	√	√	—	—	—	—
		LUTDR1L		8									
F06E5H		LUTDR1H		8									
F06E6H	UART1 reception data register	LURDR1	0000H	16	√	√	√	√	√	—	—	—	—
		LURDR1L		8									
F06E7H		LURDR1H		8									
F06E8H	UART1 wait transmission data register	LUWTDR1	0000H	16	√	√	√	√	√	—	—	—	—
		LUWTDR1L		8									
F06E9H		LUWTDR1H		8									
F06ECH	LIN1 break and sync field detection status register	LBSS1	00H	8	√	√	√	√	√	—	—	—	—
F06EEH	LIN1 response space dominant signal detection status register	LRSS1	00H	8	√	√	√	√	√	—	—	—	—

Note LCHSEL.LSEL0 bit is the condition of 1 (channel.1 access selection).

7. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F23, F24 User's Manual: Hardware Rev. 1.00

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.09.30	-	First edition issued.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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