

Renesas Synergy<sup>™</sup> Platform

# Renesas Synergy<sup>™</sup> Platform Pin Configurator Usage

## Introduction

This application note describes how to use pin configurator for Renesas Synergy<sup>™</sup> Platform in e<sup>2</sup> studio or the IAR Embedded Workbench (IAR EW for Synergy).

### Objectives

The objective of this application note is to help users to be familiar with the procedure of configuring pins of the Synergy project by using the Pin Configurator of e<sup>2</sup> studio or IAR EW for Synergy.

#### **Required Resources**

The procedure in this application note applies to all Renesas Synergy<sup>™</sup> devices and development boards. Before following the procedure in this application note, make sure the following resources are available

- A PC running Microsoft® Windows® 7 or 10 with the following Renesas software installed:
- IAR EW for Synergy v8.23.3 or e<sup>2</sup> studio v7.3.0 (or later)
- Synergy Software Package (SSP) v1.6.0 or later
- Renesas Synergy<sup>™</sup> Standalone Configurator (SSC) v7.3.1 (only for IAR EW for Synergy)

You can download the required Renesas software and view the installation instruction from the Renesas Synergy<sup>™</sup> Platform (<u>https://www.renesassynergy.com</u>).

#### **Operating Environment**

Target devices	Development Kit for Renesas Synergy™ S7G2.
	Development Kit for Renesas Synergy™ S124.
	Development Kit for Renesas Synergy™ S3A7.
SSP	SSP v1.6.0 or later
IDE	e <sup>2</sup> studio v7.3.0 (or later) or IAR EW for Synergy v8.23.3
Toolchains	GNU ARM® Compiler GCC_7.2.1.20170904 (included in e <sup>2</sup> studio)
	IAR EW for Synergy



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## 1. Generating a Synergy Project

This chapter describes how to create a Synergy C project used for demonstrating the operation of pin configurator. If you already have a Synergy project, please skip to chapter 2.

#### **1.1** Generating a Synergy Project using e<sup>2</sup> studio

Invoke e<sup>2</sup> studio and launch a workspace. Select File → New → Synergy C Project to open the project creation wizard.

e <sup>2</sup>	workspace - e² studio	
File	Edit Source Refactor Navigate Search Project Renesa	s Views Run Window Help
	New Alt+Shift+N	Synergy C/C++ Project
	Open File	Makefile Project with Existing Code
<b>_</b>	Open Projects from File System	C/C++ Project
		📑 Project

#### Figure 1. New Synergy C Project

#### 2. Select Renesas Synergy C Executable Project and click Next.

All	Renesas Synergy C Executable Project	^
C/C++	RENESAS A C Executable Project for Renesas Synergy.	
	Renesas Synergy C Library Project RENESAS A C Library Project for Renesas Synergy.	
		~
	<	>

Figure 2. Project template



- 3. In the project creation wizard, input project information:
  - A. **Project name**: enter a name, for ex: **Pin\_Configurator\_Example**.
  - B. Use default location: Checked.
  - C. Toolchain: GCC ARM Embedded.
  - D. License: In case license file is not input:
    - a. Click Change license file to open the Synergy License dialogue box.
    - b. Click [...] button and browse to this location for license: {e<sup>2</sup> studio installed folder} \internal\projectgen\arm\licenses and select the license file in XML format. This license file is available only when SSP is installed.
  - E. Click the **Next** button to continue.

	rgy C Executable Project)	
ecify the new project details.		
oject	Toolchains	
roject name Pin_Configurator_Example	GCC ARM Embedded	
Use <u>d</u> efault location		
ocation: C:\Users\Vinh Loi\e2_studio\worksr	pace\Pin_ConfiguratorBrowse	
Choose file system: default ~		
Choose nie system, <b>derault</b>		
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cense icense file: C:\Renesas\Synergy\e2studio_v7.3.0_ssp_v1.6 icense Details: CUSTOMER INFORMATION:	6.0\internal\projectgen\arm\licenses\SSP_License_Example_Eva 6.0\internal\projectgen\arm\licenses\SSP_License_Example_Eval e = * * * projectgen > arm > licenses * * * Search licenses Organize * New folder Term 21	الله e _2013 م e modified 2/2019 4:40 PM

Figure 3. Synergy Project Creation Wizard



- 4. In the Device Selection dialog, input device and tool information:
  - A. Board: S7G2 DK
  - B. **Toolchain version**: Latest GNU compiler approved for use with Renesas Synergy. Currently 7.2.1.20170904
  - C. Other fields are kept as default as shown in the figure below.
  - D. Click **Next** button to continue.

2 studio - Proje	ct Configuration (Synergy C ct Configuration (Synergy apport that you require.	-			
(	0 52 DK =S7G27H2A01CBD	Board	Details		
Select Tools Toolchain: Toolchain version: Debugger:	GCC ARM Embedded 7.2.1.20170904 J-Link ARM		~	Available Tools GCC ARM Ember 7.2.1.201709 6.3.1.201706 4.9.3.201505 Debuggers J-Link ARM RTOS Express Logic Smart Manual IO Registers S Software Mar	04 20 29 : ThreadX
?		< <u>B</u> ack	<u>N</u> ext >	<u>F</u> inish	Cancel

#### Figure 4. Device Selection



#### 5. In the project templates dialog, select project type: **Blinky** and click **Finish** to create project.

	<ul> <li>Project Configuration (Synergy C Executable Project)</li> <li>type of project you wish to create.</li> </ul>	
roject Tei	nplate Selection	
0	BSP	-
	Base Board Support Package for the chosen Synergy family.	
	[Renesas.Synergy.1.6.0.pack]	
•	Blinky	
	Blinky project.	
	[Renesas.Synergy.1.6.0.pack]	
0	Blinky with ThreadX	
	Threaded version of Blinky project.	
	[Renesas.Synergy.1.6.0.pack]	
ode Gen	eration Settings	
_	nergy Code Formatter	

#### Figure 5. Project Templates

6. You may be prompted to open the Synergy Configuration perspective. Click **Yes** to open the perspective.

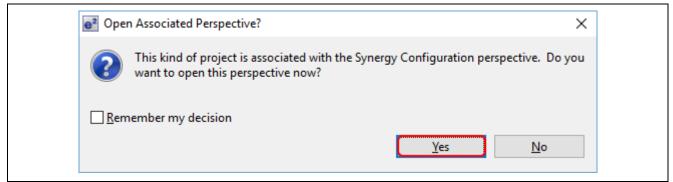


Figure 6. Open Synergy Configuration Perspective



# 7. New Synergy Project is successfully created and launched in Synergy Configuration perspective. There are 3 panes in this perspective: **Project Explorer**, **Synergy Configuration**, and **Package**.

Edit Navigate Search Project Renesas Views					
🛯 🏝 🏶 Debug 🛛 👋 Pin_Configurator	Exam > 0	2 0 6 0 / 0 0 + • • •	Province and a local distance of the		
			Quick Access	Debug Sn	nart Configurator 🙂 Synergy Configuration
Project Explorer 💠 🛛 🖻 🗞 🖤 😤	Pin_Configurator_Example] Synergy Configuration	on <sup>22</sup>	° 0	🗗 Package 🔤	Q Q ▼ <b>B</b> ▼ <b>M</b> ▼ °
Pin_Configurator_Example Solution of the second	Summary		Generate Project Content		3 4 5 6 7 8 9 10 11 303 VSS VSS P90S P911 VCC VLO VC1 P902
> e src > e synergy > e script > e synergy_cfg	Project Summary Board: S7G2 DK Device: R7FS7G27H2A01Cl	RD.		C P111 P110 P	301 VCC VCC 9312 P912 P200 VLO V55 P901 112 9304 9309 9310 9311 P201 P904 V58 P315 113 9305 9306 9307 9308 P910 9903 VCC 9204
configuration.xml     Pin_Configurator_Example Debug.launch     R7FS7G27H2A01CBD.pincfg     S7G2-DK.pincfg	Toolchain: GCC ARM Embedde Toolchain Version: 7.2.1.20170904 SSP Version: 1.6.0		S7G2	P P614 P612 P	115 P114 P014 P015 P008 P000 P000 P313 P414 113 P608 P300 P906 P907 ALS P314 P710 P712 A14 P609 PA12 PA11 PA08 P613 P206 P713 P807
⑦ Developer Assistance	Selected software components Board support package for R7FS7G27H Board support package for S7G2 Board support package for S7G2 Simple application that blinks an LED. N	v1.6.0 v1.6.0 o RTOS included v1.6.0		3 P407 P406 P 6 P605 P604 P 6 P602 P601 P	<ul> <li>C. Kalop Paki Paki Paki Paki Paki</li> <li>Peter Paki Paki Paki Paki Paki</li> <li>Peter Paki Paki Paki Paki Paki Paki</li> <li>Peter Paki Paki Paki Paki Paki Paki Paki</li> <li>Peter Paki Paki Paki Paki Paki Paki Paki Paki</li></ul>
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Properties 🖺 Problems 🏶 Smart Browser 🎞	◆当会 回算者 へ	Pin Conflicts			3.44
vice: R5F565NED(RX65N) Li	ist updated: 2019/05/22 at 16:44:32 ICT	0 items			
ontext Help User's Manual Technical Update Appli otal: 27	cation Notes Tool News Notifications	Description	^	Module	New Notification There are 6 new Tool Topics Hint There are 20 new Community New
Received Category Contents		Ĵ			LatesThere is 1 new Renesas News

Figure 7. New project opened in "Synergy Configuration" Perspective

## 1.2 Generating a Synergy Project using IAR EW for Synergy

1. In the IAR EW for Synergy menu, choose **Renesas Synergy**  $\rightarrow$  **New Synergy Project...** 

IAR Embedded Workbench	n IDE
File Edit View Project	Renesas Synergy Tools Window Help
1 🗅 🕒 🔛 🖓 🔚 🕹 🕹	⑦ Configurator ▼ < Q > 5 ► Ξ <
Workspace	Settings
	Export Synergy User Pack
Files	New Synergy Project

Figure 8. Create New Project



2. In the **Save Workspace As** dialog box that appears, choose a folder to save the workspace in and enter the workspace name: **MyWorkspace** and click **Save**.

← → → ↑ 📙 ≪ workspace → RESG_EWSYN	✓ O Search RESG_EWSYN
Organize 🔻 New folder	[≡≡ ▾ ?
<ul> <li>3D Objects</li> <li>Desktop</li> <li>Documents</li> <li>Downloads</li> <li>Music</li> <li>Pictures</li> </ul>	Date modified Type No items match your search.
Videos Local Disk (C:) Local Disk (E:)	
Network	
· ·	
File <u>n</u> ame: MyWorkspace Save as <u>t</u> ype: Workspace Files (*.eww)	~

Figure 9. Save Workspace

- 3. In the Renesas Synergy Settings dialog box that appears, specify:
  - A. Location where Renesas Synergy SSC/SSP is installed: C:\Renesas\Synergy\SSC\_[SSC version] (default installation folder).
  - B. License file: C:\Renesas\Synergy\SSC\_[SSC version]\internal\projectgen\arm\licenses
    - a. Note 1: The SSP license MUST be installed under the SSC\_[SSC version] folder.
    - b. Note 2: If the license is installed in e<sup>2</sup> studio, user may copy the [internal] folder of e<sup>2</sup> studio (C:\Renesas\e2studio \internal\projectgen\arm\Licenses) to the SSC [SSC version] folder.
  - C. Replace encrypted files with decrypted files: unchecked



C:\Renesas\Synergy\ssc_	v7.3.0_ssp_v1.6.0		~	   
License file:				
C:\Renesas\Synergy\ssc_	v7.3.0_ssp_v1.6.0\internal\p	projectgen\arm\licenses\SS	P_License_Exan ~	·]
License information:				
CUSTOMER INFORMAT Company: Renesas Elect UserName: Renesas Syn Email: noreply@renesas.c LICENSE INFORMATION Issued: 31/05/2018 SUPPORTED COMPONE	ionics America Inc. ergy Evaluation User iom I: INTS:			^
Component: Synergy BSF Permissions: Source=yes,	, Edit=yes,Save=yes,View=ye	es,Compile=yes		~

#### Figure 1-10 Renesas Synergy Settings

4. In the **Save As** dialog box that appears, choose a folder that save the project and enter the project name: **Pin\_Configurator\_Example** and click **Save**.

Save As		×
$\leftarrow$ $\rightarrow$ $\checkmark$ $\uparrow$ $\frown$ $\checkmark$ workspace $\rightarrow$ RESG_EWSYN $\rightarrow$	✓ Ö Search RESG_EWSYN	Q I
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🏪 Local Disk (C:)		
Local Disk (E:)		>
File <u>n</u> ame: Pin_Configurator_Example		~
Save as type: Project Files (*.ewp)		~
∧ Hide Folders	Save	Cancel

Figure 11. Save project



- 5. When the **Synergy Standalone Configurator** opens, specify:
  - A. SSP version: 1.6.0 or later
  - B. Board: S7G2 DK
  - C. Device: R7FS7G27H2A01CBD
  - D. Click Next

Device Select	ion			
SSP version:	1.6.0	~	Board Details	
Board:	S7G2 DK	$\sim$		
Device:	R7FS7G27H2A01CBD			

Figure 12. Device Selection

6. In the Project Template Selection, select Blinky. Click Finish.

	Standalone Configurator type of project you wish to create.			Y	
Project le	emplate Selection	enosen synergy i	arriny.		
	[Renesas.Synergy.1.6.0.pack]				1
•	Blinky Blinky project. [Renesas.Synergy.1.6.0.pack]				l
	Blinky with ThreadX				
	Threaded version of Blinky project.				
	IRenesas Superay 1.6.0 nackl				

Figure 13. Select project template



#### 7. The Synergy Standalone Configurator window will be launched.

Synergy Standalone Configurator										_	-			×
Help										0	1.000		_	
[Synergy Project] Synergy Configuration 🛛		- [		🗊 Pa	ickag	e			Q	•		•	Ab 🔻	- 0
Summary		Generate Project Conte	ent	A	1 P	2 3 302 P3	4 03 VS	5 VSS	6 P905	7 P911	8 VCC	9 VLO	10 VCL1	11 A
Project Summary	3	ENESAS	^				01 VCC							
-	-	Accelerate. Innovate. Differentiate.		c p	111 P	110 P1	12 P30	1 P309	P310	P311	P201	P904	VSS	P31!
Board: S7G2 DK Device: R7FS7G27H2A01CBD				D	/cc	SS P1	13 P30	5 P306	P307	P308	P910	P903	vcc	P204
Device: R7FS7G27H2A01CBD SSP Version: 1.6.0		C700		EP	610 P	611 P1	15 P11	4 P914	P915	P908	P909	P900	P313	P414
		57GZ		FP	614 P	612 P6	13 P60	3 P300	P906	P907	RES	P314	P710	P71:
Selected software components							14 P60				<u> </u>			_
Board support package for R7FS7G27H2A01CBD	v1.6.0			нν	(CL1 )	ss vo	C PAO	PA10	PA02	PA13	P913	РВ00	PB04	PBO
Board support package for S7G2	v1.6.0		~	зp	A07 P	406 PA	05 PA0	4 PA03	PA01	PAOO	¥ P703	P406	P704	PB0:
You Tube				кp	605 P	604 P6	03 P10	7 P607	P606	P808	P809	P515	P404	P70:
You lube Gallery Support				L	602 P	601 P6	00 P10	5 P811	P812	VCC	VSS	P007	P003	VSS
Summary BSP Clocks Pins Threads Messaging Components				м	vss N	CC P1	05 P80	1 P505	P506	P508	P015	P014	P010	P004 🗸
<			>	<										>
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Properties are not available.		Description		^						M	lodul	e		Pir
		<												>

Figure 14. Synergy Configurator

8. We will work with the above configurator later. For now, switch back to IAR EW for Synergy window. The Synergy project is generated successfully.

MyWorkspace - IAR Er	mbe	dde	d Workbench IDE - Arm 8.23.3		_		$\times$
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>P</u> roject <u>I</u>	<u>R</u> ene	esas	Synergy <u>J</u> -Link <u>T</u> ools <u>W</u> indow <u>H</u> el	p			
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Pin_Configurator_Exa							
Pin_Configurator_Example							
Ready							

Figure 15. Project is created

## 2. Launching Pin Configurator

This chapter describes how to launch the Pin Configurator using e<sup>2</sup> studio or IAR EW for Synergy.



## 2.1 Launching Pin Configurator using e<sup>2</sup> studio

- 1. In e<sup>2</sup> studio, double click the file Configuration.xml in Project Explorer to open the Synergy Configuration Editor.
- 2. When the **Synergy Configuration Editor** launches, the first page displayed is the **Summary** page. Click the **Pins** tab to open the **Pin Configurator** page.

Project Explorer 🎫 🛛 🖻 🎕 🗇 👻 =	□	• E	Package <sup>22</sup>	
<ul> <li>Pin_Configurator_Example</li> <li>Includes</li> </ul>	Pins Configuration	Generate Project Content	A P302 P303 VS	5 6 7 8 9 10 11 5 VSS P905 P911 VCC VL0 VCL P902
> @ src	Select pin configuration	Pins Tutorial 🛵 🔻 🔍	* P109 P108 P301 VO	C VCC 9312 P912 P200 VLO VSS P901
> 🐸 synergy > 😂 script	S7G2-DK.pincfg 🛛 🗸 🗹 Generate data: g_bsp_pin_cfg		C P111 P110 P112 P30	4 P309 P310 P311 P201 P904 VSS P315
> > synergy_cfg			0 VCC VSS P113 P30	15 P306 P307 P308 P910 P903 VCC P204
configuration.xml Pin_Configurator_Example Debug.launch	Pin Selection Pin Configuration		# P610 P611 P115 P11	4 P914 P915 P908 P909 P900 P313 P414
R7FS7G27H2A01CBD.pincfg	type filter text 🤐 🗑 🖻	- fr	P614 P612 P613 P60	B P300 P906 P907 RES P314 P710 P712
S7G2-DK.pincfg	Ports		1 P813 PA15 PA14 P60	P PA12 PA11 PA05 P615 P206 P713 P807
> ⑦ Developer Assistance	Peripherals     Other Pins		" VOLI VSS VCC PAG	9 PA10 PA02 PA13 P913 P800 P804 P806
	other Pins		1 PA07 PA06 PA05 PA0	H PA03 PA01 PA00 P703 P406 P704 P802
			# P605 P604 P603 P10	7 P607 P606 P808 P809 P515 P404 P702
				6 P811 P812 VCC VSS P007 P003 VSS
				H PS05 P506 P508 P015 P014 P010 P004
			-	1 P502 P507 P510 VREFL AVSS 0 P011 P008
	1000			13 P503 P509 VCC AVCC VREPL P006 P001
	Summary BSP Clocks Pins Threads Messaging Components		<	ning build Haran son is und magne

Figure 16. Launch Synergy Configuration Editor in e<sup>2</sup> studio

## 2.2 Launching Pin Configurator using IAR EW for Synergy

The Synergy Standalone configurator has been opened in step 8 of section 1.2.

If the configurator is closed, in the IAR EW for Synergy menu, choose **Renesas Synergy**  $\rightarrow$  **Configurator...** to open it again.

You can also click on the *icon* on the toolbar to open the configurator.

The East view Project	Rer	nesas Synergy J-Link Tools Wind			_	
🗅 🗅 😐 🕋 🔒 🕹 🖒 🗂	Ð	Configurator	< 📮 > 🕢 🖻 🔳 🔹 •	≡ 0 •	÷ 🔍 🕲 ;	Ŧ
Workspace	3	Settings				
Debug		Export Synergy User Pack				
Files		New Synergy Project				
Leg Source Files     Leg Source Files     Leg Soc     Synergy     Leg Output     Dutput     Din_Configurator_Exa						

Figure 17. Launch Synergy Configuration Editor in IAR EW for Synergy

When launching the Synergy Configuration Editor, the page displayed is the [Summary] page. Click the **Pins** tab to launch the **Pin Configurator** page.



Synergy Standalone Configurator										—				$\times$
Help														
[Synergy Project] Synergy Configuration 33			ā F	Packa	ge				00	2 -		▼ Ab		
Pins Configuration	Generate Project (	Content			2	3 P303 \	ir	5	6 P005	7 0011	8	9	i	1: /
Select pin configuration	Pins Tutorial	/2 - 副				P301 \								
S7G2-DK.pincfg			с	р́111	P110	́Р112 Р	304 P	9309	́Р310	р́311	P201	P904	VSS	P3:
			D	vcc	VSS	P113 P	305 P	9306	P307	P308	P910	P903	vcc	P2
Pin Selection Pin Configuration			E	P610	P611	P115 P	114 P	914	P915	P908	P909	P900	P313	¥
type filter text 🖉 🖪 🖻		Ê	F	P614	P612	P613 P	608 P	9300	P906	P907	RES	P314	P710	P7:
> - Ports			G	P813	PA15	PA14 P	609 P	PA12	PA11	PA08	P615	P206	P713	PB
> 🗸 Peripherals			н	VCL1	VSS	VCC P	A09 P	PA10	PA02	PA13	P913	PB00	PB04	PB
> Other Pins			3	PA07	PA06	PA05 P	A04 P	PA03	PA01	PA00	P703	¥ P406	P704	PB
			к	P605	P604	P603 P	107 P	P607	P606	P808	P809	P515	P404	¥ P7
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Summary BSP Clocks Pins Threads Messaging Components						P105 P		_						-
<		>	<	• 33	100	105	001	505	- 300	1300	1013	FUIT		>
🗆 Properties 🖹 Problems 📑 🤝	🗖 🗖 🎦 🔁 Pin Conflicts											≱	, v	- 6
	0 items													
Properties are not available.	Description		^							Мо	dule			Pir
,														
	<						_							3

Figure 18. Launch Pin page

## 3. Pin Configurator GUI

The **Pin Configurator** allows you to configure the pins in the Synergy project. The GUI of the **Pin Configurator** in e<sup>2</sup> studio and IAR EW for Synergy are the same. It consists of 4 main parts:

- 1. Select pin configuration
- 2. Pin Selection
- 3. Pin Configuration
- 4. Package

Pin_Configurator_Example	ole] Synergy Configuratior	33		•	Pack	age	88						9	•		. • 1	• •
Pins Configuration	ı		Generate Project Content		_	_		P304				_					
-				51	vcc	vss	P113	P305	P306 P	307 P3	08 P91	LO P903	vcc	P204	P413	P412	P411
Select pin configuration			Pins Tutorial 🆧 🔻 🛍	4	E P61	0 P611	P115	P114	P914 P	915 P9	08 P90	9 P900	P313	P414	P711	P709	P415
S7G2-DK.pincfg	✓ Generate of	lata: g_bsp_pin_cfg			F P61	P613	2 P613	P608	P300 P	906 P9	07 RE	S P314	P710	P712	VSS 1USBH	vccus	USBHS
				ן ו	P81	3 PA15	5 PA14	P609	PA12 PA	A11 PA	08 P61	15 P206	P713	P807	VSS 2USBH	USBHS	AVSSU
Pin Selection	Pin Configuration				va	ı vss	VCC	PA09	PA10 P/	A02 PA	13 P91	13 PB00	P804	P806	VCC	AVCCU	P213
<i>A</i>   🕀 E	8		e C		PAO	7 PA06	5 PA05	PA04	PA03 PA	A01 PA	00 P70	3 P406	P704	P802	P805	VSS	ксоит
> - Ports	Module name:	P300	^		K P60	5 P604	P603	P107	P607 P	606 P8	08 P80	09 P515	P404	P702	P803	PB01	VBAT
> < Peripherals	Symbolic Name:	JTAG_TCK			L P60	2 P601	P600	P106	P811 P	812 V	c vs	S P007	P003	VSS	vcc	P705	P706
> Other Pins	Comment:		0		• VSS	vcc	P105	P804		506 PS	08 P01	LS P014	P010	P004	P806	P405	P700
	Port Capabilities:	DEBUGO: SWCLK			P10	2 P103	P104	P501	9502 P	507 P5	10 VRE		P011	P008	P002	P400	P402
		DEBUGO: TCK GPT0: GTIOCA			P P10	1 P800	P810	P803	9503 P	509 V		C VREF	P006	P001	P807	P513	P514
		SPI1: SSL1			R P10	0 P801	P802	P500		a.2 V	SS VRE	FHVREF	H P009	P005	P000	P805	P512
	P300 Configuration		*	1	1	2	3	4	5	6 7	8	9	10	11	12	13	14

Figure 19. Pin Configurator GUI

The details and how to use each part of the Pin Configurator will be described in the following chapters.



## 4. How to use the Select pin configuration pane

The **Select pin configuration** pane is used to select the pin configuration file. A pin configuration file represents the setting for a specific Synergy device. When modifying the pin setting, the changes will be saved to the pin configuration file.

## 4.1 GUI Introduction

The **Select pin configuration** pane consists of the following components:

- 1. **configuration drop-down list**: allows you to select an existing pin-configuration file or create a new configuration file.
- 2. Generate data:
  - A. Checkbox: checked by default. Generate pin configuration to source code.
  - B. Text box: contains the name of the data structure to be generated for the pin-configuration. The default data structure g\_bsp\_pin\_cfg is necessary for the project as it defines initial pin configuration. Renaming will cause build error but adding new data structure is possible by following chapter 4.3.
- 3. **Pins Tutorial link**: open a tutorial video on web browser.
- 4. Select device button <sup>(2)</sup>: change the device of the pin configuration.
- 5. Import button 💾: import an existing (compatible) Pin Configuration into the Synergy project

Select pin configuration		Pins Tutorial ⁄ 🔻 🛍
S7G2-DK.pincfg 🗸 🗸 🗸	Generate data: g_bsp_pin_cfg	

#### Figure 20. Select pin configuration

## 4.2 Using Single Configuration file (default)

When a new Synergy project is created, a pincfg file for the selected device and the pincfg contained in the selected BSP will be generated. These pin-configuration files are named after the device name (R7FS7G27H2A01CBD.pincfg) and board name (S7G2-DK.pincfg).

In e<sup>2</sup> studio, they are displayed in the **Project Explorer** window.

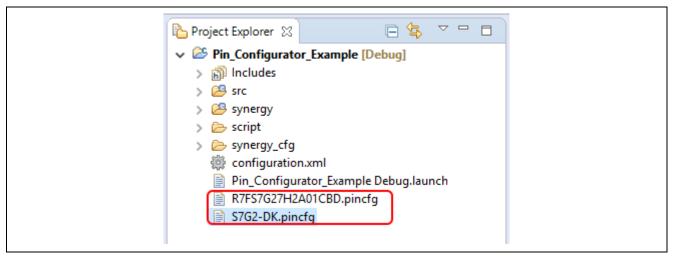


Figure 21. Pin configuration files in e<sup>2</sup> studio

In IAR EW for Synergy, the pin configuration files are not displayed in the **Workspace** window. To view them, open Windows Explorer and go to the project folder.



C » data (D:) » workspace » EWSYN »	
Name	Date modified
.module_descriptions	12/11/2016 9:20 PM
📜 .settings	12/11/2016 9:20 PM
📜 Debug	12/11/2016 9:20 PM
📕 script	12/11/2016 9:20 PM
📕 settings	12/11/2016 9:20 PM
📕 src	12/11/2016 9:20 PM
📕 synergy	12/11/2016 9:20 PM
synergy_cfg	12/11/2016 9:20 PM
🖹 buildinfo.xml	12/11/2016 8:53 PM
🖹 configuration.xml	12/11/2016 8:53 PM
MyWorkspace.custom_argvars	12/11/2016 9:13 PM
🔀 MyWorkspace.eww	12/11/2016 8:21 PM
Pin_Configurator_Example.dep	12/11/2016 8:23 PM
Pin_Configurator_Example.ewd	12/11/2016 8:23 PM
Pin_Configurator_Example.ewp	12/11/2016 8:23 PM
R7FS7G27H2A01CBD.pincfg	10/14/2016 1:11 AN
S7G2-DK.pincfg	12/11/2016 9:16 PM

#### Figure 22. Pin configuration files in IAR EW for Synergy

Normally, you can ignore the R7FS7G27H2A01CBD.pincfg and perform every pin configuration with S7G2-DK.pincfg.

Select pin configuration			
S7G2-DK.pincfg		Generate data: g_bsp_pin_cfg	
Select pin configuration			
R7FS7G27H2A01CBD.pincfg	~	Generate data:	

Figure 23. Only the S7G2-DK.pincfg is used

#### 4.3 Using Multiple Pin-Configuration files

A Synergy project usually only needs to use one pin-configuration file. However, in some applications, multiple pin configuration files are needed. It allows dynamic switching of pin configurations during run time, for example, for setting different power modes.

The multiple pin configurations will be created in different data structures. The following steps describe how to create a new pin configuration file manually.



- 1. Select **New default configuration...** in the configuration drop-down list to create a new configuration file.
- 2. Rename the newly created configuration file as you like.

Select pin configuration
S7G2-DK.pincfg   R7FS7G27H2A01CBD.pincfg   S7G2-DK.pincfg   onfiguration Onfiguration
e² New Default Pin Configuration       ×         New pin configuration name:       ×         NewName       ×         OK       Cancel

Figure 24. Create a new pin-configuration file

3. The new configuration file is automatically added to the Select pin configuration drop-down list.

Select pin configuration		Pins Tutorial 海 🔻 🛍
NewName.pincfg ~	Generate data: NewConfig	
R7FS7G27H2A01CBD.pincfg S7G2-DK.pincfg		
NewName.pincfg	nfiguration	
<new configuration="" default=""></new>		

#### Figure 25. New configuration file is added to the drop-down list

4. Select **NewName.pincfg** in the drop-down list and enter a unique name for it in the text box. For example: **NewConfig**.

Select pin configuration	
NewName.pincfg ~	Generate data: NewConfig

## Figure 26. Unique name for the new pin configuration

## 4.4 Importing a Pin Configuration

User can import an existing (compatible) pin configuration into a Synergy project. This is a 'partial' import, which means that the new setting will be merged to the current settings. The following steps describe how to use the import function.

1. Select a pin configuration file to import to. In this case, select the **NewName.pincfg** created in section 4.3.

Select pin configuration	
NewName.pincfg ~	Generate data: NewConfig

Figure 27. Select NewName.pincfg



2. Click on the button to open the Import Pin Configurations from File dialog

Select pin configuration		Pins Tutorial 🖧 🔻 🗟
NewName.pincfg ~	Generate data: NewConfig	

Figure 28. Click the Import button

- 3. Select file to import:
  - A. In e<sup>2</sup> studio, click on **Workspace...** to select file from user's workspace or click on **File System...** to select file from file system.
  - B. In IAR EW for Synergy, click on **File System...** to select file from file system.

In this example, click **File System...**, go to the Project Folder and select S7G2-DK.pincfg to import from it.

File:	
?     OK     Cancel     Workspace     F	ile System
e <sup>2</sup> Open	×
← → • ↑ 🖡 « work > Pin_Configurator_Ex • ひ	Search Pin_Configurator_Exam 👂
Organize • New folder	
∧     Name       > ≱ Quick access	Date modified
✓ SThis PC	5/22/2019 4:57 PM
synergy_erg	5/22/2019 4:57 PM
> 🔓 3D Objects 📄 NewName.pincfg	5/23/2019 4:08 PM 5/23/2019 1:53 PM
	J/ZJ/ZU13 1.JJ PIVI
Desktop     R7FS7G27H2A01CBD.pincfg     S7G2-DK pincfg	5/23/2019 1·59 PM
> Documents	5/23/2019 1:59 PM 5/23/2019 3:56 PM
CZC2 DK sin fr	
<ul> <li>Documents</li> <li>Downloads</li> <li>S7G2-DK.pincfg</li> <li>test.pincfg</li> </ul>	5/23/2019 3:56 PM

Figure 29. Import Setting from S7G2-DK.pincfg

4. Click OK. If there is no conflict, the settings of S7G2-DK.pincfg will be imported to NewName.pincfg.



- 5. If conflicts exist, the import function points out conflicts and provides the following options to the user:
  - A. Cancel the import operation
  - B. Ignore the conflicts and import the conflicting settings anyway
  - C. Continue the import operation without importing the conflicting settings.

e <sup>2</sup> Confl	icts found	_		×
	Conflicts were found while the import operation from file: S7G2-DK.pin	icfg.		
	Select one of the following options: Press Cancel to cancel the import operation. Press Ignore to continu the import operation; conflicting settings will be Press OK to continue the import operation; conflicting settings will not be			
	Cancel <u>I</u> gnore OK		<u>D</u> etails >	>

Figure 30. Conflicts found during the import process

### 4.5 Changing the selected device of Pin Configuration file

User can change the device in a pin configuration file. The following steps describe how to use this function.

1. Select a pin configuration file to change the device. In this case, select the **NewName.pincfg** created in section 4.3.

NewName.pincfg	Select pin configuration	
	NewName.pincfg ~	Generate data: NewConfig

Figure 31. Select pin configuration file



2. Click the device to open the drop-down list and select the desired device to change to. In this example, we change the device from renesas.s7g2\_bd to renesas.s7g2\_fc.

		👨 Pack	age 🖇	X							0, (	€ -		-	Ab 🔻		
0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Generate Project Cont	ent	A	P302	P303	VSS	VSS	P905	P911	vcc	VLO	VCL1	P902	P202	vccus	USBDP	P407	A
Pins Tutorial 🛵 🔻	<u>,</u>	B P109	P108	P301	vcc	vcc	P312	P912	P200	VLO	VSS	P901	P203	VSSUSE	USBDM	P408	в
	Renes	sas S124	>	112	P304	P309	P310	P311	P201	P904	VSS	P315	P205	P207	P409	P410	c
	Renes	as S128	>	113	P305	P306	P307	P308	P910	P903	vcc	P204	P413	P412	P411	P708	D
		sas S1JA	>	115	P114	P914	P915	P908	P909	P900	P313	P414	P711	P709	P415	vss	E
		sas S3A1	>	613	P608	¥300	P906	P907	RES	P314	P710	P712	VSS 1USBH	vccus	USBHS	извня	F
		sas S3A3 sas S3A6	>	A14	P609	PA12	PA11	PAGE	P615	P206	P713			í====	AVSSUS		1 I
		as S3A7	>	E -	PA09	PA10	PA02	PA13	P913	P800	P804	P806			P213	P212	i
	Renes	as S5D5	>	A05	PA04	PA03	PA01	PA00	P703	P406	P704	PB02	P805	VSS	хсолт	XCIN	3
	Renes	as S5D9	>	E									_	P801	VBAT	VCL	ĸ
✓	Renes	sas S7G2	>	~	ren	esas.	s7g2_	bd/r	enesa	s.224	bga						
_				t r	ren	esas.	s/g2	bg <b>r</b>	enesa	s.1/6	bga		-	P705	P706	P707	
		M VSS	VCC		ren	esas.	s7g2_	v re	nesa	s.144I	qfp			P405	P700	P701	м
		N P102	P103		ren	esas.	s7g2_	fc/re	nesas	.176l	qfp			P400	P402	P403	N
		P P101	P800	Ĩ			-	•	nesa					P513	P514	P401	P
		R P100	P801		ren	esas.	s7g2_	lk/re	nesas	.145lg	ga		t	P805	P512	P511	R
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	>				R	7FS7G	627xxx	oooxB	D - 22	24BG4	A (Top	o Viev	v)				

Figure 32. Change the selected device

3. The MCU package of the new device selected will be displayed in the **Package** view. Note: This change only affects the currently selected pin configuration. The device of other pin configurations remains unchanged.

In  $e^2$  studio, the **Package** view is opened by default in the **Synergy Configuration** perspective. If it is closed, select **Window**  $\rightarrow$  **Show** View  $\rightarrow$  **Pin Configurator**  $\rightarrow$  **Package** to open it.

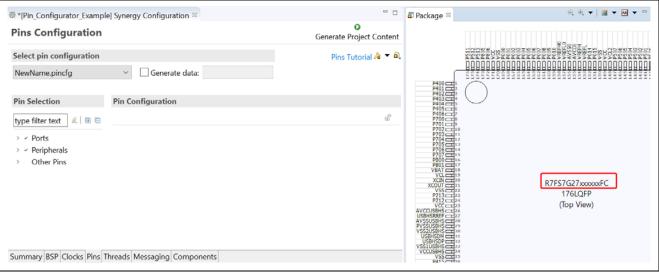


Figure 33. Package view is updated after changing device



- 4. If conflicts exist, the device changing function points out conflicts and provides the following options to the user:
  - A. Cancel the device changing operation.
  - B. Ignore the conflicts and continue to change the device, conflicting settings will be imported.
  - C. Click **OK** to continue changing device. Conflict settings will not be imported.

e <sup>2</sup> Conflicts fou	ınd				—		×
Confli	icts were fo	ound while changing	g the device and pa	ckage .			
Press	Cancel to Ignore to	e following options: cancel changing the continu changing th	device and packag		ngs wil	l be impor	ted
	OK to con	tinue changing the	device and package	; conflicting setting	js will n	ot be	
		Cancel	<u>l</u> gnore	OK		<u>D</u> etails >	>

Figure 34. Conflicts found during changing device

5. To continue chapter 5, change the pin configuration from NewName.pincfg back to S7G2-DK.pincfg.

#### 5. How to use the Pin Selection pane

The **Pin Selection** pane shows all of the pins that are available for the device. The pins are categorized into groups - "Ports", "Peripherals", and "Other Pins".

Note: The usage of **Pin Selection** is the same for IAR EW for Synergy and e<sup>2</sup> studio.



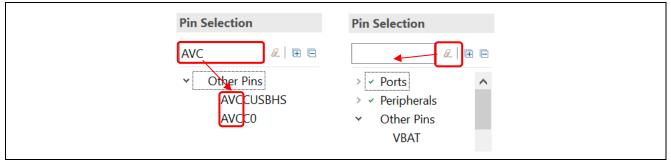
#### 1. The **Pin Selection** pane contains:

- A. Filter text box
- B. Clear button
- C. Expand All button
- D. Collapse All button
- E. Pins tree which contains the categorized pins

	Image: Pin_Configurator_Example] Synergy Configuration ≥ Pins Configuration
	Select pin configuration         S7G2-DK.pincfg         ✓         Generate data:         g_bsp_pin_cfg
Filter text box	Pin Selection     Pin Configuration     Clear       type filter text     Image: Collapse All       > < Ports     All       > < Peripherals     Expand All

### Figure 35. Pin Selection Pane

2. Typing text in the filter text box will list out the pins that contain the text. Clicking on the **Clear** button will clear the text box and the filter results.



#### Figure 36. Use the filter text box

3. The Expand All button and the Collapse All button will expand and collapse the pins tree respectively.

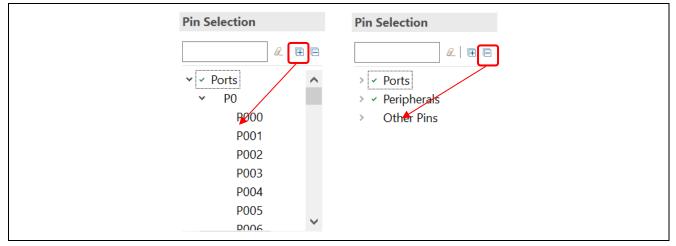


Figure 37. Use the Expand All and Collapse All button



4. Selecting a port or peripheral in the **Pin Selection** pane will show its settings in the **Pin Configuration** area. It can then be modified and set up as necessary. The icon of the selected pin will also be marked with blue border in the **Package** view.

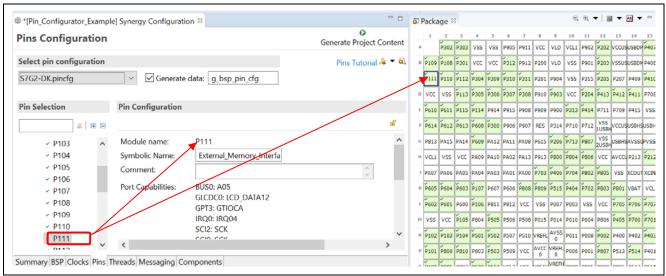


Figure 38. Select a Port in Pin Selection pane

## 6. How to use the Pin Configuration pane

The **Pin Configuration** pane allows user to change the setting of Ports and Peripherals that are selected in the **Pin Selection** pane.

Note: The use of **Pin Configuration** is the same for IAR EW for Synergy and e<sup>2</sup> studio.

- 1. The Pin Configuration pane contains:
  - A. Lock/Unlock Settings button
  - B. Setting area

Pin Configuration	Setting Area				
				Lock/Unlock Settings	
Module name:	P108				^
Symbolic Name:	JTAG_TMS				
Comment:			$\hat{}$		
Port Capabilities:	DEBUG0: SWDIO DEBUG0: TMS GPT0: GTIOCB SCI9: CTS_RTS_SS SPI1: SSL0				
P108 Configuration					
Mode:	Peripheral mode	~			
Pull up:	None	~			
Drive Capacity:	Low	$\sim$			
Output type:	CMOS	$\sim$			~

Figure 39. Pin Selection Pane



2. Click on the Lock/Unlock Setting button to disable/enable the modification of the selected item in the **Pin Configuration** pane.

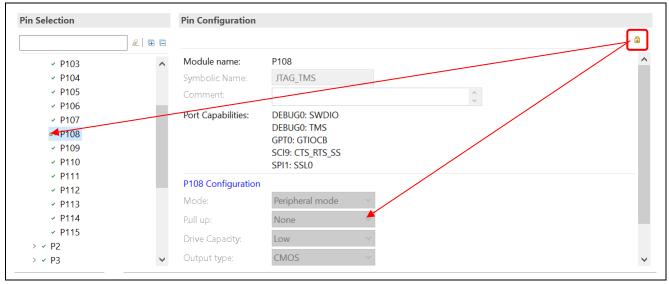


Figure 40. Lock a selected Pin



3. Click on the (follow connection) button in the setting area of a connected pin to go to the setting area of the corresponding peripheral and vice versa.

Module name:	P108
Symbolic Name:	JTAG_TMS
Comment:	
Port Capabilities:	DEBUG0: SWDIO DEBUG0: TMS GPT0: GTIOCB SCI9: CTS_RTS_SS SPI1: SSL0
P108 Configuration	
Mode:	Peripheral mode $\sim$
Pull up:	None ~
Drive Capacity:	Low ~
Output type:	CMOS ~
Chip input/output	
P108:	✓ DEBUG0_TMS ✓
	$\mathbf{i}$
Module name:	DEBUG0
Usage:	When switching between modes, first disable.
Operation Mode:	JTAG ~
Input/Output	
TCK:	✓ P300 ✓
TDI:	✓ P110 ✓
TDO:	✓ P109 ✓
TMS:	✓ P108 ✓
SWCLK:	None 🗸
SWDIO;	None 🗸
SWO:	None V

Figure 41. Switching between Pin and Peripheral setting

4. If a module setting is configured incorrectly, that module will be marked with the error symbol in the Pin Selection pane and Pins Configuration pane. The details of the conflicts will be shown in the Pin Conflicts or Problems window. All conflicts need to be resolved before generating the source code. For example, in DEBUG0 module, change the TCK to None to make the setting wrong. After finishing, change it back to P300.



Select pin configuration						Pins Tutorial 🖧 🔻
S7G2-DK.pincfg	✓ Generate	data: g_bsp_pin_c	fg			
Pin Selection		Pin Configuration				
debug	2 8 8					ซ์
<ul> <li>Peripherals</li> <li>System:DEBUG</li> </ul>		Module name: Usage:	DEBUG0 When switching	g between modes, first di	sable.	
DEBUG0		Operation Mode:	JTAG	~		
		Input/Output TCK:	* None			
		TDI:	- P110	~	4	
		TDO:	- P109	~	\$	
		TMC	P109	4	4	1
Summary BSP Clocks <sup>9</sup> Pins Three	eads Messaging	Components				
Properties 🕴 Problems 🛱 🍕 Sn	nart Browser			* * * * *	De Pin Conflicts	
error, 1 warning, 0 others					1 error, 0 warnings, 0 others	
Description		~	52. 	128	Description	Module
Errors (1 item)					Incorrect settings for Operation	Mode: JTAG, expected pin DEBUG0
Incorrect settings for Oper	ation Mode: JTA	, expected pin DEB	UG0.TCK to be con	nected		

Figure 42. Error in Pin Configuration

#### 5. After the pins are configured correctly, press Ctrl + S to save the changes.

	♥ [Pin_Configurator_Example] Synergy Configuration <sup>№</sup> Pins Configuration
An asterisk (*) indicates that the changes in setting is not saved. Press [Ctrl+S] to save it	Select pin configuration         S7G2-DK.pincfg         ✓ Generate data:         g_bsp_pin_cfg

Figure 43. Unsaved setting

#### 7. How to use the Package View

The **Package** view displays all available pins in the device along with their attributes.

Note: The usage of **Package** view is the same for IAR EW for Synergy and e<sup>2</sup> studio.

In e<sup>2</sup> studio, the **Package** view is opened by default in the **Synergy Configuration** perspective. If it is closed, select **Window**  $\rightarrow$  **Show View**  $\rightarrow$  **Pin Configurator**  $\rightarrow$  **Package** to open it.

## 1. The **Package** view contains:

#### A. Pins table

Display all the pins along with their attribute. The Pins attribute are shown as background color and label.

B. Zoom In, Zoom Out button

Zoom in and zoom out the **Pins table** 

- C. Select Attribute for Background Color button Change the background colors of the pin according to the in attributes selected.
- D. Select Attribute for Labels button Switch between the module name and symbolic name of the pins.
- E. Description text Describe the color being used in the **Pins table**.



		age	3	4	5	6	_	8			2, -		$\geq$	<b>₩ *</b>	_		Select Attribute for Labels
	1	P302	P303	VSS	VSS	9905	7 P911	8 VCC	9 VLO	10 VCL1	11 P902	12 P208	13 VCCUS	14 BUSBDP	15 P407	A	TOT Labers
	P109	P108	¥301	vcc	vcc	¥9312	P912	P200	VLO	VSS	P901	¥203	VSSUS	USBDM	P408	B	Select Attribute for
	¥111	P110	P112	¥304	¥309	¥310	P311	P201	P904	vss	P315	P205	P207	P409	pe410	c	Background Color
	VCC	VSS	P113	¥305	¥306	¥307	¥308	P910	¥903	vcc	¥204	¥413	¥412	P411	P708	2	
	P610	P611	P115	P114	P914	P915	P908	P909	P900	P313	¥414	P711	P709	P415	VSS	E	Zoom In,
	P614	¥612	¥613	¥608	¥300	P906	P907	RES	P314	P710	P712	VSS 1USBH	vccus	EUSBHS	OUSBHS	F	Zoom Out
	P813	PA15	PA14	¥609	PA12	PA11	PAOS	P615	¥206	P713	PB07	VSS 2USBHS	USBHSI	AVSSU	spyssus	G	
	VCL1	vss	vcc	PA09	PA10	PAO2	PA13	P913	¥800	¥804	¥806	vcc	AVCCU	P213	¥212	н	
	PA07	PA06	PAOS	PA04	PA03	PA01	PAOO	¥703	¥406	¥704	¥802	¥05-	VSS	ксоит	XCIN	3	Pins table
	¥605	¥604	¥603	P107	P607	P606	<b>P806</b>	¥809	P515	¥404	¥702	¥803	¥801	VBAT	VCL	к	
	¥602	¥601	P600	P106	P811	P812	VCC	vss	P007	P003	vss	VCC	P705	¥706	¥707	L	
1	VSS	VCC	¥105	P804	¥505	P506	P508	P015	P014	P010	P004	P806	¥405	¥700	¥701	м	
	¥102	¥103	P104	¥501	¥502	P507	P510	VREFL	AVSSO	P011	P008	¥002	P400	P402	¥403	N	
	¥101	¥800	P810	P803	¥503	P509	vcc	AVCC 0	VREFL 0	P006	P001	¥807	P513	P514	P401	P	
	¥100	¥801	P802	¥500	¥504	VCL2	VSS	VREFH	VREFH 0	P009	P005	P000	P805	P512	P511	R	
1	1	2	3	4 R	5 7ES70	6 27xxx	7 000xBl	8 D - 22	9 4BGA	10 (Tor	u Viev	12 v)	13	14	15		
		ction s	status:	~		rning	D				o viev	•/					Description Text

Figure 44. Package View GUI

2. When an item in the **Pin Selection** is selected, all the corresponding pins will be bordered with blue line. In this example, PB04, PB05, PB02 and PB03 are used by the Serial Communications Interface (SCI8), thus they are marked by blue line in the package view.

in Selection	Pin Configuratio	n			E P610	P611	P115		4 P915	P908	P909 P	900 P31	.3 P414	P711	P709	P415
ci 🖉 🗉 🖻					F P614	P612	P613	9608 P3	0 P906	P907	RES P	314 P71	.0 P712	VSS 1USBF	vccus	USBH:
SCI1	Operation Mode:	Simple SPI	~	^	G P813											AVSSI
SCI2	Input/Output				H VCL1	VSS	vcc	PA09 PA	0 PA02	PA13	P913 P	вос рво	4 PB06	vcc		P213
SCI3	TXD_MOSI:	✓ PB04	~	4	J PA07	PA06	PA05	PA04 PA	3 PA01	PA00	ртоз р	406 P70	14 PB02	PB05	VSS	хсои
SCI4 SCI5	RXD_MISO:	✓ PB05	~	\$	к р605	P604	P603		7 P606	P808	P809 P	515 P40	4 P702	PB03	Р 01	VBAT
SCI6	SCK:	✓ PB03	~		L P602	P601	P600	P106 P8	1 P812	vcc	VSS P	007 -00	9 V33	vee	705	P706
SCI7	CTS_RIS_SS.	✓ PB02	×.	\$	M VSS	vcc	P105	P804 P5	5 P506	P508	P015 P	014 P01	0 P004	P806	¥ P405	P700
SCI8	SDA:	None	~	Image: A state of the state	N P102	P103	P104		2 P507	P510	VREFL A	VSS POI	1 P008	8 P002	P400	P402
< >	<			>	P P101	P800	P810	P803 P5	3 P509	vcc	AVCC V	REFL POC	6 P001	P807	P513	P514
Immary BSP Clocks Pins 1	hreads Messaging	Components			R P100	P801	P802	2500 P5	4 VCL2		<u> </u>					

Figure 45. Pins of SCI8 are marked with blue line in Package view



#### 3. Selecting a pin in the **Package** view will show its setting in the **Pin Configuration** pane.

Select pin configuration		F	Pins Tutorial 緒 🤊	▼ 🗟, 👘	P109	P108	РЗ01	vcc	VCC P
S7G2-DK.pincfg	✓ ✓ Generate of Contracts	data: g_bsp_pin_cfg			P111	P110	P112	¥ P304	P309 P
				C	vcc	VSS	P113	P305	P306 P
Pin Selection	Pin Configuration			E	P610	P611	P115	р́114	P914 P
			i.	ŝ ,	P614	P612	P613	P608	P300 P
> ~ P5	Module name:	P604		▲ G	P813	PA15	PA14	P609	PA12 P
Υ ✓ P6	Symbolic Name:	External_Memory_Interfa		н	VCL1	VSS	vcc	PA09	PA10 P
P600 ✓ P601	Comment:		$\sim$	1	PA07	PA06	PA05	PA04	PA03 P/
<ul> <li>✓ P601</li> <li>✓ P602</li> </ul>	Port Capabilities:	BUS0: D12_DQ12			P605	P604	9603	р́107	P607 P
✓ P603	P604 Configuration			I	P602	P601	P600	P106	P811 P
~ P604	Mode:	Peripheral mode		P	VSS	vcc	P105	P804	P505 P
✓ P605 P606	Pull up:	None ~		v P	P102	P103	р́104	P501	P502 P
P607	<		>		P101	P800	P810	P803	р р503 р
Summary BSP Clocks Pins T	hreads Messaging Cor	nponents		F	P100	P801	P802	P500	P504 V

Figure 46. Select a Pin in Package view

4. When a pin is configured correctly, it is marked with an ✓ (OK) symbol. If it is incorrectly configured, it is marked with 🗳 (Error) symbol.

																1
A	1 NC	2 P302	3 P303	4 VSS	5 VSS	6 P905	7 P911	VCC_	9 VLO	10 VCL1	11 P902	12 P202	VCC_	USB_	15 P407	A
		102	1000	V 55	V 55	-ano	1911	DCDC	VL0	VCL1	1902	P202	USB	DP		
В	P109	P108	P301	VCC	VCC	P312	P912	P200	VLO	VSS	P901	P203	USS_ USB	USB_ DM	P408	B.
С	P111	P110	P112	P304	P309	P310	P311	P201	P904	VSS	P315	P205	P207	P409	P410	с
D	vcc	VSS	P113	P305	P306	P307	P306	P910	P903	vcc	P204	P413	P412	P411	P708	D
E	P610	P611	P115	P114	P914	P915	P908	P909	P900	P313	P414	P711	P709	P415	VSS	E
F	P614	P612	P613	P608	×	P906	P907	RES	P314	P710	P712	VSS1_ USBHS	VCC_ USBHS	USBHS, DP	USBHS, DM	Error pin setting
G	P813	PA15	PA14	P609	PA12	PA11	PA06	P615	P206	P713	P807	VSS2_ USBHS	USBHS, RREF	AVSS_ USBHS	PVSS_ USBHS	G
н	VCL_F	VSS	vcc	PA09	PA10	PA02	PA13	P913	P800	P804	P806	vcc	AVCC_ USBHS	P213	P212	н
J	PA07	PA06	PA05	PA04	PA03	PA01	PAOO	P703	P406	P704	P802	P805	VSS	хсоит	XCIN	3
к	P605	P604	P603	P107	P607	P606	P806	P809	P515	P404	P702	P803	P801	VBATT	VCLO	K Correct pin
L	P602	P601	P600	P106	P811	P812	vcc	vss	P007	¥003	vss	vcc	<b>~</b>	P706	P707	L setting
м	VSS	vcc	P105	P804	P505	P506	P508	P015	P014	P010	P004	P806	P405	P700	P701	M
N	P102	¥103	P104	P501	P502	P507	P510	VREFL	AVSSO	P011	P008	P002	P400	P402	P403	N
P	¥101	P800	P810	P803	P503	P509	vcc	AVCC 0	VREFL 0	¥006	P001	P807	P513	P514	P401	P
R	¥100	P801	P802	P500	P504	VCL2	VSS	VREFH	VREFH 0	P009	P005	¥000	P805	P512	P511	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	 1

Figure 47. Correct and error symbol in Package view



- 5. You can change the background color of the pins based on the selected attribute. Click on the **button** on the top right corner of **Package** view to show the drop-down list:
  - A. Connection Status (default): Error, Warning, OK
  - B. Drive Capacity: High, Medium, Low
  - C. Mode: Analog Mode, Disable, IRQ Mode, Input Mode, Output mode (Initial High), Output mode (Initial Low), Peripheral mode.
  - D. Output Type: CMOS, n-ch open drain
  - E. Pull Up: None, input pull-up

Selecting one item from the list will change the background color of the **Pins table**. The colors will be described in the Description Text area.

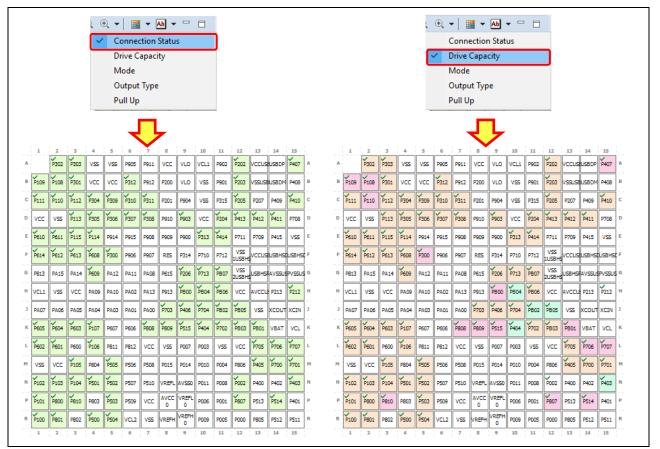


Figure 48. List of Pins attributes



6. You can also switch between the module name and symbolic name of the pins by clicking on the button on the top right corner of **Package** view:

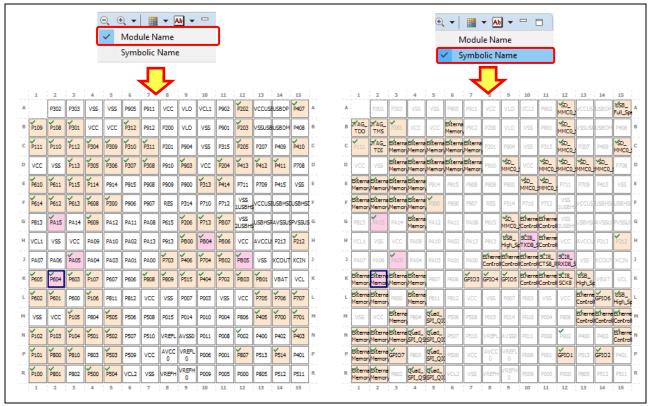


Figure 49. Module name and Symbolic name in Package view



# 8. Generating Pin Configuration source code

#### 8.1 Generating source code in e<sup>2</sup> studio

1. After configuring the pins, you can click on the **Generate Project Content** button to generate the necessary pin configuration source files for the project

Pins Configura	tion			Generate Project Conte
Select pin configur	ation			Pins Tutorial ⁄ 🔻
S7G2-DK.pincfg		✓ Generate	data: g_bsp_pin_cfg	
Pin Selection		Pin Configuration		
ß	ŧ.			۵
> ~ P5 > ~ P6 > ~ P7	^	Module name: Symbolic Name: Comment:	P604 External_Memory_Interfa	0
> ~ P8 > ~ P9		Port Capabilities:	BUS0: D12_DQ12	
<ul> <li>PA</li> <li>PB</li> <li>Peripherals</li> <li>Other Pins</li> </ul>		P604 Configuration Mode: Pull up:	Peripheral mode None V	
	$\sim$	<		>

Figure 50. Generate Project Content button

2. The source code for pin Configuration is generated at synergy\_cfg/ssp\_cfg/bsp/bsp\_pin\_cfg.h and src/synergy\_gen/pin\_data.c.

Note: Do not edit these files as they will be overwritten when building the project and whenever the **Generate Project Content** button is pressed.



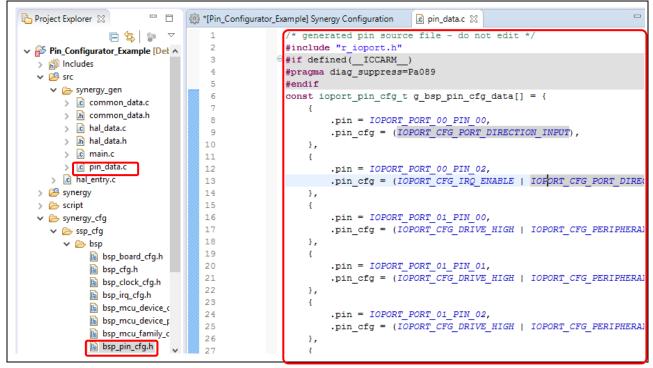


Figure 51. Source code for Pin Configuration

3. In case of using multiple pin configurations, different data structures can be created in pin\_data.c. This allows dynamic switching of pin configurations during run time (for example, for different power modes).

In this example, we use two pin configuration files to generate two data structures.

NewName.pincfg	📄 R7FS7G27H2A01CBD.pincfg 🛛 👹 [Pin_Configurator_Example] Synergy 🕼 pin_data.c 🖾 🧮
1	<pre>/* generated pin source file - do not edit */</pre>
2	#include "r_ioport.h"
3	⊖#if defined(ICCARM)
4	#pragma diag_suppress=Pa089
5	#endif
6	<pre>const ioport_pin_cfg_t g bsp pin_cfg_data[ = {</pre>
7	{
8	.pin = IOPORT_PORT_00_PIN_00,
9	<pre>.pin_cfg = (IOPORT_CFG_IRQ_ENABLE   IOPORT_CFG_PORT_DIRECTION_I</pre>
10	},
11	£
12	.pin = IOPORT_PORT_00_PIN_01,
13	.pin_cfg = (IOPORT_CFG_PORT_DIRECTION_INPUT),
14	},
15	£
700 701 702 703 704 705 705 706 707	<pre>const ioport_pin_cfg_t NewConfig_data[] = {     {         .pin = IOPORT_PORT_00_PIN_00,         .pin_cfg = (IOPORT_CFG_IRQ_ENABLE   IOPORT_CFG_PORT_DIREC     },     {         .pin = IOPORT_PORT_00_PIN_01,         .pin cfg = (IOPORT_CFG_PORT_DIRECTION_INPUT),     } }</pre>
708	},
	1 r {
709	<pre>// {     .pin = IOPORT_PORT_00_PIN_02,</pre>
708 709 710 711	{

Figure 52. Different data structures for different Configurations



4. Each pin configuration will have its own CSV file which contains all pin configurations. The CSV files can be found at synergy\_cfg/ssp\_cfg/bsp/\*.csv.

🖻 🔄 💱 🗢								
🗸 😂 Pin_Configurator_Example [Det 🔺		Α	В	С	D	E	F	G
> 前 Includes	1	Name	Pin	Function	Symbolic	Drive Capa	IRQ	Mode
> 🔑 src	2	AVCC0	P8	ADC AVC	CO			
> 🔑 synergy	3	AVCCUSB	H13	USBHS0 A	VCCUSBH	5		
> 🗁 script	4	AVSS0	N9	ADC AVS				
✓ ➢ synergy_cfg	5	AVSSUSB	G14	USBHS0 A	VSSUSBHS			
✓ ➢ ssp_cfg ✓ ➢ bsp	6	P000	R12	_				Disabled
bsp_board_cfg.h	7 7	P001	P11					Disabled
bsp_cfg.h	8	P002	N12	GPIO			IRQ8-DS	Input mod
bsp_clock_cfg.h	9	P003	L10					Disabled
📓 bsp_irq_cfg.h	10	P004	M11					Disabled
📓 bsp_mcu_device_c	11	P005	R11					Disabled
bsp_mcu_device_p	12	P006	P10					Disabled
bsp_mcu_family_c	13	P007	L9					Disabled

Figure 53. CSV files

# 8.2 Generating source code in IAR EW for Synergy

1. After configuring the pins, you can click on the **Generate Project Content** button to generate the necessary pin configuration source files for the project.

Generate Project Content
Pins Tutorial 烯 🔻 🗟

Figure 54. Generate Project Content button



2. The source code is generated at <ProjectDir>\Synergy\Source Files\src\synergy\_gen\pin\_data.c.

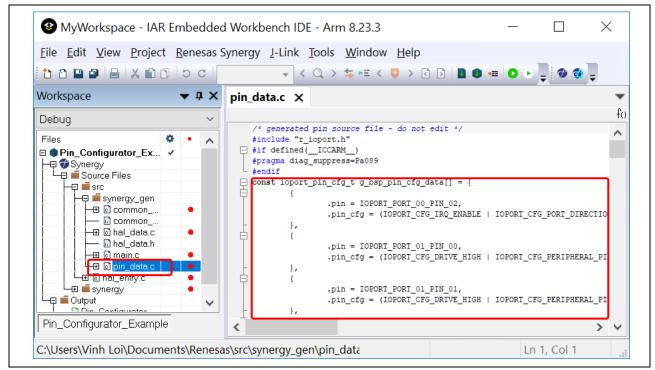


Figure 55. Source code for Pin Configuration

3. In case of using multiple pin configurations, different data structures can be created in pin\_data.c. This allows dynamic switching of pin configurations during run time (For example, for different power modes). In this example, we will use S7G2-DK.pincfg and NewName.pincfg to generate two data structures. The data structures are named after the unique names that were entered in the text box in previous steps: **g\_bsp\_pin\_cfg** and **NewConfig** 

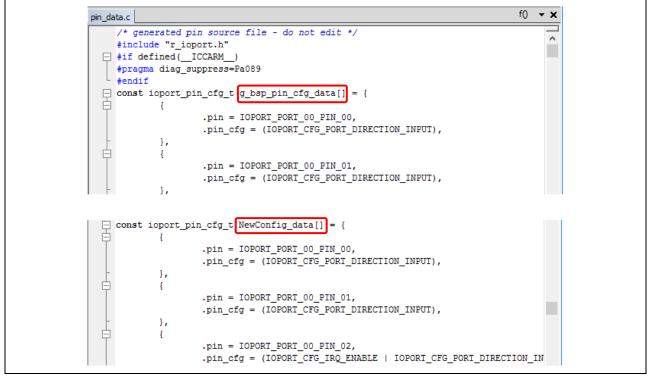


Figure 56. Different data structures for different Configurations



4. Each pin configuration will have its own CSV file which contains all pin configurations. The CSV files are not shown on the **Workspace** window, but you can open Windows Explorer and locate the file at <ProjectDir>\synergy\_cfg\ssp\_cfg\bsp\.

		~	orkspace >						
Na	me	^		D	ate modified	Ту	pe		Size
	bsp_cfg.h			11	/28/2016 4:3	2 PM H	File		2 KB
	bsp_clock_c	:fg.h		11	/28/2016 4:3	2 PM H	File		2 KB
	bsp_irq_cfg	.h		11	/28/2016 4:3	2 PM H	File		30 KB
	bsp_pin_cfg			11	/30/2016 1:5	8 PM H	File		1 KB
×a	NewName.			11	/30/2016 1:5	8 PM M	icrosoft Exce	I C	18 KB
1	S7G2-DK_BI	inkv.csv		11	/30/2016 1:5	8 PM M	icrosoft Exce	I C	18 KB
1									
1									
	<u> </u>	Pin po	Function	Symbolic	Drive Cap	IRQ	Mode	Outpu	ut ty <mark>  Pull up</mark>
2	AVCC0	P8	Function	Symbolic	Drive Cap	IRQ	Mode	Outpu	ut ty <mark> </mark> Pull up
2 3	AVCC0 AVCC_USE	P8 H13	Function	Symbolic	Drive Cap	IRQ	Mode	Outpu	ut ty <mark>ı</mark> Pull up
2 3	AVCC0 AVCC_USE AVSS0	P8 H13 N9	Function	Symbolic	Drive Cap	IRQ	Mode	Outpu	ut ty <mark>ı</mark> Pull up
2 3 4	AVCC0 AVCC_USE AVSS0 AVSS_USE	P8 H13 N9	Function	Symbolic	Drive Cap	IRQ	Mode	Outpu	ut ty  Pull up
2 3 4 5	AVCC0 AVCC_USE AVSS0 AVSS_USE NC	P8 H13 N9 G14	Function	Symbolic	Drive Cap	None	Mode		ut tyj Pull up
2 3 4 5 6	AVCC0 AVCC_USE AVSS0 AVSS_USE NC P000	P8 H13 N9 G14 A1	Function	Symbolic	Drive Cap			de	ut tyj Pull up
2 3 4 5 6 7	AVCC0 AVCC_USE AVSS0 AVSS_USE NC P000 P001	P8 H13 N9 G14 A1 R12	Function	Symbolic	Drive Cap	None	Input mo	de	ut tyj Pull up
2 3 4 5 6 7 8 9	AVCC0 AVCC_USE AVSS0 AVSS_USE NC P000 P001 P002	P8 H13 N9 G14 A1 R12 P11	Function	Symbolic	Drive Cap	None None	Input mo	ode ode ode	ut tyj Pull up

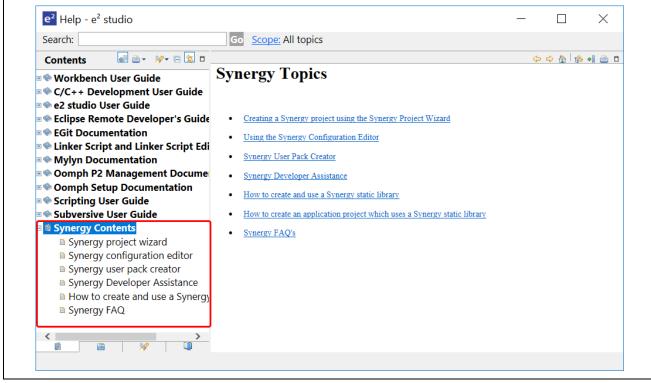
Figure 57. CSV files

## 9. Additional Information

For more information on the Pin Configurator or other Synergy Configurator sections, please refer to e<sup>2</sup> studio Help Contents.

Select Help → Help Contents, go to Synergy Contents → Synergy configuration editor to open the topic related to the Synergy Configurator.





#### Figure 58. Synergy Topic in e<sup>2</sup> studio Help Contents

For introduction and installation guide of IAR EW for Synergy, refer to IAR EW for Synergy Help Contents Select Help  $\rightarrow$  Contents..., go to IAR Embedded Workbench(R) for Renesas Synergy(TM).

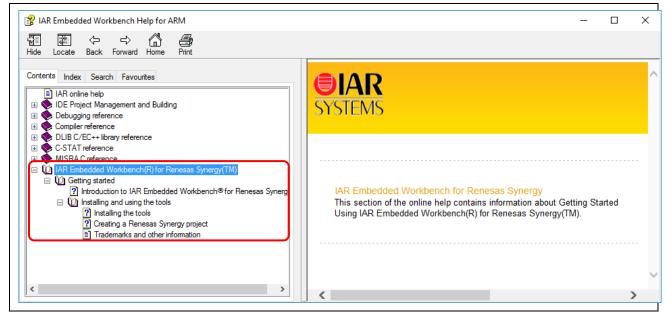


Figure 59. Synergy Topic in IAR EW for Synergy Help Contents



# Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

Synergy Software	www.renesas.com/synergy/software
Synergy Software Package	www.renesas.com/synergy/ssp
Software add-ons	www.renesas.com/synergy/addons
Software glossary	www.renesas.com/synergy/softwareglossary
Development tools	www.renesas.com/synergy/tools
Synergy Hardware	www.renesas.com/synergy/hardware
Microcontrollers	www.renesas.com/synergy/mcus
MCU glossary	www.renesas.com/synergy/mcuglossary
Parametric search	www.renesas.com/synergy/parametric
Kits	www.renesas.com/synergy/kits
Synergy Solutions Gallery	www.renesas.com/synergy/solutionsgallery
Partner projects	www.renesas.com/synergy/partnerprojects
Application projects	www.renesas.com/synergy/applicationprojects
Self-service support resources:	
Documentation	www.renesas.com/synergy/docs
Knowledgebase	www.renesas.com/synergy/knowledgebase
Forums	www.renesas.com/synergy/forum
Training	www.renesas.com/synergy/training
Videos	www.renesas.com/synergy/videos
Chat and web ticket	www.renesas.com/synergy/resourcelibrary



# **Revision History**

		Description	
Rev.	Date	Page	Summary
1.00	Jan.01.19	—	First release document
1.01	Sep.30.19	_	Updated for SSP v1.6.0



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