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SH7280 Group

Reception of Serial Data by the SCI in Clock Synchronous Mode

Introduction

This application note describes reception of serial data by using the clock-synchronous transfer function of the serial communications interface (SCI). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

This sample application employs the clock-synchronous serial transfer function of the serial communications interface (SCI) to perform data reception. Figure 1 shows an example of connection for reception by the SCI in clock synchronous mode.

- SCI2 is used.
- The communications format has a fixed 8-bit data length.
- SCI2 single-direction communications is started by the receive interrupt. Interrupt processing is activated by the receive-data-full interrupt.
- Once 32 bytes of data have been received, operation for reception is halted.

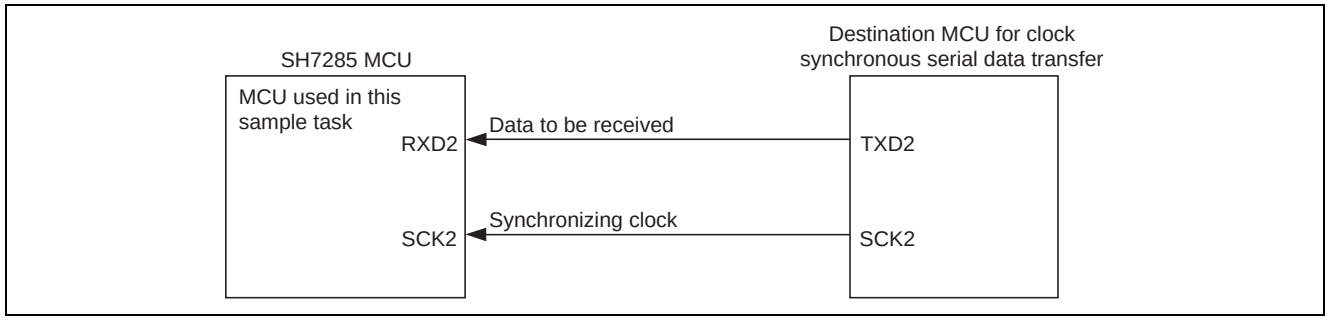


Figure 1 Connection Example for Reception by the SCI in Clock Synchronous Mode

1.2 Module Used

Serial communications interface (SCI2)

1.3 Applicable Conditions

MCU	SH7285	
Operating frequency	Internal clock:	100 MHz
	Bus clock:	50 MHz
	Peripheral clock:	50 MHz
C compiler	SuperH RISC engine Family C/C++ Compiler Package Ver.9.1.1	
	(from Renesas Technology Corp.)	

2. Description of the Sample Application

This sample application employs the receive-data-full interrupt (RXI) source of the serial communications interface (SCI) to receive serial data in clock synchronous mode.

2.1 Summary of MCU Module Used

In clock synchronous mode, the SCI receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communications. An internal clock or an external clock from the SCK pin can be selected as the SCI clock source. When an internal clock has been selected, a synchronizing clock is output from the SCK pin. When an external clock has been selected, a synchronizing clock is input into the SCK pin. The receiving section of the SCI has the double-buffer structure, which enables high-speed continuous data transfer.

In clock-synchronous serial communications, each data bit is output on the communications line from one falling edge of the serial clock to the next. Data is guaranteed valid at the rising edge of the serial clock.

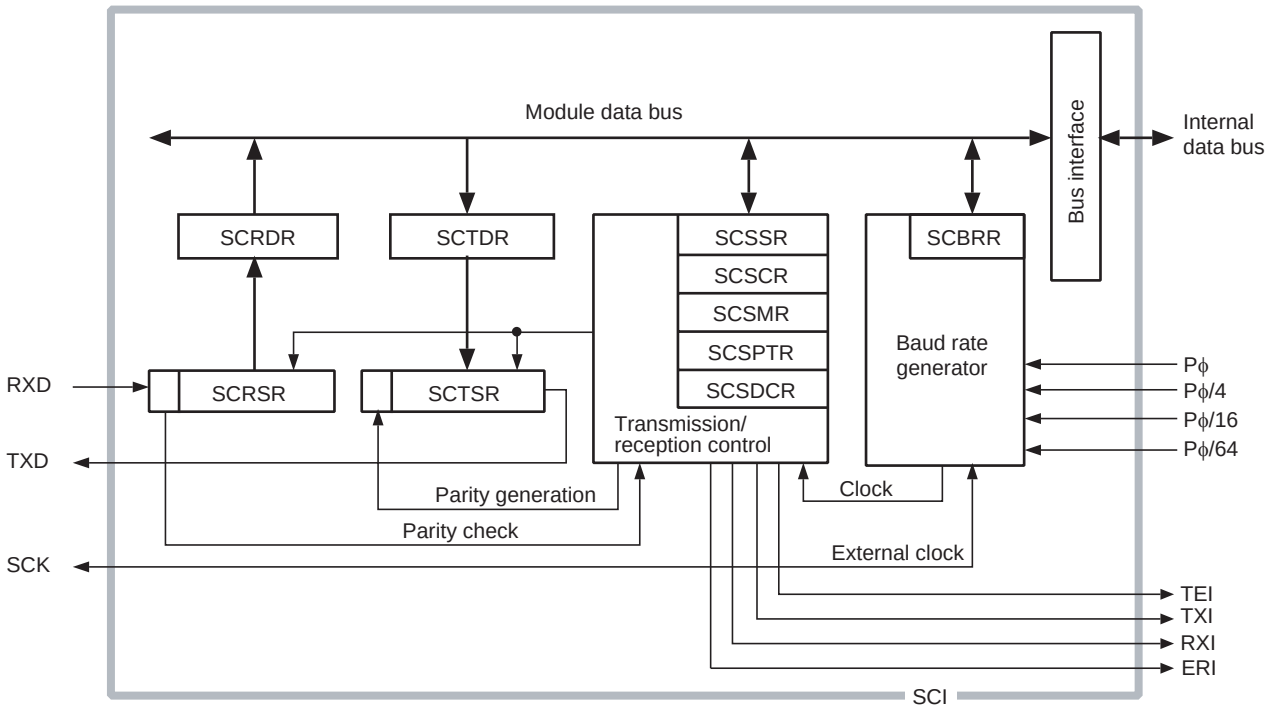
In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communications line remains in the state of the MSB.

For details on the SCI, please refer to the section on serial communications interface in the *SH7280 Group Hardware Manual (REJ09B0393)*.

Table 1 gives an overview of serial communications in clock synchronous mode. Figure 2 shows a block diagram of the SCI.

Table 1 Overview of Serial Data Communications in Clock Synchronous Mode

Item	Description
Number of interfaces	4 (SCI0, SCI1, SCI2, SCI4)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: Peripheral clock) For external clock: Input clock on the SCK pin
Data format	Transfer data length: Fixed at 8 bits Order: LSB first and MSB first are selectable
Baud rate	For internal clock: 1 kbps to 500 kbps (Pϕ = 50 MHz) For external clock: Up to 8,333,333.3 bps (Pϕ = 50 MHz, external input clock of 8.3333 MHz)
Error detection	Overrun error
Interrupt requests	Receive-data-full interrupt (RXI) Receive error interrupt (ERI)
Clock sources	Internal and external clocks are selectable
	• Internal clock When the internal clock has been selected, the SCI operates using the clock from the baud-rate generator and outputs this clock to external devices as the synchronizing clock. • External clock When the external clock has been selected, the SCI operates on the input synchronizing clock, not using the on-chip baud rate generator.



[Legend]
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 2 Block Diagram of the SCI

2.2 Description of the Sample Program

Table 2 gives the settings for SCI communications function of this sample task, and figure 3 shows the operations in data reception.

Table 2 Settings for Communications Function of the Sample Program

Item	Description
Module	SCI2
Communications mode	Clock synchronous mode
Interrupts	Receive-data-full interrupt (RXI) Receive error interrupt (ERI)
Transfer rate	100 kbps
Number of data to be received	32 bytes
Data length	8-bit data (fixed)
Bit order	LSB-first
Synchronizing clock	Internal clock, or synchronizing clock on the SCK pin

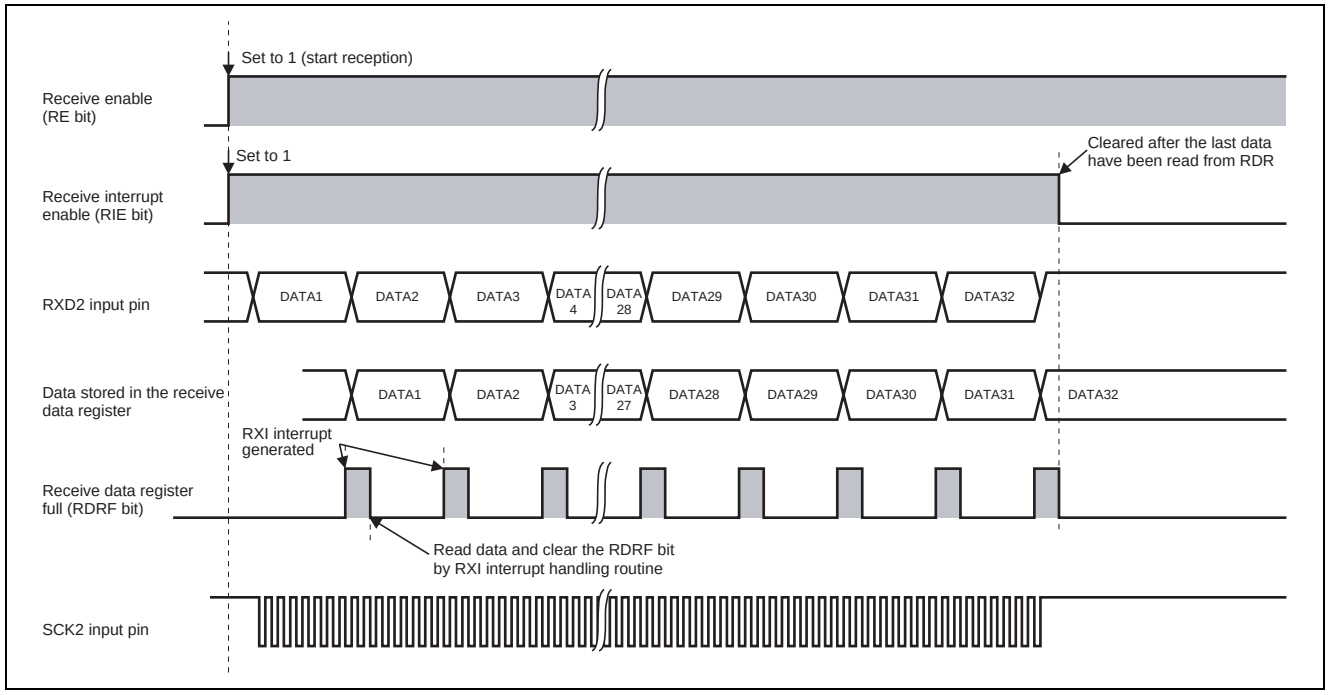


Figure 3 Operations for Data Reception

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCI2 for clock-synchronous mode operation.

Figure 4 shows the flow of processing by the sample task, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for initialization of data reception in clock synchronous mode, and figure 7 shows the flow for setting up the pin function controller. Furthermore, figure 8 shows the flow for handling receive error interrupts in clock synchronous mode, and figure 9 shows the flow for handling receive interrupts in clock synchronous mode. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual (REJ09B0393)*.

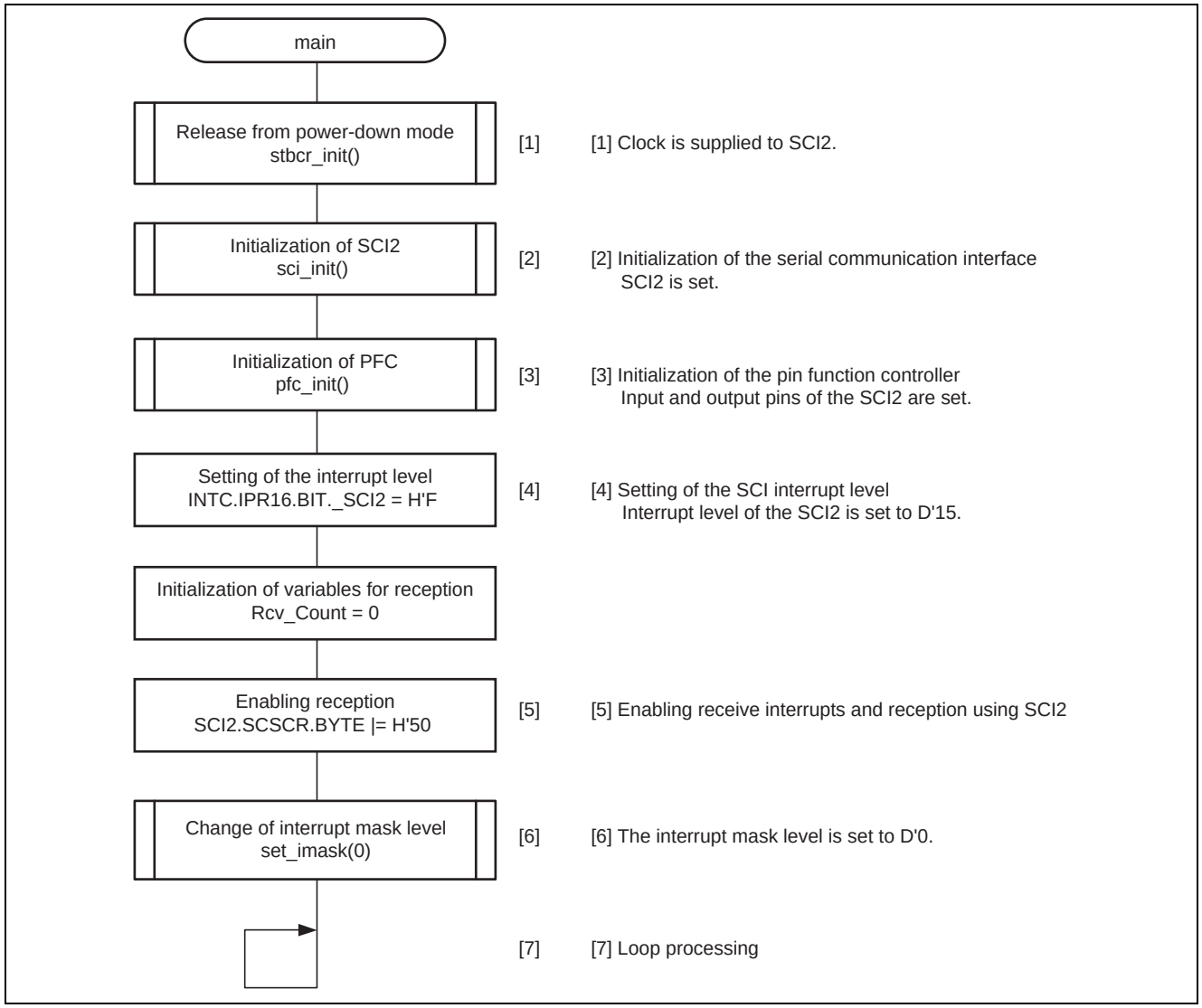


Figure 4 Flow of Processing by the Sample Program

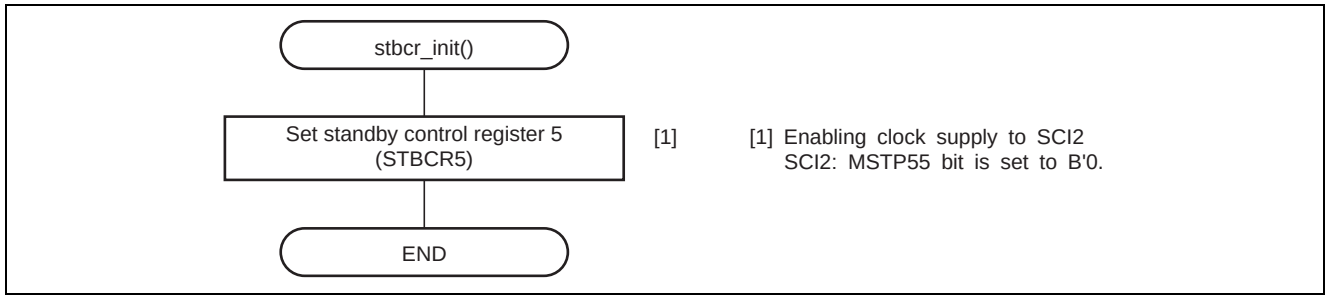


Figure 5 Flow of Settings for Release from Module-Standby Mode

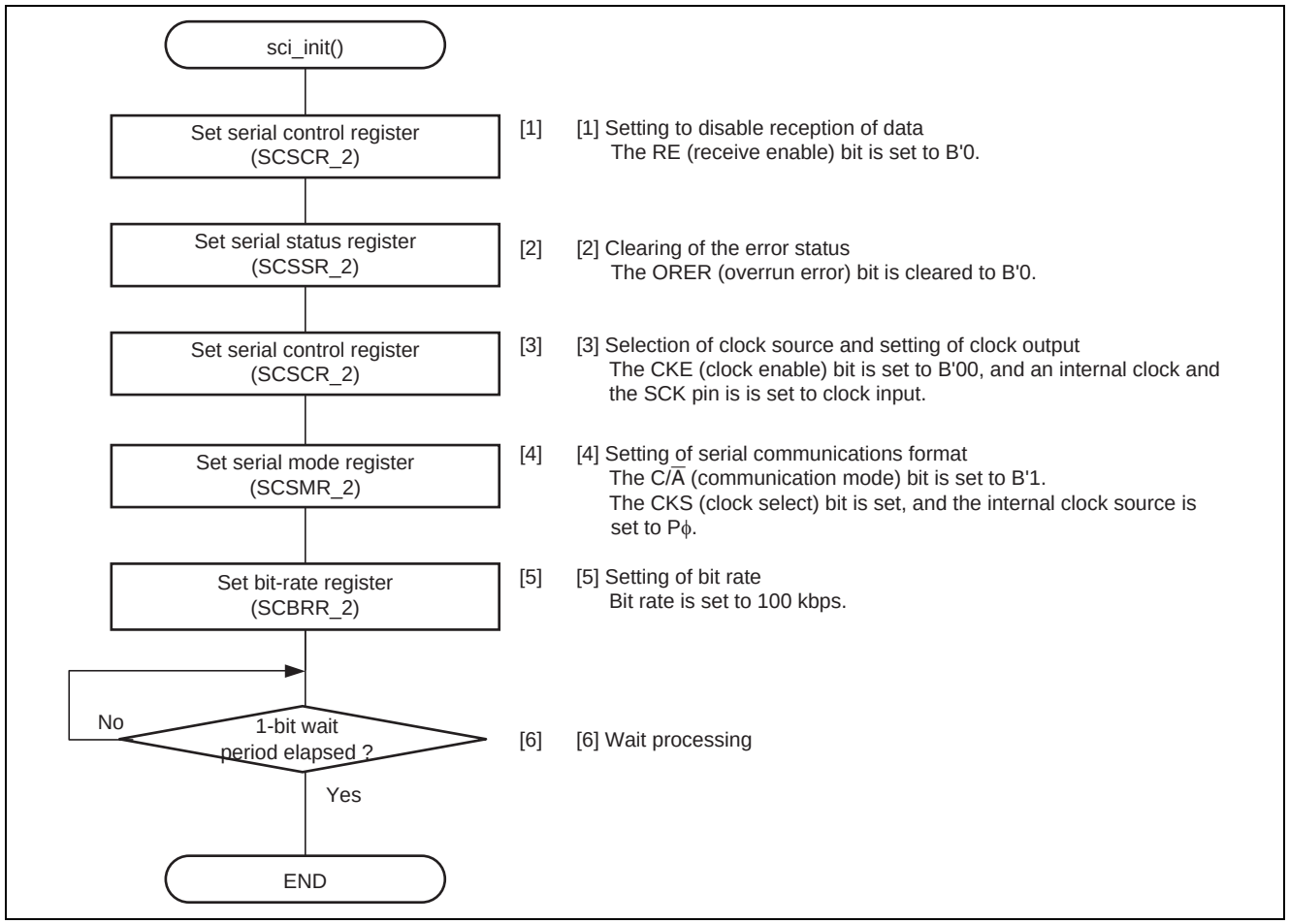


Figure 6 Flow for Initialization of Data Reception in Clock Synchronous Mode

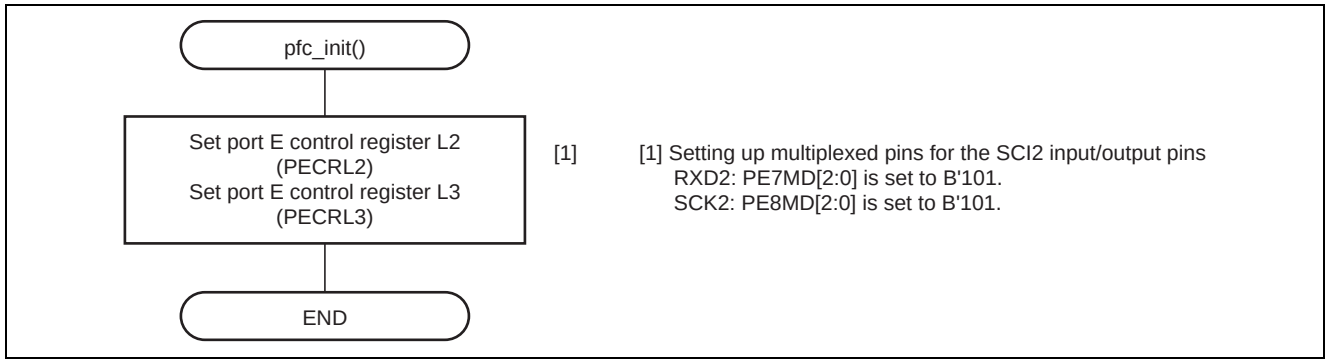


Figure 7 Flow for Setting Up the Pin Function Controller

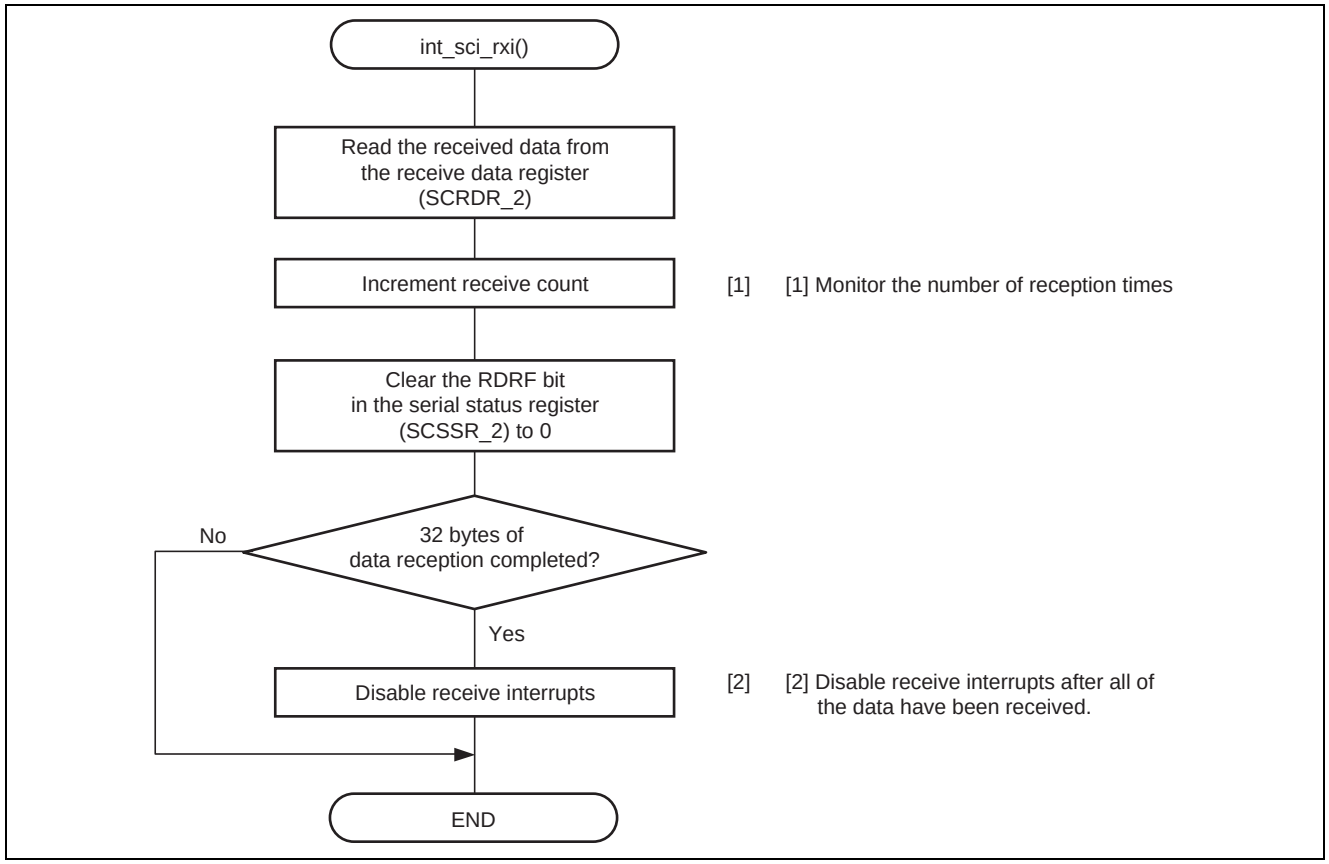


Figure 8 Flow for Handling Receive Interrupts in Clock Synchronous Mode

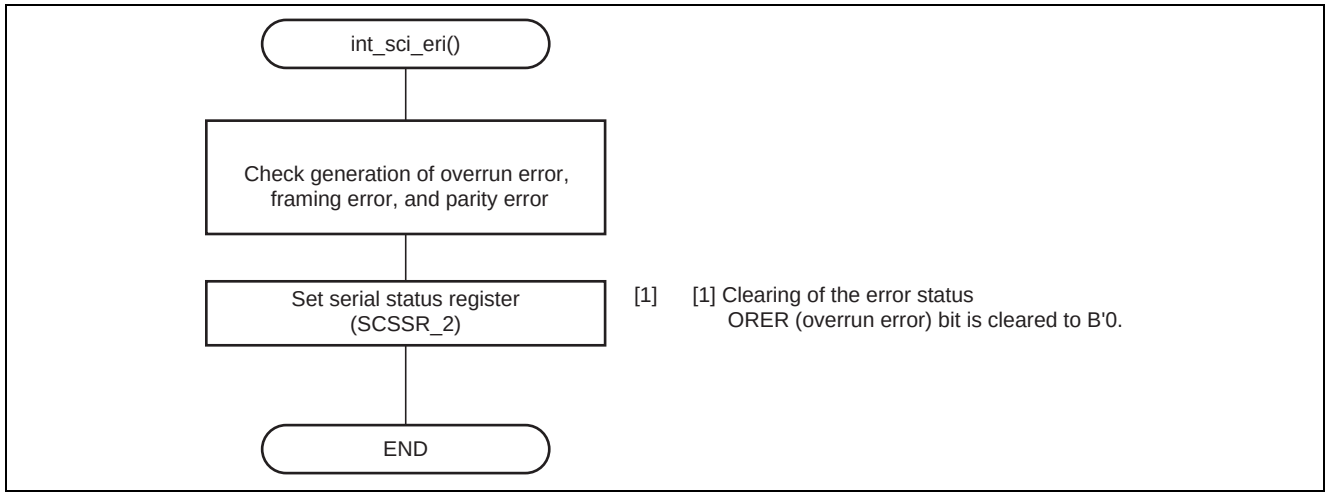


Figure 9 Flow for Handling Receive Error Interrupts in Clock Synchronous Mode

2.4 Procedure for Processing by the Sample Program

In this sample task, character strings are received after initialization of SCI2 for data reception in clock synchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample task.

Table 3 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	STC [2:0] = B'001: × 1/2 (Bϕ) IFC [2:0] = B'000: × 1 (Iϕ) PFC [2:0] = B'001: × 1/2 (Pϕ)
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	MSSCS[1:0] = B'01: PLL output clock MSDIVS[1:0] = B'01: × 1/2 (Mϕ)
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	ASSCS[1:0] = B'01: PLL output clock ASDIVS[1:0] = B'01: × 1/2 (Aϕ)

2.4.2 Power-Down Modes

Table 4 gives settings for the standby control register in the sample task.

Table 4 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 5 (STBCR5)	H'FFFE 0418	H'DF	MSTP55 = B'0: SCI2 operates

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample task.

Table 5 Settings for Register of Interrupt Controller

Register Name	Address	Setting	Description
Interrupt priority register 16 (IPR16)	H'FFFE 0C14	H'00F0	IPR16 [7:4] = H'F: SCI2 is at level 15

Note: The order of priority for RXI2 and TXI2 is determined by the order of the offset addresses of the corresponding interrupt vectors. For details of the interrupt priority levels, refer to the description of the interrupt exception handling vector table and priority, in the interrupt controller section of the *SH7280 Group Hardware Manual (REJ09B0393)*.

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample task.

Table 6 Settings for Register of Pin Function Controller

Register Name	Address	Setting	Description
Port E control register L2 (PECRL2)	H'FFFE 3A14	H'5000	PE7MD [2:0] = B'101: RXD2 input
Port E control register L3 (PECRL3)	H'FFFE 3A12	H'0005	PE8MD [2:0] = B'101: SCK2 input/output

2.4.5 Serial Communications Interface

Table 7 gives settings for the registers of the SCI in the sample task.

Table 7 Settings for SCI Register

Register Name	Address	Setting	Description
Serial mode register_2 (SCSMR_2)	H'FFFF 9000	H'80	C/$\overline{A}$ = B'1: Clock synchronous mode CHR = B'0: 8-bit data CKS [1:0] = B'00: Pϕ clock
Bit rate register_2 (SCBRR_2)	H'FFFF9002	D'124	Clock synchronous mode Bit rate: 100 k (bits/s) *[1]
Serial control register_2 (SCSCR_2)	H'FFFF 9004	H'02	Initialization RIE = B'0: Disables receive-data-full interrupt (RXI) and receive-error interrupt (ERI) request RE = B'0: Disables reception of data
			At the time of setting Clock synchronous mode CKE [1:0] = B'10: Internal clock, or SCK pin is used for synchronizing clock output
		H'50	When receiving operation is enabled RIE = B'1: Enables receive-data-full interrupt (RXI) request RE = B'1: Enables reception of data
Serial status register_2 (SCSSR_2)	H'FFFF 9008	H'00	At the time of setting All flags are cleared to 0.

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface of the *SH7280 Group Hardware Manual (REJ09B0393)*.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7280 Group Hardware Manual (REJ09B0393)
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