R8C/35C Group

Low-Speed On-Chip Oscillator Frequency Measurement

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June 11, 2010

1. Abstract

This document describes a method and an application example to measure the low-speed on-chip oscillator frequency using the input capture function (timer RC) in the R8C/35C Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

- MCU: R8C/35C Group

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

The low-speed on-chip oscillator frequency can be measured by using the input capture function to detect the rising edge of the fOCO-S clock divided by 128 (fOCO128). (1). When detecting an active edge or when the timer RC counter overflows, generate a timer RC interrupt. When an interrupt is generated by overflow (OVF is 1), count the number of overflows. When an interrupt is generated by detecting an active edge (IMFA is 1), read the value in the general register (TRCGRA) as the current value and the value in the buffer register (TRCGRC) as the previous value. The frequency measurement value can be calculated using the value read from the main processing the number of overflows.

Settings

- Select fOCO40M as the timer RC count source.
- Detect the input capture at a rising edge.
- Enable interrupts when detecting an active edge.
- Enable interrupts when the timer RC counter overflows.

Frequency calculation

- Refer to Figure 3.2 for the formula.

Note:

1. The fOCO-S clock generated by the low-speed on-chip oscillator is used as the clock source.

Figure 3.1 shows a Block Diagram. Figure 3.2 shows a Timing Diagram.

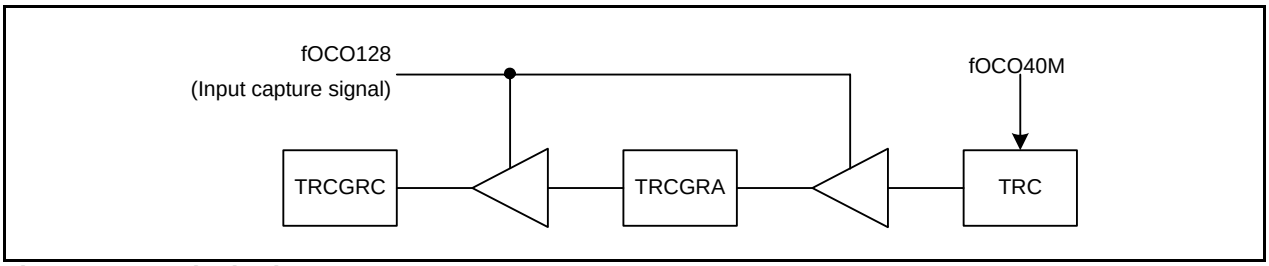
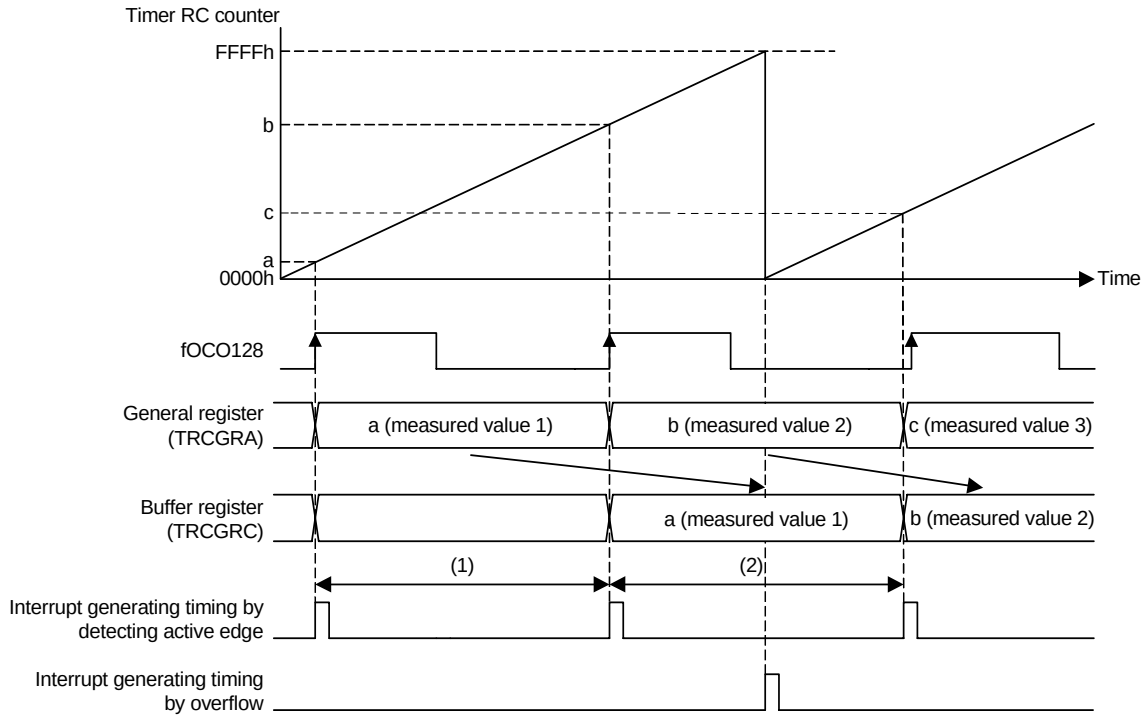


Figure 3.1 Block Diagram



(1): Measured value 2 – measured value 1 (no overflow)
(2): 10000h – measured value 2 + measured value 3 (one overflow)

Frequency based on the calculation result:
Frequency = 1 ÷ (calculation result × time for one count) (timer per count = 1/40 MHz (typ) = 25 ns)
Examples:
1. Frequency when the result for (1) is 46000
Frequency = 1 ÷ (25 ns × 46000) = 869.5 Hz
Low-speed on-chip oscillator frequency = 869.5 Hz × 128 = 111.3 kHz
2. Frequency when the result for (2) is 39000
Frequency = 1 ÷ (25 ns × 39000) = 1025.6 Hz
Low-speed on-chip oscillator frequency = 1025.6 Hz × 128 = 131.3 kHz

Figure 3.2 Timing Diagram

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	301 bytes	In the rej05b1243_src.c module
RAM	11 bytes	In the rej05b1243_src.c module
Maximum user stack	9 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group hardware user's manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (high-speed on-chip oscillator).		

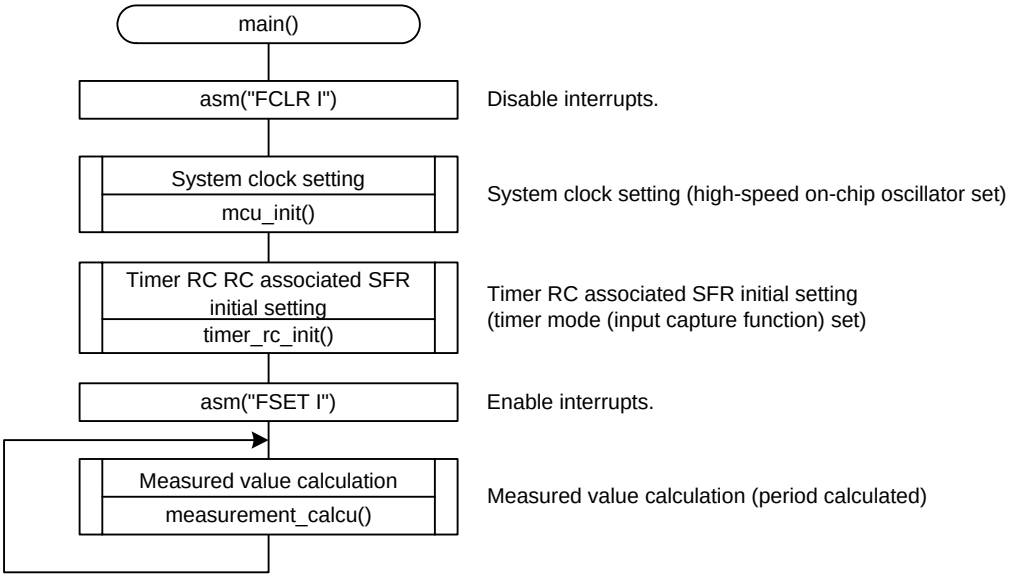
Declaration	void timer_rc_init(void)		
Outline	Timer RC associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform initial setting for the SFR register to use timer RC for the input capture.		

Declaration	void measurement_calcu(void)		
Outline	Measured value calculation		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char f_capture		Capture flag
	unsigned short ovf_cnt		Overflow counter
	unsigned short present_value		RAM for retaining TRCGRA register value
	unsigned short last_value		RAM for retaining TRCGRC register value
	unsigned long measurement_value		RAM for retaining measured value
Returned value	Type	Value	Meaning
	None	—	—
Function	Calculate the measured value based on the number of overflows, the read TRCGRA register value, and TRCGRC register value.		

Declaration	void _timer_rc(void)		
Outline	Timer RC interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char f_capture		Capture flag
	unsigned short ovf_cnt		Overflow counter
	unsigned short present_value		RAM for retaining TRCGRA register value
	unsigned short last_value		RAM for retaining TRCGRC register value
Returned value	Type	Value	Meaning
	None	—	—
Function	Count the number of overflows when timer RC overflows. Read the TRCGRA register value and TRCGRC register value at input capture.		

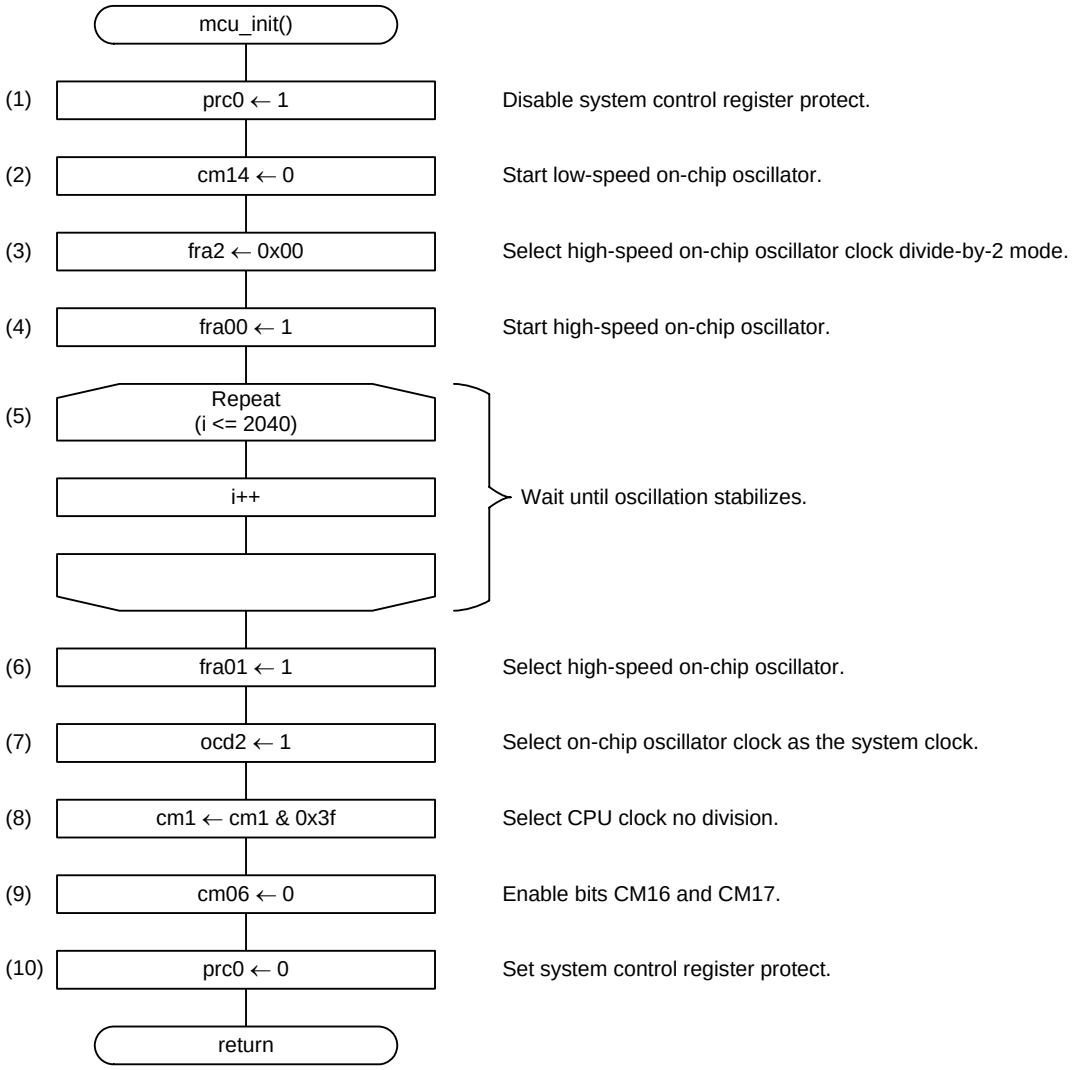
4.2 Main Function

• Flowchart



4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the division ratio for the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

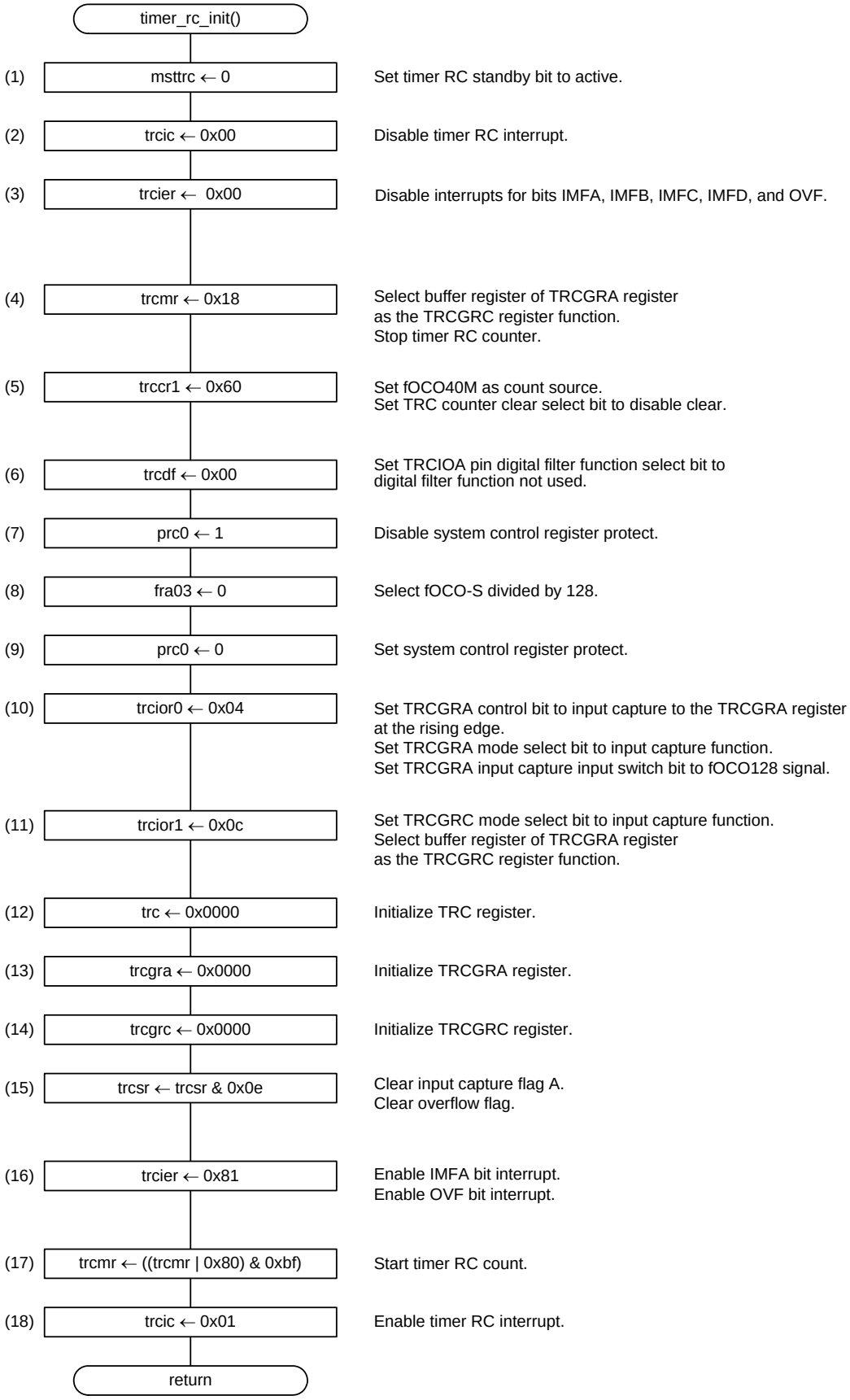
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Timer RC Associated SFR Initial Setting

• Flowchart



• Register settings

(1) Set the timer RC module to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b5	MSTTRC	Timer RC standby bit	0: Active	R/W

(2) Disable the timer RC interrupt.

Interrupt Control Register (TRCIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(3) Disable all timer RC interrupt sources.

Timer RC Interrupt Enable Register (TRCIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit	R/W
b7	OVIE	Overflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit	R/W

(4) Set the timer RC mode register.

Timer RC Mode Register (TRCMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	x	1	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	BFC	TRCGRC register function select bit	1: Buffer register of TRCGRA register	R/W
b7	TSTART	TRC count start bit	0: Count stops	R/W

(5) Set timer RC control register 1.

Timer RC Control Register 1 (TRCCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	1	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	TCK0	Count source select bit	b6 b5 b4 1 1 0: fOCO40M	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation)	R/W

(6) Set the timer RC digital filter function select register.

Timer RC Digital Filter Function Select Register (TRCDF)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	—	x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit	0: Function is not used	R/W

(7) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(8) Select fOCO-S divided by 128.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	—		

Bit	Symbol	Bit Name	Function	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected	R/W

(9) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

(10) Set timer RC I/O control register 0.

Timer RC I/O Control Register 0 (TRCIOR0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	x	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit	1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit	0: fOCO128 signal	R/W

(11) Set timer RC I/O control register 1.

Timer RC I/O Control Register 1 (TRCIOR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	1	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	IOC2	TRCGRA control bit	1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	1: General register or buffer register	R/W

(12) Initialize the timer RC counter to 0000h.

Timer RC Counter (TRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15-b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

(13) Initialize timer RC general register A to 0000h.

Timer RC General Register A (TRCGRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15-b0	General register. Can be used to read the TRC register value at input capture.	R/W

(14) Initialize timer RC general register C to 0000h.

Timer RC General Register C (TRCGRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15-b0	Buffer registers. Can be used to hold transferred value from the general register.	R/W

(15) Clear input capture flag A and overflow flag.

Timer RC Status Register (TRCSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read	R/W
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read	R/W

(16) Set bits IMIEA and OVIE to enable the interrupts.

Timer RC Interrupt Enable Register (TRCIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	1: Enable interrupt (IMIA) by the IMFA bit	R/W
b7	OVIE	Overflow interrupt enable bit	1: Enable interrupt (OVI) by the OVF bit	R/W

(17) Start the timer RC count.

Timer RC Mode Register (TRCMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	x		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRC count start bit	1: Count starts	R/W

(15) Enable the timer RC interrupt.

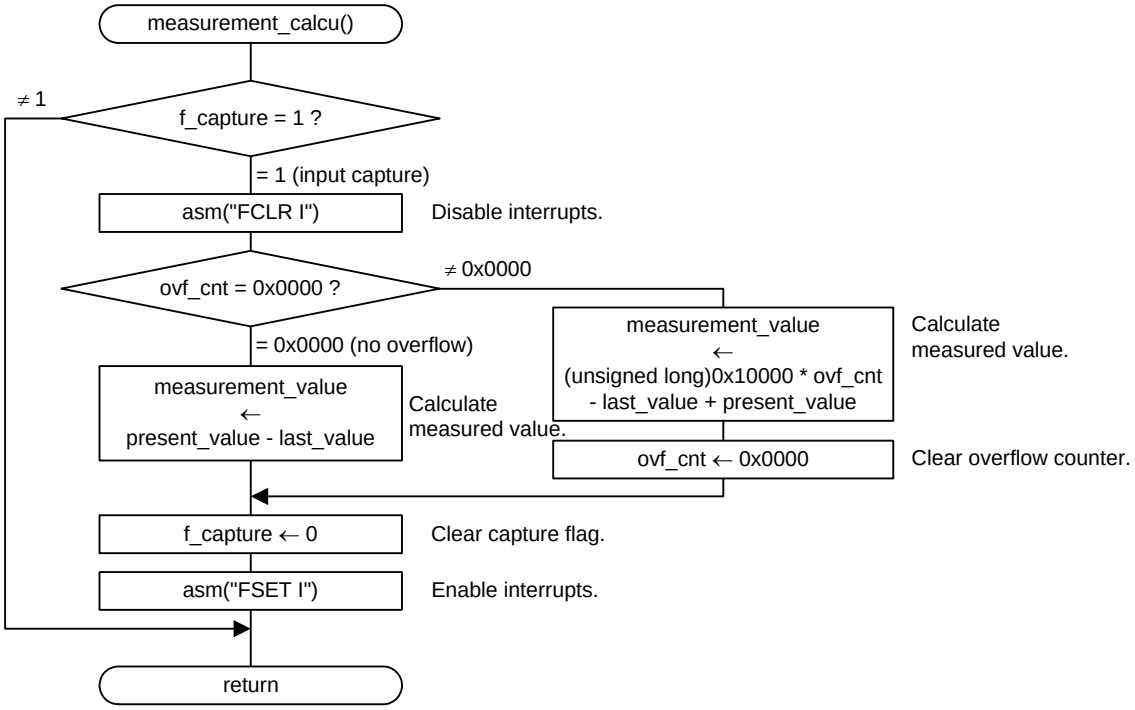
Interrupt Control Register (TRCIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 1: Level 1	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

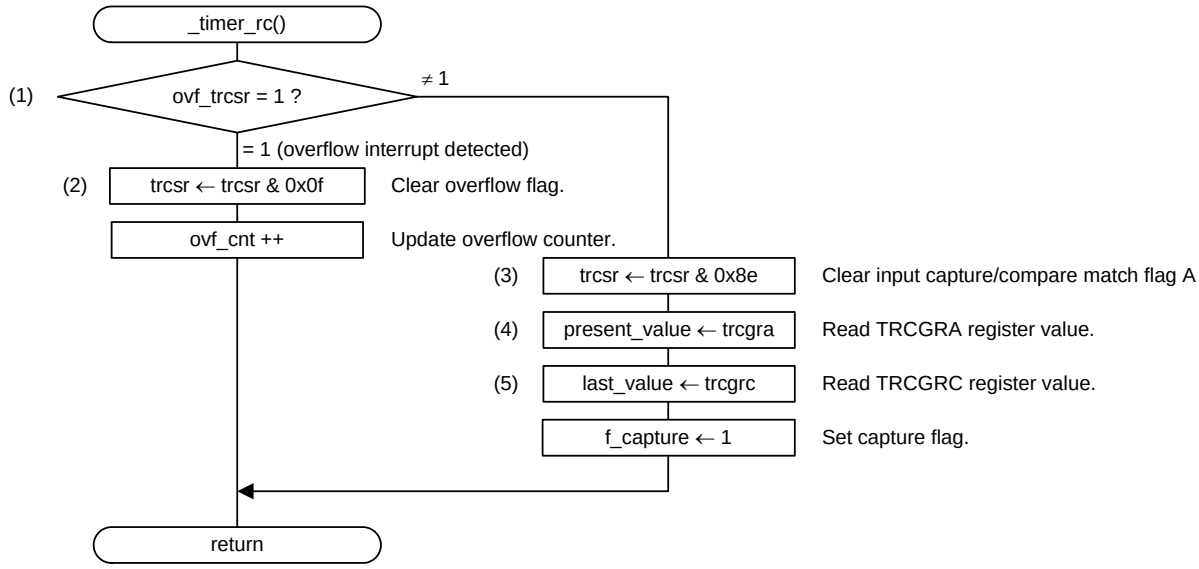
4.5 Measured Value Calculation

• Flowchart



4.6 Timer RC Interrupt Handling

• Flowchart



• Register settings

(1) Verify that timer RC counter overflowed.

Timer RC Status Register (TRCSR)

Bit	Symbol	Bit Name	Function	R/W
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read [Source for setting this bit to 1] When the TRC register overflows	R/W

(2) Clear the overflow flag.

Timer RC Status Register (TRCSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	—	—	x	x	x	

Bit	Symbol	Bit Name	Function	R/W
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read	R/W

(3) Clear input capture/compare match flag A.

Timer RC Status Register (TRCSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read	R/W

(4) Read the TRCGRA register value as the current value.

Timer RC General Register A (TRCGRA)

Bit	Function	R/W
b15-b0	General register. Can be used to read the TRC register value at input capture.	R/W

(5) Read the TRCGRC register value as the previous value.

Timer RC General Register C (TRCGRC)

Bit	Function	R/W
b15-b0	Buffer registers. Can be used to hold transferred value from the general register.	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/35C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/35C Group Low-Speed On-Chip Oscillator Frequency Measurement

Rev.	Date	Description	
		Page	Summary
1.00	June 11, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

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