R8C Family

Implementing System Timer in MR8C/4

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Introduction

The heartbeat of every kernel is the time tick, often called system timer. Without a system timer in the RTOS, no events can occur. Depending on the complexity of the RTOS, for every system tick, the kernel will conduct checks on the need to switch tasks, call a particular cyclic or alarm subroutine, etc.

This document discusses the fundamental principles of system timers and explains in greater details the mechanism and implementation methodology of MR8C/4 system timer.

Target Device

Applicable MCU: R8C Family

Contents

1. Guide in using this Document

This document provides detail and simple explanations in evaluating the need for a system timer and the steps of implementing it in MR8C/4.

Table 1 Explanation of Document Topics

Topic	Objective	Pre-requisite
What is a Tick?	Explanation on the fundamental principles of system timer	Knowledge in embedded system
Resolution of System Timer	Discussion on the most critical step in setting up a system timer	Knowledge in embedded system
How MR8C/4 System Timer Works?	Explanation on how system timer works in MR8C/4	Knowledge in MR8C/4
How to Implement System Timer in MR8C/4	Listing of steps in the implementation of system timer in MR8C/4	Knowledge in MR8C/4
Reference Documents	Listing of documents that equip users with knowledge in the pre-requisite requirements	None

2. What is a Tick?

In an RTOS, every moment within the kernel is referred to as a tick. A tick can be measured in seconds, milliseconds or even microseconds. Ticks provide a measurement of elapsed time durations. An RTOS provides a mechanism for tracking this elapsed time through a system timer. This timer is in turned triggered in the application via a periodic interrupt. Figure 1 illustrates an occurrence of a system timer interrupt. Every time it is triggered, the timer increments a counter that holds the number of elapsed ticks. Subsequent readings taken are compared to provide a measure of elapsed time durations.

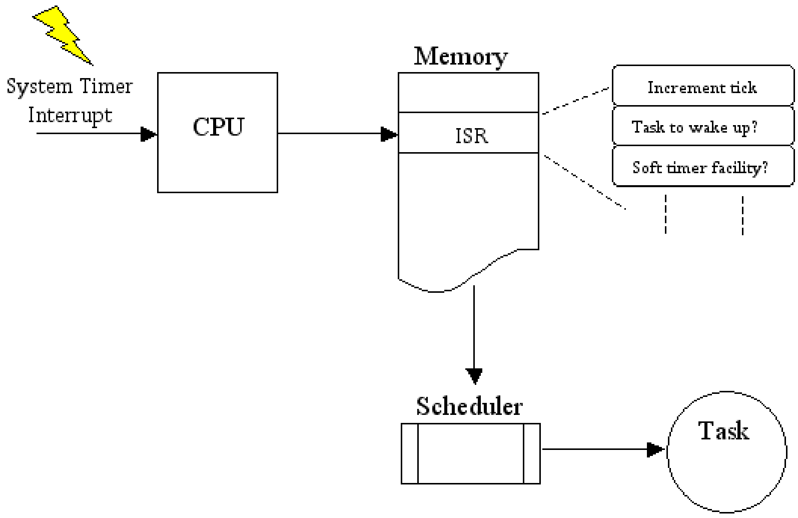


Figure 1: System Timer Interrupt Servicing

3. Resolution of System Timer

A crucial step in the setup of system timer is the definition of its resolution, meaning the accuracy it offers to measure time. Resolution defines the rate at which the timer is triggered to make it sufficient for performing time-based services (e.g. to delay a task or track elapsed time for an alarm handler).

Several considerations are required in the definition of a system timer resolution. They can be generally classified as below:

- Application where RTOS is implemented
- Storage of system timer counter
- Understanding limitation of hardware timer

3.1 Application where RTOS is implemented

The resolution required is dependent on the application nature of the RTOS. A system tick rate of 1Hz (i.e. 1sec) probably will be sufficient for a fluid level monitor whereas a keypad reader might need a system tick rate of 100Hz (i.e. 10ms) in order to specify delays for key debounce algorithm. However, an unduly fast system tick rate will result in substantial overhead and incurred extra consumption of processing power, and should be avoided.

3.2 Storage of system timer counter

In MR8C/4, a 6-bytes system timer variable (refer to Figure 2) was allocated for holding the tick count value. With a maximum system tick resolution of 1ms, it was possible to provide a maximum specifiable counting of up to a whopping 8925 years, thereby alleviating the concern of overflow.

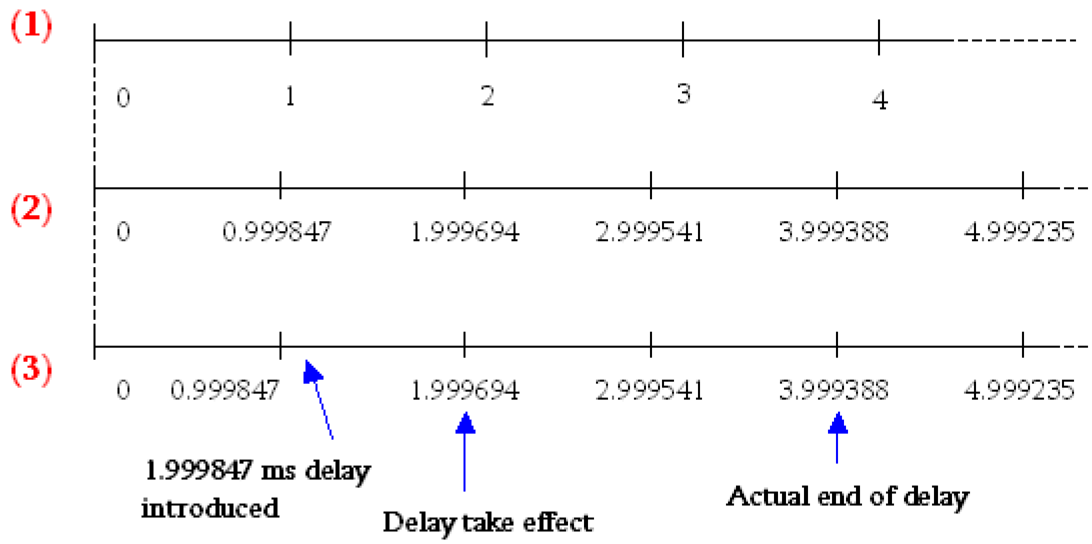
Figure 2: MR8C/4 System Timer Counter Variable

3.3 Understanding Limitation of Hardware Timer

Not all hardware timers can accurately generated the timing users specified. For example, IBM PC hardware timer is only able to generate a tick rate of 999,847 nanoseconds. If a user specify a delay of 2 milliseconds, actual delay achieved will be greater than 2 milliseconds.

Firstly, the execution of delay function is asynchronous with the running of system timer interrupt (i.e. delay function can be called in-between tick counts). In order to ensure the minimum specified delay is achieved, one additional clock tick will be added.

Secondly, due to the discrepancy between the tick rate of the hardware timer (i.e. 999,847 nanoseconds) and the tick rate required (i.e. 1 milliseconds), additional delay will be incurred. Figure 3 further illustrates these explanations.



1. Perceived system timer tick rate of 1 ms.
2. Actual hardware timer tick rate at 0.999847 ms. User wants to implement one-tick delay of 1 ms but will only get one-tick delay of 0.999847 ms.
   To ensure a minimum delay of 1 ms is achieved, additional clock tick need to be added. Projected delay will be 1.999847ms (1ms delay + 0.999847ms).
3. If a delay duration of 1.999847ms is introduced, it spans across more than 2 tick counts (i.e. 1.999847/0.999847 = 2.00015). As delay function will only be activated at the next clock tick, actual delay incurred will be 3 x 0.999847 = 2.999541ms.

Figure 3: Hardware Timer Limitation

4. How MR8C/4 System Timer Works?

In MR8C/4, users specify one of the hardware timers in R8C devices as the system timer. This hardware timer will trigger interrupt at a frequency defined by users. Figure 4 gives an overview of the system timer interrupt processing MR8C/4.

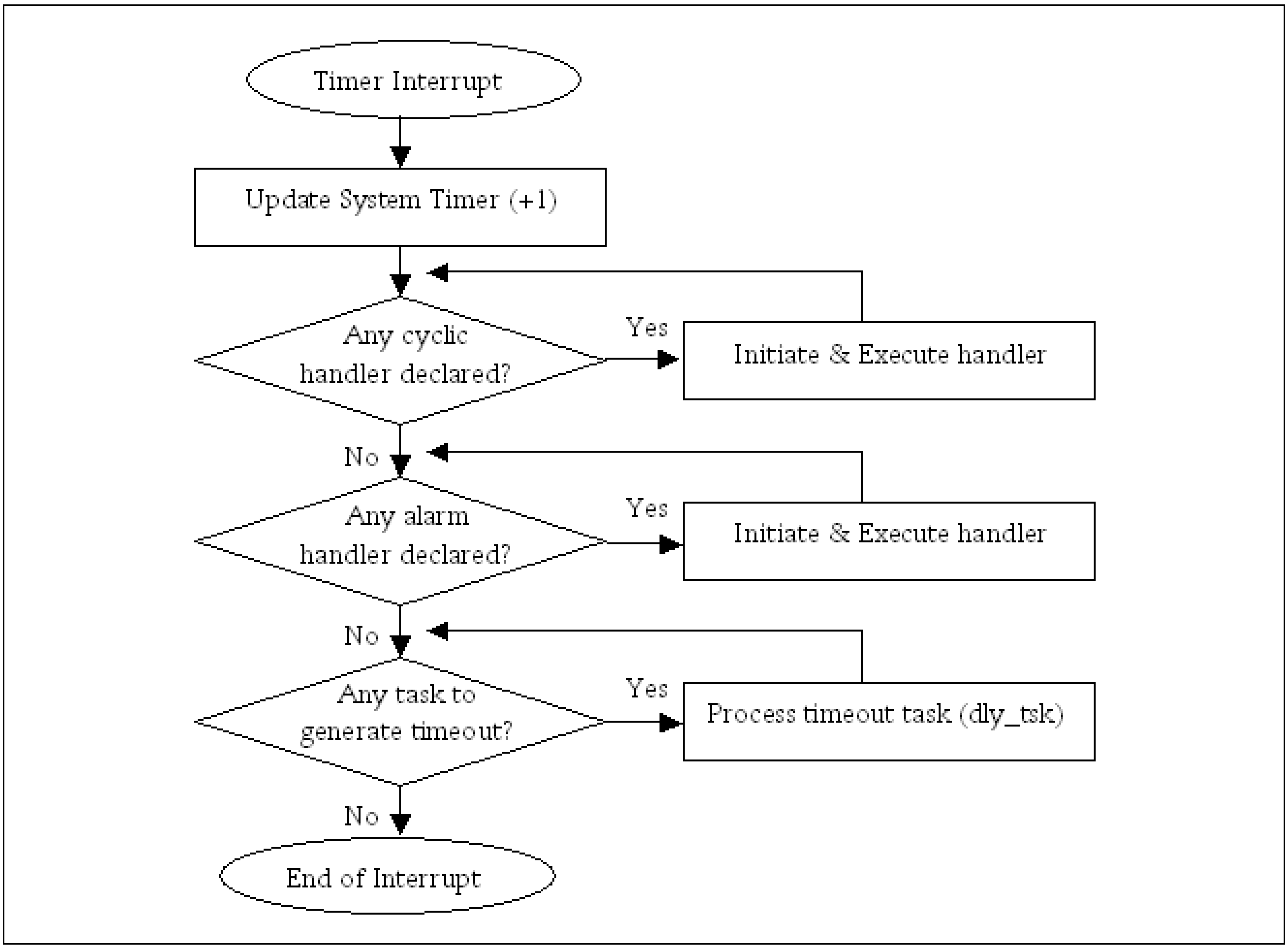


Figure 4: System Timer Interrupt Processing

As shown in Figure 4, system timer interrupt involves processing of time management functions (i.e. time event handlers and "*dly_tsk*" service call). Therefore, contrary to other RTOS, it is not mandatory to create a system timer in MR8C/4 if none of the time management functions is used. This eliminates the incurrence of unnecessary overheads.

5. How to Implement System Timer in MR8C/4?

To setup a system timer in MR8C/4, users are required to perform the following steps in the configuration file:

1. Select one of the hardware timers as a system timer
2. Define system timer settings (i.e. interrupt priority level, frequency, resolution)
3. Define system timer interrupt vector

5.1 Selecting Hardware Timer as System Timer

There are four options for this entry. Users can specify either RA, RB, OTHER or NOTIMER. RA denotes the selection of timer RA as system timer. Similarly, RB denotes selection of timer RB. OTHER is used when timer other than timers RA or RB is used as the system timer. If none of the MR8C/4 time management function is used, NOTIMER may be used to specify no system timer to be created.

If OTHER is selected, it is necessary to define the system timer interrupt vector as explained in section 5.3. For all other entries, section 5.3 need not be performed.

```
// system clock definition
clock{
    mpu_clock   = 20MHz;
    timer    = RA;
    IPL = 3;
};
```

Figure 5: Selecting Timer RA as System Timer in Configuration File

5.2 Defining System Timer Settings

The next step is to define the interrupt priority level, MPU operating frequency and resolution of the system timer.

For the definitions of system timer interrupt priority level, users will be able to specify a priority level between 1 to kernel mask level (as system timer interrupt is a kernel interrupt) for the "*IPL*" entry. This priority level also denotes the precedence of time event handlers (i.e. cyclic and alarm handlers).

The resolution of the system timer interrupt is determine by a computation of the time tick numerator and denominator as shown in Figure 6.

Figure 7 illustrates the definition of system timer settings.

$$\text{Time Tick Cycle (milliseconds)} = \frac{\text{tick\_nume (1 to 65535)}}{\text{tick\_deno (fixed at 1)}}$$

Figure 6: Defining System Timer Resolution

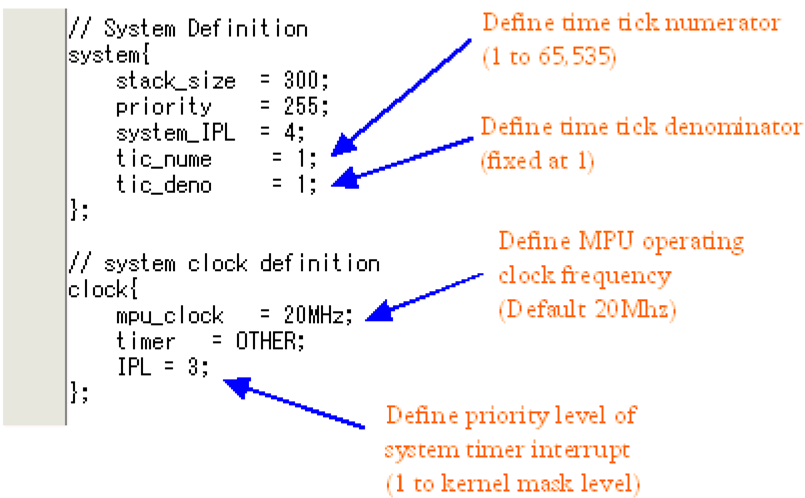


Figure 7: Defining System Timer Settings

5.3 Defining System Timer Interrupt Vector

This step specifies the hardware timer (other than timers RA or RB) chosen to be the system timer. For example, if the R8C device chosen has a timer RC and the timer RC is selected as the system timer, users are required to specify the selection of timer RC as a system timer by assigning the system timer handler to the entry address of timer RC interrupt vector. Figure 8 illustrates the assignment of timer RC as the system timer for the R8C/Lx devices.

R8C/Lx Device Relocatable Vector Tables

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	20. Timer RC
Timer RD0	+32 to +35 (0020h to 0023h)	8	TRD0IC	21. Timer RD
Timer RD1	+36 to +39 (0024h to 0027h)	9	TRD1IC	
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC	22. Timer RE
UART2 transmit/NACK2	+44 to +47 (002Ch to 002Fh)	11	S2TIC	25. Serial Interface (UART2)

Configuration File Entries

```
interrupt_vector[7]{
    os_int   = YES;
    entry_address   = _SYS_STMR_INH();
    pragma_switch   = E;
};
```

software interrupt number

entry address of
system timer interrupt handler

Figure 8: Defining System Timer Interrupt Vector

6. Reference Documents

User's Manual

- MR8C/4 V1.00 User's Manual
- R8C Family Hardware Manual

The latest version can be downloaded from the Renesas Technology website

Website and Support

Renesas Technology Website

- http://www.renesas.com/

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	March.01.10	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   - The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     - In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   - Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   - After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   - Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to

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